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ABSTRACT

A DUAL METAL GATE PROCESS: METALS AND THEIR SILICIDES

Methods for forming dual-metal gate CMOS transistors are described. An NMOS and a PMOS active area of a semiconductor substrate are separated by isolation regions. A metal layer is deposited over a gate dielectric layer in each active area. Silicon ions are implanted into the metal layer in one active area to form an implanted metal layer which is silicided to form a metal silicide layer. Thereafter, the metal layer and the metal silicide layer are patterned to form a metal gate in one active area and a metal silicide gate in the other active area wherein the active area having the gate with the higher work function is the PMOS active area. Alternatively, both gates may be metal silicide gates wherein the silicon concentrations of the two gates differ. Alternatively, a dummy gate may be formed in each of the active areas and covered with a dielectric layer. The dielectric layer is planarized thereby exposing the dummy gates. The dummy gates are removed leaving gate openings to the semiconductor substrate. A metal layer is deposited over a gate dielectric layer within the gate openings to form metal gates. One or both of the gates are silicon implanted and silicided. The PMOS gate has the higher work function.

FIGURE 6