

PROTOCOL AWARE DIGITAL CHANNEL APPARATUS**BY**

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Related Patent Applications

[0001] The present application is related to U.S. Patent Application Serial Number _____, filed on a same date as the present application, entitled A METHOD FOR TESTING IN A RECONFIGURABLE TESTER; by George W. Conner, assigned to the same assignee as the present invention, and is incorporated herein by reference.

BACKGROUND

[0002] Automated stored pattern functional testing affords a critical step in the production of integrated circuit (IC) devices to provide parametric and operational characterization of the devices. An automatic test equipment system includes test circuitry that is connected to a control computer. The control computer provides a user interface that accepts and stores functional test pattern data for activating the test circuitry to provide stimulus signals to a device-under-test and receives the response signals from the device-under-test. The response signals are evaluated to determine the parametric and operational characterization of the integrated circuit devices.

[0003] The device-under-test (DUT) is mounted on a device interface board or DIB, which provides the physical interface from/to the pin electronics. The pin electronics circuitry is the electrical interface that provides/receives the

electrical test stimulus/response signals to/from the device-under-test via the DIB. The test stimulus signals from the test circuitry are supplied through pin electronics to the device-under-test via the DIB. The test response signals from the device-under-test are transferred through DIB to the pin electronics and on to the test circuitry. The test stimulus signals and the test response signals are correlated by the test circuitry to determine whether the device-under-test has passed or failed the test.

[0004] The stimulus signals generated by the test circuitry include data signals and clock signals to synchronize the stimulus input. The effectiveness of the test depends on the accurate placement of these signals relative to one another. For example, several different signals, such as, clock, data, and enable signals are coordinated and triggered at appropriate times to ensure that meaningful data is acquired during the test process. Inaccuracy of clock and data signal edge placement will result in false test results. As the operating speed of devices to be tested increases, the margins of error for edge placement accuracy decreases.

[0005] A system-on-a-chip (SOC) provides multiple digital and analog integrated circuit functions incorporated on the same semiconductor substrate. An example of an SOC is a cellular telephone that incorporates not only cellular telephone receiving, processing, and transmitting functions, but also photographic and video processing functions, audio digital signal processing and semiconductor memory circuits. Presently, in most SOC testing, the individual functions of an SOC are tested separately in multiple testing methods, such as by SCAN testing, Built-In-Self-Test (BIST), and functional testing. System Level Test typically employs custom circuitry and is

generally only used for high average selling price low mix devices, such as microprocessors. A final system level test may be implemented on customized test apparatus created specifically for the testing of specific SOC devices such as microprocessors. Although it would be desirable to perform a System Level Test for other SOC devices, building custom functional test apparatuses for low average selling price SOCs is not cost effective.

[0006] A difficulty in testing SOCs with automatic test circuitry is that the parametric and individual functional testing with the automatic test circuitry is a deterministic test operation. The test stimulus signals are applied with certain timing and structure, and the test response signals are expected to have a particular timing and structure. If the test response signals do not match the expected timing and structure for the given parameters, the SOC device-under-test is determined to have failed. The functions of the SOC device may operate with differing timing and clocking specifications and may in fact operate asynchronously. An SOC device may be operational when the response test signals indicate otherwise, when the asynchronicity of the communicating functions cause the test response signals to appear incorrect.

[0007] There have been attempts within present automatic test equipment systems to simulate the operating conditions of an SOC device-under-test. Because of the nondeterministic function of the asynchronous communication between circuit functions, the normal operating environment of the functions can not be accurately recreated for the SOC device-under-test. Present automatic test equipment environments lack the ability to easily and accurately provide the nondeterministic electrical and timing conditions of the normal operating environment of the

SOC device-under-test. This lack of the nondeterministic electrical and timing conditions within automatic test equipment systems, further do not measure the margin of error for an SOC device-under-test with regard to its tolerance under varying
5 operational conditions that may be present in its normal operational environment.

[0008] Therefore, what is needed is an automatic test equipment system capable of providing deterministic and nondeterministic test stimulus signals. The nondeterministic
10 test stimulus signals provide the electrical and timing protocol of the normal operating environment of the device-under-test such that the automatic test equipment system responds to test response signals of the device-under-test as though the device-under-test is operating in its normal environment.

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SUMMARY

[0009] In one embodiment, provided is a protocol specific circuit for simulating a functional operational environment into which a device-under-test is placed for
20 functional testing. The protocol specific circuit includes a protocol aware circuit constructed to receive a non-deterministic signal communicated by a device-under-test and to control a transfer of the test stimulus signal to the device-under-test in response to the a non-deterministic signal.

[0010] In some embodiments the protocol specific circuit
25 is constructed to receive the non-deterministic signal communicated by a protocol specific device-under-test via pin electronics and to control transfer of the test stimulus signal from a test signal generator to the device-under-test. In some
30 embodiments, the protocol specific circuit is constructed to store the test stimulus signal from the test signal generator in

a stimulus signal storage device, such as a FIFO. In some embodiments, the protocol specific circuit is constructed to store the non-deterministic signal in a response signal storage device, such as a FIFO.

5 [0011] In various embodiments, the protocol specific circuit is constructed to extract the non-deterministic signal from the response signal storage device for comparison by a failure processor with an expected response signal, and determine an operational condition of the device-under-test.

10 [0012] In some embodiments, the protocol specific circuit is constructed for mounting in automated test equipment to allow the automatic test equipment to simulate a functional operational environment into which the device-under-test is placed for functional testing and the protocol aware circuit
15 interprets the non-deterministic signal to determine a synchronization time and a latency time for transmission of the test stimulus signal.

[0013] In another embodiment, provided is a protocol specific circuit having a configurable protocol aware circuit
20 capable of being preconfigured to communicate test stimulus signal between a test signal generator and a specific device-under-test via pin electronics in response to a non-deterministic signal from the device-under-test.

[0014] In some embodiments, the protocol specific
25 circuit is preconfigured to respond to a specific device-under-test in response to the non-deterministic signal having an asynchronously occurring signal from the device-under-test. In some embodiments, the protocol specific circuit includes a protocol decoder, which may be programmable, such as a field
30 programmable gate array. In some embodiments, the field

programmable gate array includes the protocol aware circuit coupled to a memory device, such as a FIFO.

[0015] In some embodiments, the protocol specific circuit includes a memory buffer configured to store the test stimulus signal generated by the test signal generator and to provide the stored test stimulus signal via the pin electronics, to the device-under-test in response to a non-deterministic signal from the device-under-test. The memory buffer may be a FIFO.

[0016] In various embodiments, the protocol specific circuit includes a pass-through circuit coupled in parallel with the protocol aware for receiving deterministic signals from the device-under-test.

[0017] In another embodiment, provided is test equipment including a protocol aware channel for testing a device-under-test, the protocol aware channel includes a protocol specific circuit coupled between a test signal generator and a pin electronics circuit, the protocol specific circuit is constructed to be capable of being preconfigured to respond to the protocol specific device-under-test in response to a non-deterministic signal from the device-under-test.

[0018] In some embodiments, the protocol specific circuit includes a protocol decoder. In some embodiments, the protocol specific circuit includes a field programmable gate array, which may include the protocol aware circuit coupled to a memory device. In some embodiments, the protocol specific circuit includes a memory buffer configured to store the at least one test stimulus signal generated by the test signal generator and to provide the stored test stimulus signal via the pin electronics, to the device-under-test in response to a non-deterministic signal from the device-under-test. In some

embodiments, the protocol specific circuit includes a pass-through circuit coupled in parallel with the protocol aware for receiving deterministic signals from the device-under-test.

BRIEF DESCRIPTION OF THE DRAWINGS

5 [0019] Fig. 1 is a block diagram of an integrated circuit device structure having a non-deterministic behavior.

[0020] Fig. 2 is a block diagram of an embodiment of a protocol specific circuit within an automatic test equipment system.

10 [0021] Fig. 3 is a block diagram of another embodiment an automatic test equipment system incorporating one embodiment of a protocol specific circuit.

[0022] Fig. 4 is a block diagram of an automatic test equipment system incorporating multiple instances of one of the
15 embodiments of the protocol specific circuits.

[0023] Figs. 5a and 5b are flow diagrams of a method for simulating within an automatic test system a functional operational environment into which a device-under-test is placed for functional testing.

20 [0024] Fig. 6 is a block diagram illustrating a Double Data Rate Random Access Memory Controller protocol, which some embodiments of the protocol specific circuit may simulate.

[0025] Fig. 7 is a block diagram of one embodiment of the protocol specific circuits within an automatic test
25 equipment system configured to simulate the Double Data Rate Random Access Memory Controller protocol of Fig. 6.

[0026] Figs. 8 and 9 are plots respectively of the read and write timing of the Double Data Rate Random Access Memory Controller protocol as generated by one of the embodiments of

the protocol specific circuits within an automatic test equipment system of Fig. 5.

DESCRIPTION

[0027] As described above, in recent years stored pattern functional testing has run into increasing difficulties with devices that do not behave deterministically. Presently, the level of integration and complexity of semiconductor processing is allowing for integrated circuit chips to effectively be a complete "system-on-a-chip" (SOC). A system-on-a-chip integrates all the functional circuit elements of a computer or other electronic system into a single integrated circuit (chip). These integrated circuit elements may be any combination of digital circuits, analog circuits, random access memory, mixed analog and digital signal circuits, and often include radio-frequency functions. Referring to Fig. 1, the SOC devices has multiple intellectual property (IP) integrated circuit element blocks **105a** and **105b**. In the present illustration, only two of the IP blocks **105a** and **105b** are shown for ease of explanation, but it is apparent to one skilled in the art that large numbers of complex IP blocks are integrated on an SOC device **100**. In this illustration, the two IP blocks communicate through an asynchronous interface **110**.

[0028] When the SOC device **100** is tested to determine parametric and functional operation, the SOC device **100** is placed in a device-under-test fixture **125** and connected through pin electronics to the automated test equipment system **120**. The pin electronics provides the electrical interface between the device-under-test and automated test equipment system **120**. The automated test equipment system **120** generates, transmits, receives, and evaluates sets of test patterns **130** and **135** to determine the parametric and functional operation of the SOC device **100**.

[0029] Each of the IP blocks **105a** and **105b** generally has its own clock and timing domains **115a** and **115b** that are generally not synchronized. The test stimulus signal **132** may cause the IP block **105a** to communicate with the IP block **105b**, which will cause the test response signal **139** of the IP block **105b** to be incorrect. Similarly, the test stimulus signal **137** may cause the IP block **105b** to communicate with the IP block **105a**, which will cause the test response signal **134** of the IP block **105a** to be incorrect. This nondeterministic communication will vary between SOC devices **100** and within the same SOC device **100** at different voltages and temperatures.

[0030] The current generation automated test equipment systems **120** are capable of providing the test stimulus signals **132** to the IP block **105a** and the test stimulus signals **137** to the IP blocks **105b** and receiving the test response signals **134** from the IP blocks **105a** and the test response signals **139** from the IP blocks **105b**. In this case the testing is deterministic in that the test response signals **134** and **139** match certain structures and timing to be valid. Any communication between the IP blocks **105a** and **105b** is curtailed and the interaction is not verified.

[0031] The current generation automated test equipment systems **120** have very limited capability to deal with non-deterministic SOC devices **100** other than provide to certain latency factors. This causes the test engineer significant problems, in that the first prototyped devices, more than likely, will not work when the test stimulus signals **132** and **137** are the simulation vectors used in the design verification. A series of trial and error loops ensues in which the test engineer tries to move vectors around until he finds a passing arrangement. Due to the large volume of data involved and the

need to re-simulate every trial, each loop may take days, the net result being months added to the test and evaluation phase of a new SOC device.

[0032] In all probability, the test engineer may never
5 find a single set of test stimulus signals **132** and **137** that works for all devices and may be faced with supporting many sets of the test stimulus signals **132** and **137**. In this situation, if any one passes, the device is deemed good. This causes a test time penalty for having to support many patterns and there is a
10 very real possibility that not all possible good patterns will have been discovered, thus creating an adverse yield impact.

[0033] In this situation, months can be added to time to market and device yields may be reduced. Some organizations have chosen to address the inability to cope with the
15 nondeterministic functioning of the IP blocks **105a** and **105b** within a SOC device **100** by moving away from functional testing on an automated test equipment system **120** entirely using some form of structural test. While structural test is a necessary ingredient of a successful test plan, it is not sufficient in
20 the present era of semiconductor processing with current geometries.

[0034] To solve the problem of device non-determinism to permit use of automated test equipment systems **120**, an embodiment of an automated test equipment systems **120** includes a
25 protocol specific circuit for simulating a functional operational environment into which an SOC device **100** to be tested is placed for functional testing. The protocol specific circuit is aware of the protocol that the IP blocks **105a** and **105b** are communicating. The basic problem caused by non-
30 determinism is that while the SOC device **100** may end up doing the same thing each time, it doesn't necessarily do it the same

way each time. It may want data presented a cycle earlier or later than the last time it ran. An obvious solution to this behavior is, rather than simply spewing data at the SOC device **100**, to wait until the device is ready for it. In order to wait
5 until the SOC device **100** is ready, however, the automated test equipment system **120**, in some sense, understands the function of the test response signals **134** and **139** from the SOC device **100**.

[0035] To keep up with increasing SOC device **100** speeds, current automated test equipment systems **120** have increased the
10 pipeline depth of the pattern generators. This has allowed the use of low cost CMOS technology for all but the last few transistors in the automated test equipment system **120** channel, yet has permitted speeds in excess of 6.4 Gbps, with patterns that approach Gigabit depth, to be achieved. A side effect of
15 this trend is that if the pattern flow of the automated test equipment system **120** needs to be changed in order to respond to the device, there may be a latency of several microseconds to clear the pipeline.

[0036] A protocol aware circuit is placed as close as
20 possible to the device-under-test fixture **125** and thus to the SOC device **100** to receive the non-deterministic test response signals **134** and **139** communicated by a SOC device **100** through the device-under-test fixture **125**. The protocol aware circuit controls a transfer of test stimulus signals **132** and **137** to the
25 SOC device **100** in response to non-deterministic test stimulus signals **132** and **137**.

[0037] Refer now to Fig. 2 for a detailed explanation of the protocol specific circuit **205** within an embodiment of an automated test equipment system **200**. A data generator **225**
30 creates the test stimulus signals from the test pattern commands stored in the Dynamic Random Access Memory (DRAM) **220**. The test

stimulus signals are transferred to the source memory **230** of the protocol specific circuit **205** which acts to speed match the test stimulus signals to the specifications of the SOC device-under-test **215**.

5 [0038] Ideally, the source memory **230** is a random access memory (RAM) that allows the random access of the test stimulus signals. In a true RAM mode, it may not be necessary to provide test vectors for operation, the DUT can write data in and then read the data out when requested. The RAM typically works for
10 speeds below around 1GHz and port pin counts up to 128 pins, in current technology. However, because of the performance requirements of the SOC device-under-test **215** with faster speeds or wider busses, the source memory **230** may be a First-In-First-Out (FIFO) memory where the test stimulus signals are ordered
15 and transferred at the required speed. It should be noted, that either/both the FIFO and true RAM mode (in addition to other protocols) are supported in various embodiments.

 [0039] The output of the source memory **230** is sent to a transmission buffer circuit **235** that amplifies and conditions
20 the test stimulus signals for transfer on the physical interconnections **237** and **239** to the pin electronics **210a** and **210b**. The pin electronics **210a** and **210b** provides the electrical interface **202** and **204** between the SOC device-under-test **215** and the automated test equipment system **200**. In normal
25 deterministic operation, the test stimulus signals are transferred at determined times and with a determined structure based on the test vectors stored in the DRAM **220**. The test stimulus signals are applied to the desired IP block **217i** of the IP blocks **217a**, **217b**, ..., **217i**, ... and **217n** that populate the SOC
30 device-under-test **215**.

[0040] In the deterministic operation mode, the IP block **217i** responds with the test response signals on the interface **204** to the pin electronics **210a** and **210b**. The pin electronics **210a** and **210b** then transfer the test response signals on the interface **252** to the receiver **250**. The receiver **250** amplifies and conditions the test response signals and transfers them to the capture memory **255**. The capture memory **255** acts to buffer the test response signals for transfer from the protocol specific circuit **205** to the failure processor **260**. The capture memory **255** is generally a FIFO memory where the ordered test response signals are transferred at the required speed.

[0041] The failure processor **260** receives the test response signals from the capture memory **255** and the test stimulus signals from the data generator **225** for comparison. Any of the test response signals that are incorrect are logged to the DRAM **220** for further analysis.

[0042] The deterministic operation mode of the automated test equipment system **200** as described provides the deterministic operation as in the automated test equipment systems of the prior art. The protocol specific circuit **205** has mode selection circuits **240** and **265** that switch from the deterministic operation mode to the non-deterministic operation mode based on the state of the protocol aware selection signal **245**. For the deterministic operation mode, as just described, the protocol aware selection signal **245** is set such that the mode selection circuit **240** has the control of the source memory **230** from the data generator **225** and the mode selection circuit **265** has the control of the capture memory **255** from the failure processor **260**. In the non-deterministic operation mode, the protocol aware selection signal **245** is set such that the control

of the source memory **230**, and the capture memory **255** is from a protocol aware engine **270**.

[0043] The protocol aware engine **270** may be a reconfigurable integrated circuit such as for example a field programmable gate array (FPGA) that is reconfigured to accept a protocol from the SOC device-under-test **215**, decode the protocol into a command, address, and/or data. From the received command, address, timing, and/or data, the protocol aware engine **270** determines the structure and the timing of the test stimulus signals that are to be transferred from the source memory **230** to the IP block **217i** through the transmitter **235** and the pin electronics **210a** and **210b**. For example, if the automated test equipment system **200** is to stimulate random access memory (RAM) and the IP block **217i** of the SOC device-under-test **215** is a memory controller, the memory controller **217i** sends test response signals that when decoded are the address, command, control, timing, and data for a RAM. The protocol aware engine **270** receives test response signals and decodes the test response signals into the address, command, control, timing, and data. The protocol aware engine **270** determines the structure and timing of the test stimulus signals that are to be supplied to the IP block **217i** of the SOC device-under-test **215**. In the case of a read command of the RAM, the protocol aware engine **270** determines the read latency timing and the structure of the data to be transferred and commands the source memory **230** to transfer the test stimulus signals accordingly. In the case of the write, the protocol aware engine **270** decodes the address and commands from the capture memory **255** to store the written data. The protocol aware engine **270** also initiates any response acknowledging the write as a test stimulus signal to the IP block **217i**. In this action, any of the IP blocks **217a**, **217b**, ...,

and **217n** that are being tested will interact with the IP block **217i** in a functionally correct manner as though the SOC device-under-test **215** were in its standard operating environment.

[0044] It should be noted that the source memory **230** and
5 the capture memory **255** could be random access memories such as a static RAM or dynamic RAM. However, in simulating the operating environment of a high performance SOC device-under-test **215**, the source memory **230** and the capture memory **255** may be First-In-First-Out (FIFO) memories. The FIFO memories by their nature
10 allow faster transfer and receipt of the test stimulus signals than do the static and dynamic RAM's.

[0045] To assure appropriate synchronicity of the transfer of the test response signals, the protocol aware engine **270** may optionally be clocked by the Device-Under-Test clock **280**
15 during the non-deterministic mode of operation and the automated test equipment system **200** clock **285** for deterministic operation. The automated test equipment system **200** clock **285** may be optionally selected when automated test equipment system **200** is initiating the non-deterministic operation, as a master, and is
20 thus the source of the clock. The optional multiplexer **275** is controlled by the aware selection signal **245** to control the operational mode of the protocol aware engine **270** between the deterministic and the non-deterministic modes.

[0046] The protocols that various embodiments of the
25 automated test equipment system **200** may be required to simulate fall generally into two broad categories. In a first example, the SOC device-under-test **215** controls the interface between automated test equipment system **200** and the SOC device-under-test **215**. In a second example, the automated test equipment
30 system **200** controls the interface between the SOC device-under-test **215** and the automated test equipment system **200**. In the

first example, the SOC device-under-test **215** communicates the non-deterministic signals and the automated test equipment system **200** responds. In the second example, the automated test equipment system **200** sends the test stimulus signals with the appropriate protocol structure and timing to the SOC device-under-test **215** and the SOC device-under-test **215** responds with the non-deterministic test response signals that are decoded, as described above. In either example, the automated test equipment recognizes a non-deterministic response signal from the SOC device-under-test and response.

[0047] Refer now to Fig. 3 for a detailed explanation of another embodiment of a protocol specific circuit **305** within an automated test equipment system **300**. The protocol specific circuit **305** has a channel function generator **325** that creates the test stimulus signals from the test pattern commands stored in the Dynamic Random Access Memory (DRAM) **320**. The channel function generator **325** communicates with the memory controller **360** to retrieve the test pattern commands from the DRAM **320**. The memory controller **360** generates the necessary address, timing, and command signals for accessing the test pattern commands from the DRAM **320**. The memory control **360** receives the test pattern commands and transfers them to the channel function generator **325**. The test pattern commands are then decoded to form the test stimulus signals. The test stimulus signals are then transferred to the through the mode selection circuits **340** and **365** to the transmission buffer circuit **335**. The transmission buffer circuit **335** amplifies and conditions the test stimulus signals for transfer on the physical interconnections **337** and **339** to the pin electronics **310a** and **310b**. The pin electronics **310a** and **310b** provides the electrical interface **302** and **304** between the SOC device-under-test **315** and

the automated test equipment system **300**. In normal deterministic operation, the test stimulus signals are transferred at determined times and with a determined structure based on the test vectors stored in the DRAM **320**. The test stimulus signals are applied to the desired IP block **317i** of the IP blocks **317a**, **317b**, ..., **317i**, ... and **317n** that populate the SOC device-under-test **315**.

[0048] In the deterministic operation mode, the IP block **317i** responds with the test response signals on the interface **304** to the pin electronics **310a** and **310b**. The pin electronics **310a** and **310b** then transfer the test response signals on the interface **352** to the receiver **350**. The receiver **350** amplifies and conditions the test response signals and transfers them to the capture memory **355**. The capture memory **355** acts to buffer the test response signals for transfer to the memory controller **360** and the channel function generator. The capture memory **355** is generally a FIFO memory where the ordered test response signals are transferred at the speed dictated by the specification of the IP block **317i**.

[0049] The channel function generator **325** receives and compares the test response signals and the test stimulus signals. Any of the test response signals that are incorrect are logged to the DRAM **320** through the memory controller **360** for further analysis.

[0050] The deterministic operation mode of the automated test equipment system **300** as described provides the deterministic operation as in the automated test equipment systems of the prior art. The mode selection circuits **340** and **365** switch from the deterministic operation mode to the non-deterministic operation mode based on the state of the protocol aware selection signal **345**. For the deterministic operation

mode, as just described, the protocol aware selection signal **345** is set such that the channel function generator **325** controls the transfer of the test stimulus signals from the channel function generator **325**. In the non-deterministic operation mode, control of the source memory **330**, and the capture memory **355** is from a protocol decode circuit **370**. The transmission of the test stimulus signals is transferred from the channel function generator **325** to the protocol decode circuit **370**.

[0051] The protocol decode circuit **370** may be a reconfigurable integrated circuit such as a field programmable gate array (FPGA) that is configured to accept a protocol from the SOC device-under-test **315**, decode the protocol into a command, address, and/or data. From the received address, command, control, timing, and data, the protocol decode circuit **370** determines the structure and the timing of the test stimulus signals defined by the specification of the IP block **317i**. The protocol decode circuit **370** communicates with the source memory **330** which extracts the necessary test stimulus signals from the DRAM **320** through the memory controller **360**. The test stimulus signals are transferred through the mode selection circuit **340** from the source memory **330** and those test stimulus signals that represent command responses to the IP block **317i** are transferred through the mode selection circuit **365**. The test stimulus signals are transferred through the interconnections **337** and **339** to the pin electronics **310a** and **310b** to the IP block **317i** of the SOC device-under-test **315**. For example, if the automated test equipment system **300** is to stimulate random access memory (RAM) and the IP block **317i** of the SOC device-under-test **315** is a memory controller, the memory controller sends test response signals that when decoded are the address, command, control, timing, and data for a RAM. The protocol decode circuit **370**

receives test response signals and decodes the test response signals into the address, command, control, timing, and data. The protocol decode circuit **370** determines the structure and timing of the test stimulus signals that are to be supplied to the IP block **317i** of the SOC device-under-test **315**. In the case of a read command of the RAM, the protocol decode circuit **370** determines the read latency timing and the structure of the data to be transferred and commands the source memory **330** to transfer the test stimulus signals accordingly with the protocol decode circuit **370** providing any of the specified command and timing response signals for the memory controller of the IP block **317i**.

[0052] In the case of the write, the protocol decode circuit **370** decodes the address and commands the capture memory to store the written data. The protocol decode circuit **370** also initiates responses acknowledging the write as a test stimulus signal to the IP block **317i** through the mode selection circuit **365**, the transmission circuit **335** and the pin electronics **310a** and **310b**. In this action, any of the IP blocks **317a**, **317b**, ..., and **317n** that are being tested will interact with the IP block **317i** in a functionally correct manner as though the SOC device-under-test **315** were in its standard operating environment.

[0053] It should be noted that the source memory **330** and the capture memory **355** are ideally a random access memories such as a static RAM or Dynamic RAM. However, in simulating the operating environment of a high performance SOC device-under-test **315**, the source memory **330** and the capture memory **355** may be First-In-First-Out (FIFO) memories. The FIFO memories by their nature allow faster transfer and receipt of the test stimulus signals than do the Static and Dynamic RAM's. Further, in this embodiment the source memory **330**, the capture memory

355, and the mode selection circuits **340** and **365** are also reconfigurable circuits within an FPGA.

[0054] While this embodiment is shown with a single ATE clock **385** for the protocol specific circuit **305**, the protocol specific circuit **305** may optionally be clocked by the Device-Under-Test clock during the non-deterministic mode of operation and by the automated test equipment system clock **385** during the deterministic mode to assure appropriate synchronicity of the transfer of the test response signals. An optional multiplexer (not shown) similar to the optional multiplexer **275**, as shown in Fig. 2, may be provided to switch between the Device-Under-Test clock and the automated test equipment system clock **385**. The optional multiplexer is controlled by the protocol aware selection signal **345** to control the operational mode of the protocol specific circuit **305** between the deterministic and the non-deterministic modes.

[0055] The embodiments of Figs. 2 and 3 of the automated test equipment system show a single protocol aware channel that includes the protocol specific circuit. In conventional automated test equipment system, there are multiple channels with each channel controlling the stimulus and response for a specific number of pins (i.e. 8 pins) of the SOC device-under-test. The multiple protocol aware channels of the automated test equipment system of some embodiments communicate with other protocol aware channels to decode protocol commands from the SOC device-under-test and then generate and synchronize the test stimulus signals that are the correctly structured and timed responses expected by the SOC device-under-test.

[0056] Refer now to Fig. 4 for a description of the automated test equipment system **400** of this embodiment. The automated test equipment system **400** has multiple channels of the

protocol specific circuits **405a**, ..., **405n** that are connected to multiple pin electronic units **410a**, ..., **410n**. Each of the multiple pin electronic units **410a**, ..., **410n** as described above provide the electrical interface **402a**, ..., **402n** and **404a**, ..., **404n** between the SOC device-under-test **440** and the automated test equipment system **400** through the physical interconnections of the load adapter. Each of the protocol specific circuits **405a**, ..., **405n** is connected to at least one of the multiple pin electronic units **410a**, ..., **410n** to provide the test stimulus signals to and receive the test response signals from the SOC device-under-test **440**.

[0057] Each of the protocol specific circuits **405a**, ..., **405n** has a protocol aware controller **415** which functions as the protocol aware engine **270** of Fig. 2, or the protocol decode circuit **370** of Fig. 3, in coordination with the remaining circuitry of the protocol specific circuit **205** of Fig. 2 or the protocol specific circuit **305** of Fig. 3. Each protocol aware controller **415** of the protocol specific circuits **405a**, ..., **405n** communicates with its designated DRAM **420a**, ..., **420n** to provide the necessary test commands and to log the test results of the exercising of the SOC device-under-test **440**.

[0058] In protocols that have a large number of pins, the protocol specific circuits **405a**, ..., **405n** coordinate the decoding of the commands and generate the test response signals that simulate the expected responses synchronously. To simulate the expected responses synchronously, the protocol specific circuits **405a**, ..., **405n** communicate through a synchronization communication interface **425** between those of the protocol specific circuits **405a**, ..., **405n** that may cooperate. This cooperation may effect the latency of the operation and thus the communication is structured to minimize the impact of the cross

communication between the protocol specific circuits **405a**, ..., **405n**. For instance one of the protocol aware controllers **415** may act as a master and receive the test stimulus signals directly from adjacent protocol specific circuits **405a**, ..., **405n** for decoding. The master protocol aware controller **415** then dispatches the appropriate instructions for constructing the structure and timing of the test response signals specified by the protocol, while minimized the impact of the latency for the operation. The latency synchronization signal line (**ISL**) **435** is used by the master protocol aware controller **415** for dispatching the initiation of a particular protocol action across multiple protocol specific circuits **405a**, ..., **405n**.

[0059] The automated test equipment system **400** may have multiple master oscillators **430a** and **430b** to generate the different timings determined by the protocol specific circuits **405a**, ..., **405n**. This is true especially for the deterministic operation of the automated test equipment system **400**. In the non-deterministic operation of the automated test equipment system **400**, the master oscillators **430a** and **430b** may be used for those portions of the testing involving deterministic operation while an exterior timing from the SOC device-under-test **440** may be used for the protocol aware controller **415** in non-deterministic operation.

[0060] Refer now to Figs. 5a and 5b for a description of a method for simulating within an automatic test system a functional operational environment into which a device-under-test is placed for functional testing. The device-under-test is an SOC integrated circuit that is placed in an adapter (or load) board, i.e. a DIB. The pin electronics provides the electrical interface, via the DIB, between the device-under-test and the test circuitry of the automatic test system. The method begins

by (Box 500) selecting the mode of operation of the automatic test system. If the deterministic mode of operation is determined (Box 505) to be selected, the normal operational testing of the SOC DUT is performed (Box 510). If the non-deterministic mode is determined (Box 505) to be selected, a non-deterministic response signal is received (Box 515) from the SOC device-under-test. Based on a predetermined protocol, an expected stimulus signal to be transferred to the SOC DUT is ascertained (Box 520) from the non-deterministic response signal. Transmission of the expected stimulus signal from the automatic test system to the device-under-test is initiated (Box 525). The non-deterministic response signal is stored (Box 530) within a response capture storage device. The non-deterministic response signal is evaluated (Box 540) to determine if the non-deterministic response signal was correctly transmitted from the SOC DUT to determine an operational condition of the SOC DUT.

[0061] Expected stimulus signals are generated (Box 545) from an encoded stimulus data and stored (Box 550) in an expected stimulus signal storage device. At least one of the expected stimulus signals is selected (Box 560). From the decoded non-deterministic response signal, the timing and latency delay of the expected stimulus signal is synchronized (Box 565) for transmission to the SOC DUT.

[0062] The predetermined protocols of the non-deterministic response signals and the expected stimulus signals may be a random access memory interface protocol, a communication interface protocol, or computing device interface protocol.

[0063] The decoding of the non-deterministic response signal permits the automatic test system to transfer an expected response to the SOC DUT by the expected stimulus signals with

the appropriate timing and latency delays that would be expected in the normal operating environment of the SOC DUT.

[0064] The "JEDEC Standard JESD79-3 - DDR3 SDRAM Standard", JEDEC Solid State Technology Association, Arlington, VA, June 2007, defines the Double Data Rate (DDR3) Synchronous Dynamic Random Access Memory (SDRAM) specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. One of the IP blocks of a SOC DUT, as described above, may be a controller circuit for a memory system containing DDR3 SDRAM. In a functional evaluation of the IP block of the SOC DUT, other IP Blocks may be requesting transfer of data between the controller circuit IP block and the memory system. In a test environment this type of access is not deterministic, but is based on the timing of the interactions between the IP blocks. The controller IP Block will activate the timing, command, control, and data signals to transfer data between the DDR3 SDRAM and the SOC DUT. The automated test equipment system of various embodiments responds with the appropriate signals at the specified timings and structure for the controller IP block to correctly interact with the remaining IP Blocks of the SOC DUT. As noted the timing of this interaction is non deterministic and is accomplished according to the specifications of the protocol. Referring to Fig. 6, the controller IP block **600** generates the data signals **605a** and **605b**, the command signals (RAS#, CAS#, and WE#) **610**, the select and enable signals **615** and **620**, the clocking signals (CK and CK#) **625**, the address signals, **630**, and the strobe and synchronizing signals **635a** and **635b** as defined in the DDR3 SDRAM Standard.

[0065] The protocol aware controller of various embodiments receives the signals, decodes the action, execute

the commands to perform the requested action. The protocol controller then times and synchronizes the test stimulus signals that simulate the DDR3 SDRAM responses so that they arrive at the SOC DUT with a consistent Clock Latency (CL). The non-
5 operational (NOP) cycles need to be captured and compared. The stripping out NOP cycles reduces the data set size used by the automated test equipment system of the various embodiments and is one of the immediate benefits of the protocol aware controller within the automated test equipment system of the
10 various embodiments.

[0066] As can be seen from this example, the DDR3 SDRAM protocol includes a total of 26 Address/Command/Clocking pins (**610**, **615**, **620**, **625**, and **630**) and another 22 Data/Mask/Strobe pins (**605a**, **605b**, **635a**, and **635b**) that are to be observed. A
15 total of 48 channels are employed within the automated test equipment system of this embodiment to simulate the DDR3 SDRAM function. If each of the protocol aware controllers controls a total of eight channels, with at least six of the protocol aware controllers cooperatively linked to simulate the DDR3 SDRAM to
20 test the functional operation of the controller IP block **600**.

[0067] Refer now to Fig. 7 for a description of the channel structure of the automated test equipment system **700**. The automated test equipment system **700** has a number of channel boards **705a** and **705b** (2 in this example). Each of the channel
25 boards **705a** and **705b** has a number (5 in this example) of protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j**. Each of the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** is capable of decoding, controlling, and synchronizing a number of input and output signals, in this example eight (8).
30 The channel layout for the automated test equipment system **700** is designed to accommodate the protocol of the DDR3 SDRAM from

the DDR3 SDRAM controller IP block **600**. Certain restrictions for the protocol is observed for these channels of the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** that are related to tracking. The DDR3 SDRAM timing is specified relative to either the timing clocks (CK) or the data strobes (DQS), the tracking function of the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** are employed to ensure that the appropriate timing and synchronization criteria is met. The Address/Command channels **740**, **745**, **750**, and **755** will follow the clocking channel **740** and the Data and Mask channels **725**, **730**, and **735** will follow their respective data strobe pins **725** and **730**.

[0068] Since the results of the decoded address, command, control, timing, and data signals of a protocol are communicated between the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j**, the tracking signals **720** and command signals **715** are connected to transfer the necessary tracking signals between the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j**. In the case of the DDR3 SDRAM protocol, the clock timing and command signals **740** and the data strobe (DQS) **725** and **730** are tracked and transferred to the other protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j**.

[0069] It should be noted that in most cases all or most of the channels (8) of the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** are used, but in two of the cases, the channels are only partially used (7). This is because the tracking function is split on even channel boundaries for the case of tracking a differential signal such as the clock timing (CK) and the data strobe (DQS) signals that are both differential signals. In each case, the channel boards **705a** and **705b** are

designed such that the tracked signal is the first in a tracking chain followed by the dependent signals.

[0070] It should further be noted that the DDR3 SDRAM protocol spans more than the number of protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** that populate the channel boards **705a** and **705b**. The tracking and command signals propagate from one channel board **705a** and **705b** to the other channel boards **705a** and **705b**. Backplane interface board signals exist in automated test equipment systems **700** to allow for this propagation.

[0071] One of the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** is designated as the control protocol specific circuit **710d**. The control protocol specific circuit **710d** receives the various timing and command signals (CK, CS, CAS, RAS, WE) **740** for the DDR3 SDRAM protocol. Because of the necessity for decoding the timing and command signals (CK, CS, CAS, RAS, WE) **740** appropriately and expeditiously, the timing and command signals (CK, CS, CAS, RAS, WE) **740** for any protocol are not split between the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j**.

[0072] Three protocol specific circuits **710f**, **710g**, and **710h** are not used for this implementation of the DDR3 SDRAM protocol. The three protocol specific circuits **710f**, **710g**, and **710h** are optionally used to expand the data bus of the DDR3 SDRAM to 32 bits as opposed to the sixteen bits of the example. The three protocol specific circuits **710f**, **710g**, and **710h** alternately are used as regular channels or used for an entirely different protocol for another of the IP blocks of the SOC DUT.

[0073] Refer now to Figs. 8 and 9 for an examination of the timing characteristics of the DDR3 SDRAM Protocol. In Fig. 8 the rising edge **800** of clocking signal (CK) occurs in the

middle of Command/Address signals when their signals are stable and valid. Alternately the rising edge **805** of data strobe signals (DQS) are sent out at the beginning of data signal (DQ) transfer time. A tracker or transition detector (not shown) monitoring the clock signals (CK/CK#) permits the offset of the data strobe (DQS) from the tracker by 90 degrees in order to position the level transition of the data strobe (DQS) in the middle of the clock signal (CK) when the clock signal is not in transition. Additionally on the Address/Command Control protocol specific circuits, the data strobes are activated at the tracker time or alternately offset one complete clock signal (CK) cycle later in order to center the data strobes (DQS) at the center of the eye of the data signals (DQ). This will permit the "shmooing" or varying of the conditions and inputs of the data strobes (DQS) timings to determine the eye width to find the passing regions.

[0074] In the Write Cycle of Fig. 9, when the controller IP block is sourcing data, the position of data strobe (DQS) moves to the center of the data valid time **810**. The tracking of the data strobes (DQS) allows the placement of the position of the data strobes (DQS) at the appropriate times **810** of the data signals (DQ).

[0075] The protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** converts the controller IP block **600** clock phase to the tester clock phase (with the tracker). Some degree of drift between the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** clock and clocking and data strobe signals (CK and DQS) of the controller IP block **600**. This allows generation of the clocks on the channel boards **705a** and **705b** without attempting to use the DDR3 SDRAM controller IP block **600** clock directly. The protocol specific circuits **710a**, ..., **710e**, and

710f, ..., 710j will be clocking data in/out of the protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j at a slower rate (1/4 the DDR3 SDRAM controller IP block 600 clock rate), so at least for the DDR3 SDRAM interface, the protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j clock could be 1/4 the rate of the clock signals (CK) (200MHz max). To match the data rate of the DDR3 SDRAM Standard, the capture memory and the source memories of the protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j may be paralleled FIFO memory that are read or written at the slower rate of the automated test equipment system while allowing the data to be transferred to the controller IP block 600 of the SOC DUT at its operational rate.

[0076] The internal clocking of the protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j have two alternatives. One is to use the automated test equipment system clock to clock protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j. Alternately, the clocking of the SOC DUT may be used for clocking the protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j.

[0077] All DDR3 SDRAM Standard commands are defined by the state of the command signals (CS#, RAS#, CAS#, WE# and CKE) at the rising edge of clock signal (CK). Each unique command is present on any of the clock signal (CK) boundaries 800. There are limitations, however, on allowable command sequences. For example a READ or WRITE with Burst Length 4 cannot be interrupted until complete so that there is at least one NOP or DESELECT between consecutive READ/WRITE commands. A complete table of these constraints can be found in the DDR3 SDRAM Standard. It is optional that violations of these constraints be flagged but there is a subset of violations that will cause the protocol specific circuits 710a, ..., 710e, and 710f, ..., 710j

to operate improperly (READ followed immediately by another READ for example). These will set an error flag and be logged as a fault in the controller IP block **600** of the SOC DUT.

[0078] There are only a limited number of actions the
5 protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** can perform on any given cycle:

1. Store (or compare to expected response) the Address/Command/WR Data into Capture memory;

10 2. Source Read Data from the source memory (READ FIFO); or

3. Do nothing.

[0079] A lookup table is resident in the DRAM of the protocol specific circuits **710a**, ..., **710e**, and **710f**, ..., **710j** for converting the command signal inputs (CS#, RAS#, CAS#, WE# and
15 CKE) into the possible actions.

[0080] Various embodiments of the automated test equipment system will support many different protocols for the different SOC DUT. The correct protocol is configured in the three protocol specific circuits **710a**, ..., **710f**, **710g**, and **710h**
20 when the testing of the SOC DUT is initiated. The protocols generally consist of random access memory interface protocols, communication interface protocols, computing device interface protocols, and diagnostic testing protocols, but other protocols are possible. These protocols may fall into two broad
25 categories. In a first example, the SOC DUT controls the bus (bus master). In a second example, the automated test equipment system controls the bus. The DDR3 SDRAM protocol, in the example above, is an example where the SOC DUT controls the bus and the automated test equipment system responds.

30 [0081] It is significant to note that multiple protocol engines may be implemented in the intellectual protocol blocks

of the SOC DUT. Thus, multiple protocol engines may be running concurrently on the automatic test equipment. For example, there may be a DRAM port, a JTAG port, and a MDIO port protocol engine running concurrently in the automated test equipment.

5 [0082] As described above, in the first example, the SOC device-under-test controls the interface between automated test equipment system and the SOC device-under-test. In the second example, the automated test equipment system controls the interface between the SOC device-under-test and the automated
10 test equipment system. In the first example, the SOC device-under-test communicates the non-deterministic signals and the automated test equipment system responds. In the second example, the automated test equipment system sends the test stimulus signals with the appropriate protocol structure and
15 timing to the SOC device-under-test and the SOC device-under-test responds with the non-deterministic test response signals that are decoded. In either example, the automated test equipment recognizes a non-deterministic response signal from the SOC device-under-test and responds.

20 [0083] It should be understood that the above methods and apparatus may be utilized in the manufacture of a device such as component, board, or consumer electronic good, having a SOC. Thus, after fabricating a SOC, it may be tested by simulating a functional operational environment in a tester by
25 receiving a non-deterministic response signal from the system-on-a-chip, ascertaining an expected stimulus signal to be transferred to the system-on-a-chip from the non-deterministic response signal based on a predetermined protocol, and initiating transmission of the expected stimulus signal to the
30 system-on-a-chip, as described above. The testing may be performed prior to, or after installing the SOC in the device.

[0084] While this invention has been particularly shown and described with reference to the embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

5

WHAT IS CLAIMED IS:

1. A protocol specific circuit for simulating a functional operational environment into which a device-under-test is placed for functional testing, the protocol specific circuit comprising a protocol aware circuit constructed to receive at least one non-deterministic signal communicated by a device-under-test and to control a transfer of at least one test stimulus signal to the device-under-test in response to the at least one non-deterministic signal.

2. The protocol specific circuit of Claim 1, wherein the protocol aware circuit is constructed to control the transfer of the test stimulus signal by selecting a test stimulus signal response based on the non-deterministic signal from the device-under-test and initiating transmission of the selected at least one test stimulus signal.

3. The protocol specific circuit of Claim 1, wherein the protocol specific circuit is constructed to receive the at least one non-deterministic signal communicated by a protocol specific device-under-test via pin electronics and to control transfer of the at least one test stimulus signal from a test signal generator to the device-under-test.

4. The protocol specific circuit of Claim 3, wherein the protocol specific circuit is constructed to store the at least one test stimulus signal from the test signal generator in a stimulus signal storage device.

5. The protocol specific circuit of Claim 4, wherein the

stimulus signal storage device comprises at least one of: a) FIFO memory; or b) random access memory.

6. The protocol specific circuit of Claim 1, wherein the protocol specific circuit is constructed to store the at least
5 one non-deterministic signal in a response signal storage device.

7. The protocol specific circuit of Claim 6, wherein the response signal storage device comprises at least one of: a) FIFO memory; or b) random access memory.

10 8. The protocol specific circuit of Claim 6, wherein the protocol specific circuit is constructed to extract the at least one non-deterministic signal from the response signal storage device for comparison by a failure processor with an expected response signal, and determine an operational condition of the
15 device-under-test.

9. The protocol specific circuit of Claim 1, wherein the protocol specific circuit is constructed for mounting in automated test equipment to allow the automatic test equipment to simulate a functional operational environment into which the
20 device-under-test is placed for functional testing and the protocol aware circuit interprets the at least one non-deterministic signal to determine a synchronization time and a latency time for transmission of the at least one test stimulus signal.

25 10. A protocol specific circuit comprising a configurable protocol aware circuit capable of being preconfigured to communicate at least one test stimulus signal between a test

signal generator and a specific device-under-test via pin electronics in response to a non-deterministic signal from the device-under-test.

11. The protocol specific circuit of Claim 10, wherein the
5 protocol specific circuit is preconfigured to respond to a specific device-under-test in response to the non-deterministic signal comprising an asynchronously occurring signal from the device-under-test.

12. The protocol specific circuit of Claim 10, wherein the
10 protocol specific circuit comprises a protocol decoder.

13. The protocol specific circuit of Claim 10, wherein the protocol specific circuit is programmable.

14. The protocol specific circuit of Claim 13, wherein the
15 protocol specific circuit comprises a field programmable gate array.

15. The protocol specific circuit of Claim 14, wherein the field programmable gate array comprises the protocol aware circuit and a memory device, the protocol aware circuit being coupled to the memory device.

20 16. The protocol specific circuit of Claim 15, wherein the memory device comprises at least one of: a) FIFO memory; or b) random access memory.

17. The protocol specific circuit of Claim 10, wherein the
25 protocol specific circuit comprises a memory buffer configured to store the at least one test stimulus signal generated by the

test signal generator and to provide the stored test stimulus signal via the pin electronics, to the device-under-test in response to a non-deterministic signal from the device-under-test.

5 18. The protocol specific circuit of Claim 17, wherein the memory buffer comprises at least one of: a) FIFO memory; or b) random access memory.

19. The protocol specific circuit of Claim 10, wherein the protocol specific circuit further comprises a pass-through
10 circuit coupled in parallel with the protocol aware for receiving deterministic signals from the device-under-test.

20. Automated test equipment comprising a protocol aware channel for testing a device-under-test, the protocol aware channel comprising a protocol specific circuit coupled between a
15 test signal generator and a pin electronics circuit, the protocol specific circuit being constructed to be capable of being preconfigured to respond to the protocol specific device-under-test in response to a non-deterministic signal from the device-under-test.

20 21. The automated tester of Claim 20, wherein the protocol specific circuit comprises a protocol decoder.

22. The automated tester of Claim 20, wherein the protocol specific circuit comprises a field programmable gate array.

23. The automated tester of Claim 22, wherein the field
25 programmable gate array comprises a protocol aware circuit and a memory device, the protocol aware circuit being coupled to the

memory device.

24. The automated tester of Claim 20, wherein the protocol specific circuit comprises a memory buffer configured to store the at least one test stimulus signal generated by the test
5 signal generator and to provide the stored test stimulus signal via the pin electronics, to the device-under-test in response to a non-deterministic signal from the device-under-test.

25. The automated tester of Claim 20, wherein the protocol specific circuit further comprises a pass-through circuit
10 coupled in parallel with a protocol aware circuit for receiving deterministic signals from the device-under-test.