

PATENT SPECIFICATION

1,097,413

DRAWINGS ATTACHED.

Date of Application and filing Complete Specification:

Jan. 19, 1965.

No. 2357/65.

Application made in United States of America (No. 341,558) on
Jan. 31, 1964.

Complete Specification Published: Jan. 3, 1968.

© Crown Copyright 1968.

Index at Acceptance:—H1 K(1C1, 1CX, 2S1B, 2S2P, 2S20, 3E1M, 4C9A, 4C11, 4C21, 4C23,
4F1A, 4F7, 4F8, 4F11G, 4F17, 4F18, 4GX, 5C5).

Int. Cl.:—H 01 I 1/14.

COMPLETE SPECIFICATION.

Improved Semiconductor Devices.

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and has particular application to transistor devices which are adapted to handle high power at high frequencies.

According to one aspect, the present invention provides a semiconductor device comprising a semiconductor body having a p-n junction in which a distributed resistive layer is positioned between a contact and the p or n region and is such as to maintain the current density across the junction substantially uniform.

According to another aspect, the present invention provides a transistor device including a collector region of one conductivity type, a base region of opposite conductivity type and an emitter region of conductivity type opposite to that of said base region defining p-n junction between said regions, a conducting emitter contact spaced from said emitter region, a lead connected to said emitter contact for conducting current to said emitter region, and a distributed resistive layer positioned between said lead and said emitter region, such as to maintain the current density across the emitter junction substantially uniform, wherein a portion of the resistive layer extends over said emitter contact so that the emitter current passes inwardly from the emitter contact through the resistive layer to the emitter region. The distributed resistive means is so positioned that

the current density remains substantially equal at high emitter current densities in incremental areas across the emitter junction. The distributed resistive means may be in the form of a thin layer of metal or of semiconductor material having a high sheet resistance.

The distributed resistive means essentially provides a distributed ballast resistor in series with each incremental area of the emitter junction. The ballast resistor limits the current density in the incremental areas of the emitter junction to a value close to that of the other incremental areas. Thus, the current-voltage threshold for breakdown is increased, for a particular device geometry, thereby imparting to the device a higher power handling capability. Alternatively, smaller sized units may be made for a like power rating since essentially all of the emitter area (not just the periphery) is carrying current to the same degree. Alternatively again, a combination of increased threshold for breakdown and smaller units may be provided.

A more detailed description of the invention follows in conjunction with the accompanying drawings, in which:

Figure 1 is a sectional view of a first embodiment of the invention in which the resistive means is in the form of a discrete, epitaxially-grown layer between the emitter region and the emitter contact,

Figure 2 is a sectional view of a second embodiment of the invention in which the resistive means is in the form of a discrete vapour deposited layer between the emitter contact and the emitter bus or lead, and

Figures 3A and 3B are respectively plan and sectional views of a third embodiment of the invention in which the resistive means is in the form of a multiplicity of discrete

[Price 4s. 6d.]

vapour deposited layers between a corresponding multiplicity of discrete emitter regions and the emitter contact.

Similar reference numerals are used for similar elements throughout the several Figures.

Figure 1 illustrates a first embodiment of a transistor of the invention comprising a semiconductor body 21. The body 21 has therein an emitter region 23 of one conductivity type, for example, p type; a base region 25 of the other conductivity type, for example, n type; and a collector region 27 of the one conductivity type, for example, p type. The emitter region 23 and the base region 25 are adjacent to one another and define an emitter p-n junction 29 therebetween. The collector region 27 and the base region 25 are adjacent to one another and define a collector p-n junction 31 therebetween. The emitter junction 29 and the collector junction 31 are preferably uniform and closely spaced from one another by the base region 25. The transistor may be of the p-n-p type or of the n-p-n type and, in general, may be any of the homojunction or heterojunction structures known in the semiconductor art. The collector region 27 is attached to a support 33 as with solder 35. The support 33 may be an electrically conducting metal plate and may be the header of the enclosure for the transistor. Both the support 33 and the solder 35 are selected to provide a heat-sink for conducting away heat generated in the transistor, in a manner known in the art. In Figure 1, the support 33 functions as the contact to the collector region 27. If desired, a separate collector contact to the collector region 27 may be provided. In that case, the support 33 may be electrically insulating.

A base contact 37 and a base lead 39 are connected in series to the base region 25 in a manner known in the transistor art. An emitter contact 41 and an emitter lead 43 are connected in series with one another in a manner known in the transistor art. However, unlike prior devices, the emitter contact 41 is spaced from the emitter region 23 by a thin distributed resistive layer 45. As shown in Figure 1, the resistive layer 45 is a semiconductor material which has been deposited epitaxially on the surface of the emitter region 23 by processes known in the art. However, other methods of forming said region also may be used, such as out-diffusion, vapour deposition, or recrystallization.

The resistivity and thickness of the resistive layer 45 is such that a voltage drop of at least kT/q volts, and preferably a few times kT/q volts is created at a normal operating current density. In the expression kT/q , k is Boltzman's constant, T is the absolute temperature of the layer during the operation of the transistor, and q is the electrostatic charge on an electron. For a typical transistor in

which the normal operating current density is 1000 amperes/cm², a typical value for the resistance (measured across the thickness of the layer) of one square centimeter of the layer is 10^{-4} ohms. A resistive layer 45 of 0.03 ohm-cm material approximately 30 microns thick may be appropriate in this typical transistor, giving a sheet resistance in the resistive layer 45 of approximately 10 ohms/square. The sheet resistance of the emitter region 23 should be approximately the same value or higher to prevent excessive lateral current flow in the emitter region.

The thin distributed resistive layer 45 acts as a multiplicity of small ballast resistors which tends to keep the current density through the thickness of the resistive layer 45 substantially equal across its major dimensions. The sheet resistance (resistance in the direction of the major dimensions of the resistive layer 45) should be high enough to prevent any substantial lateral current flow (current flow in the direction of the major dimensions of the resistive layer 45).

The emitter contact 41 need not cover all of the emitter region 23 and there is considerable flexibility in designing the emitter contact 41. Where there is an emitter contact 41 which covers substantially all the emitter region 23, as in the transistor illustrated in Figure 1, it is preferred that the resistive layer 45 have a high sheet resistance and that the emitter region 23 have a sheet resistance of about the same value or higher. Where the emitter contact 41 does not cover a substantial portion of the emitter region, it is preferred that the resistive layer 45 has a low sheet resistance and that the emitter junction 29 be divided into discrete sub-areas or islands, as in the transistors illustrated in Figures 2 and 3A. Dividing the emitter junction 23 effectively increases the sheet resistance of the emitter region 23 and it also increases the emitter perimeter to emitter area ratio, a desirable feature for silicon transistors.

The metal layer 42 (Figure 2) is positioned in contact with and between the emitter region 23 and the resistive layer 45. The resistive layer 45 is located between a pair of emitter contacts 41. Thus, the emitter current passes inwardly from the emitter contacts 41 through the resistive layer 45 where it is distributed and passes through the metal layer 42 to the emitter 23. In this embodiment, the metal contact 42 and the emitter region 23 each should have a high sheet resistance to minimize lateral current flow; that is, the conduction of current parallel to the major surfaces of the contact. The metal layer 42 is optional and may be present to provide a non-rectifying or ohmic contact to the emitter region 23.

In Figure 2, base contacts 37 are metallized areas which rest on the base region 25. An insulator layer 47 overlays the base contacts

37 and marginal portions of the emitter region 23. The emitter contacts 41 are metallized areas which rest on the surface of the insulator layer 47. A resistive layer 45 of, for example, partially reduced tin oxide, overlays the metal layer 42, the emitter contacts 41 and the insulator layer 47. The resistive layer 45 has a sheet resistance of approximately 1 ohm/square. This can be achieved with a layer of partially reduced tin oxide, approximately 1 mil thick. Films of resistive metals or other resistive materials can also be used for the layer 45.

The transistor illustrated in Figure 2 may be made using conventional fabrication techniques. One technique will now be described for preparing a transistor having finger-like emitter regions 23, interdigitated with finger-like base contacts 37, and having the cross section illustrated in Figure 2 through each finger-like emitter region. Start with a wafer of n-type silicon approximately 45 mils square and .6 mils thick and having a resistivity of approximately 1 ohm-cm. Mask one major surface of the wafer and then heat the wafer and mask at approximately 1000° C. for approximately 25 minutes in an ambient of nitrogen containing a boron compound, such as boron oxide (B_2O_3) vapour. A boron-diffused p-type region 25 is formed in a surface region of the wafer separated by a p-n junction 31 from the undiffused n-type region 27, which is to be the collector region 27.

The external surface of the boron-diffused region 25 is etched to remove disturbed portions and then masked, leaving exposed finger-like areas approximately 4 mils wide and 20 mils long which are connected to one another at one end, and which define the extent of the emitter region 23 in the finished device. The masked wafer is reheated at approximately 1200° C. for approximately 5 minutes in a nitrogen atmosphere containing phosphorus pentoxide (P_2O_5). Portions of the p type region 25 are converted to n type by the diffusion therein of phosphorus, thereby forming an emitter region 23, and an emitter p-n junction 29 between the emitter region 23 and the base region 25. The mask on the boron-diffused region 25 is removed and the surface is etched to remove disturbed portions. A mask is now applied to the boron-diffused side of the wafer and the base contacts 37 are produced by evaporating aluminium metal thereon to a thickness of approximately 0.5 mil. Another mask is now substituted and the metal layer 42 is produced by evaporating gold metal thereon to a thickness of approximately 0.5 micron. The metal layer 42 is thin and has a high sheet resistance, for example 10 ohms/square, to reduce current conduction in the direction of the major surfaces. The metal layer 42 is used to make ohmic contact to the emitter

region 23. Where it is not necessary to make ohmic contact, the metal layer 42 may be omitted; for example, as illustrated in Figures 3A and 3B.

Next, the metal layer 42 is masked and the entire surface is coated with an insulator layer 47 and the mask removed. The insulator 47 may be of any convenient insulator material. One suitable material is silicon oxide of the type which is produced by thermal deposition from the vapour of a silicon compound.

Then, the insulator layer 47 and the metal layer 42 are masked and the emitter contacts 41 are produced by evaporating a relatively thick layer of metal, such as aluminium, on the insulator layer 47. The emitter contacts 41 are in the shape of stripes and extend parallel to and along both sides of the emitter region 23. The emitter contact mask is then removed.

Then, the exposed surface of the emitter contacts 41, the metal layers 42, and the insulator layer 47 are coated with a resistive layer 45. The resistive layer 45 is of a metal or alloy, such as nichrome, or may be of a compound, such as partially reduced tin oxide. Metals, alloys, and some chemical compounds may be evaporated and condensed in place as a layer monitored to provide the desired thickness. Other chemical compounds may be produced by reaction or decomposition of reagents in the vapour phase and the reaction product deposited in a layer of the desired thickness. As pointed out above, the desired thickness is such that, at the rated current (amperes per cm) of the device, the current density through the junction is substantially equal across the area of the emitter junction, and the voltage drop between the emitter lead and the emitter region 23 is a few times kT/q volts. The finished transistor is then soldered to a header or other support as with solder 35.

Figures 3A and 3B illustrate a transistor of the invention comprising a semiconductor wafer 21 having therein an n-type collector region 27, a p-type base region 25, an n-type emitter region 23 divided into a plurality of discrete sub-areas or islands, a corresponding plurality of separate portions of the emitter junction 29, and a single collector junction 31. This portion of the transistor may be produced by a masking and diffusion technique known in the art. In a particular embodiment the wafer is of elemental silicon and is 225 mils long by approximately 150 mils wide by approximately 10 mils thick, and includes 88 separate rectangular islands constituting the emitter region 23. Each island is approximately 4 mils wide by 8 mils long by approximately 1 mil thick. The islands of the emitter region 23 are arranged in eight rows spaced approximately 26 mils centre-to-centre, each row having eleven islands spaced about eight mils centre-to-centre.

The entire upper surface of the wafer 21 is overlaid with an insulating layer 47 of thermally-grown silicon oxide approximately 8000 Å thick, except for the portions
 5 occupied by the base leads 37, the base bus 38 and the emitter region 23. The islands constituting the emitter region 23 are partially overlaid at the edges thereof by the insulating layer 47 so that the emitter junction 29
 10 is covered where it intersects the surface of the wafer 21.

A plurality of base contacts 37 of aluminium in the shape of fingers approximately 4 mils wide and 0.1 mil thick spaces each of the rows. A pair of emitter contacts 41 of
 15 aluminium in the shape of fingers approximately 3 mils wide and 0.1 mil thick overlay the insulator layer 47 on opposite sides of each column. As illustrated, each base contact 37 is spaced approximately 2 mils from one
 20 emitter contact 41 in each adjacent row. All of the base contacts 37 are connected together at one end by a wide base bus 38; and all of the emitter contacts 41 are connected together at one end by an emitter bus 44, so
 25 that the base contacts 37 and the emitter contacts 41 form an interdigitated structure.

A separate resistive layer 45 approximately 5 mils wide and approximately 18 mils long contacts each island of the emitter region 23 and extends over the adjacent insulator layer 47 into contact with the emitter contact 41 on
 30 each side of the island. The resistive layer 45 may be a chromium-gold alloy produced by co-evaporation of chromium metal and gold metal to a thickness monitored to provide the desired sheet resistivity. In this embodiment, it is preferred that each resistive layer 45 have a sheet resistivity of approximately 2 ohms/
 35 square, although useful devices may be prepared with sheet resistivities between 0.1 and 10 ohms/square.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a
 45 semiconductor body having a p-n junction in which a distributed resistive layer is positioned between a contact and the p or n region and is such as to maintain the current density across the junction substantially uniform.

2. A device according to Claim 1, wherein
 50 the device is a transistor having a base region of one conductivity type and an emitter region of the other conductivity type adjacent to the base region and the p-n junction is defined as

an emitter p-n junction and the resistive means are between the emitter contact and essentially all of the emitter region.

3. A device according to Claim 2, further including a collector region of said other conductivity type adjacent said base region and defining a collector p-n junction therebetween, said emitter p-n junction and said collector p-n junction being in substantially parallel spaced positions with respect to one another.

4. A device according to Claim 2 or Claim 3, wherein at least a portion of the resistive layer extends over the emitter contact.

5. A transistor device including a collector region of one conductivity type, a base region of opposite conductivity type and an emitter region of conductivity type opposite to that of said base region defining p-n junctions between said regions, a conducting emitter contact spaced from said emitter region, a lead connected to said emitter contact for conducting current to said emitter region, and a distributed resistive layer positioned between said lead and said emitter region, such as to maintain the current density across the emitter junction substantially uniform, wherein a portion of the resistive layer extends over said emitter contact so that the emitter current passes inwardly from the emitter contact through the resistive layer to the emitter region.

6. A device according to Claim 4 or Claim 5, wherein the resistive layer is located between a pair of said emitter contacts.

7. A device according to Claim 4 or Claim 5, wherein the emitter region is divided into a plurality of discrete sub-areas.

8. A device according to any one of the preceding claims, wherein the resistive layer consists of semiconductor material or a metal.

9. A device according to any one of the preceding claims, wherein the resistive layer has a high sheet resistance.

10. A semiconductor device as herein described with reference to Figure 1, or Figure 2, or Figures 3A and 3B of the accompanying drawings.

A. M. & W. M. CLARK,
 Chartered Patent Agents,
 5 Stone Buildings,
 Lincoln's Inn,
 London, W.C.2.

The entire upper surface of the wafer 21 is overlaid with an insulating layer 47 of thermally-grown silicon oxide approximately 8000 Å thick, except for the portions occupied by the base leads 37, the base bus 38 and the emitter region 23. The islands constituting the emitter region 23 are partially overlaid at the edges thereof by the insulating layer 47 so that the emitter junction 29 is covered where it intersects the surface of the wafer 21.

A plurality of base contacts 37 of aluminium in the shape of fingers approximately 4 mils wide and 0.1 mil thick spaces each of the rows. A pair of emitter contacts 41 of aluminium in the shape of fingers approximately 3 mils wide and 0.1 mil thick overlay the insulator layer 47 on opposite sides of each column. As illustrated, each base contact 37 is spaced approximately 2 mils from one emitter contact 41 in each adjacent row. All of the base contacts 37 are connected together at one end by a wide base bus 38; and all of the emitter contacts 41 are connected together at one end by an emitter bus 44, so that the base contacts 37 and the emitter contacts 41 form an interdigitated structure.

A separate resistive layer 45 approximately 5 mils wide and approximately 18 mils long contacts each island of the emitter region 23 and extends over the adjacent insulator layer 47 into contact with the emitter contact 41 on each side of the island. The resistive layer 45 may be a chromium-gold alloy produced by co-evaporation of chromium metal and gold metal to a thickness monitored to provide the desired sheet resistivity. In this embodiment, it is preferred that each resistive layer 45 have a sheet resistivity of approximately 2 ohms/square, although useful devices may be prepared with sheet resistivities between 0.1 and 10 ohms/square.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body having a p-n junction in which a distributed resistive layer is positioned between a contact and the p or n region and is such as to maintain the current density across the junction substantially uniform.

2. A device according to Claim 1, wherein the device is a transistor having a base region of one conductivity type and an emitter region of the other conductivity type adjacent to the base region and the p-n junction is defined as

an emitter p-n junction and the resistive means are between the emitter contact and essentially all of the emitter region.

3. A device according to Claim 2, further including a collector region of said other conductivity type adjacent said base region and defining a collector p-n junction therebetween, said emitter p-n junction and said collector p-n junction being in substantially parallel spaced positions with respect to one another.

4. A device according to Claim 2 or Claim 3, wherein at least a portion of the resistive layer extends over the emitter contact.

5. A transistor device including a collector region of one conductivity type, a base region of opposite conductivity type and an emitter region of conductivity type opposite to that of said base region defining p-n junctions between said regions, a conducting emitter contact spaced from said emitter region, a lead connected to said emitter contact for conducting current to said emitter region, and a distributed resistive layer positioned between said lead and said emitter region, such as to maintain the current density across the emitter junction substantially uniform, wherein a portion of the resistive layer extends over said emitter contact so that the emitter current passes inwardly from the emitter contact through the resistive layer to the emitter region.

6. A device according to Claim 4 or Claim 5, wherein the resistive layer is located between a pair of said emitter contacts.

7. A device according to Claim 4 or Claim 5, wherein the emitter region is divided into a plurality of discrete sub-areas.

8. A device according to any one of the preceding claims, wherein the resistive layer consists of semiconductor material or a metal.

9. A device according to any one of the preceding claims, wherein the resistive layer has a high sheet resistance.

10. A semiconductor device as herein described with reference to Figure 1, or Figure 2, or Figures 3A and 3B of the accompanying drawings.

A. M. & Wm. CLARK,
Chartered Patent Agents,
5 Stone Buildings,
Lincoln's Inn,
London, W.C.2.

