

FIG. 1 PRIOR ART

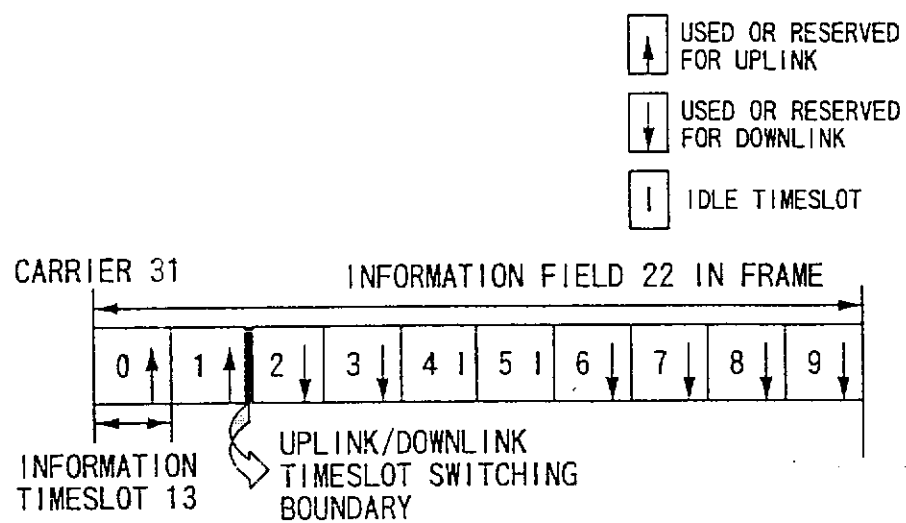


FIG. 2

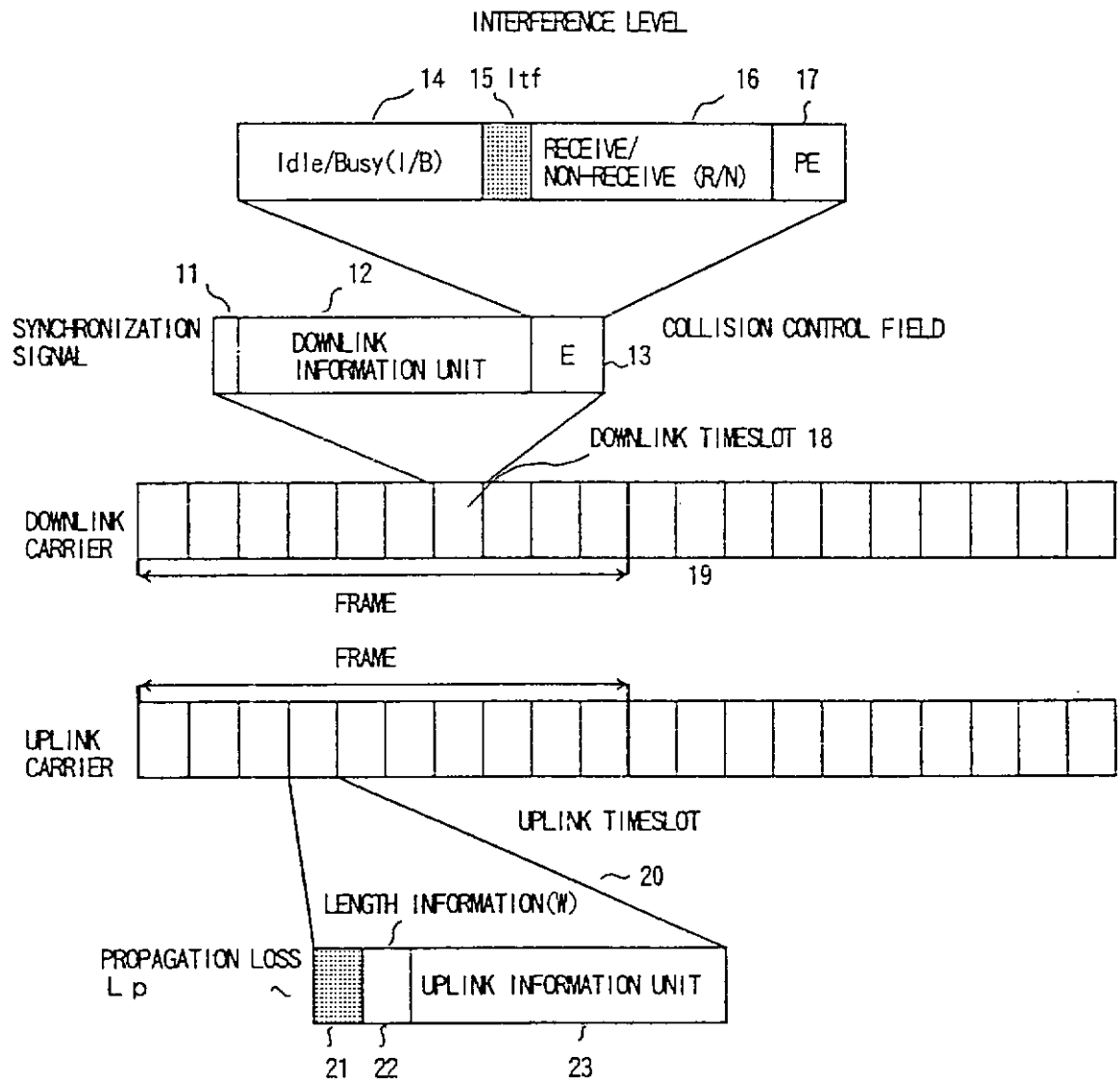


FIG. 3

BIT CONFIGURATION	PROPAGATION LOSS (dB)
0000000	- 1 3 OR LESS
0000001	- 1 2
0000010	- 1 1
⋮	⋮
1111110	1 1 4
1111111	1 1 5

FIG. 4

BIT CONFIGURATION	INTERFERENCE LEVEL (dBm)
00000000	- 2 9 5 OR LESS
00000001	- 2 9 4
00000010	- 2 9 3
⋮	⋮
11111110	- 4 0
11111111	- 3 9

FIG. 5

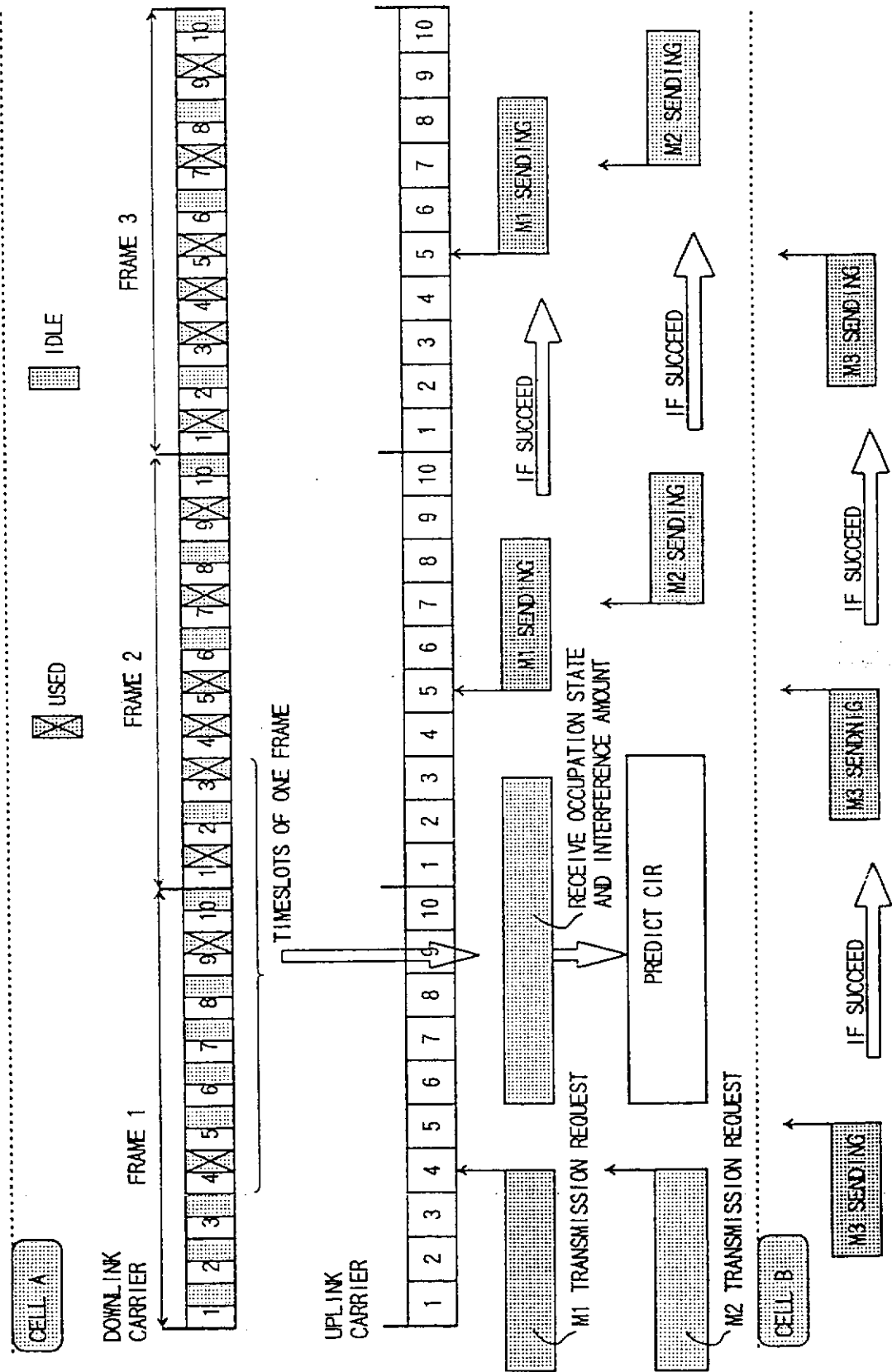


FIG. 6

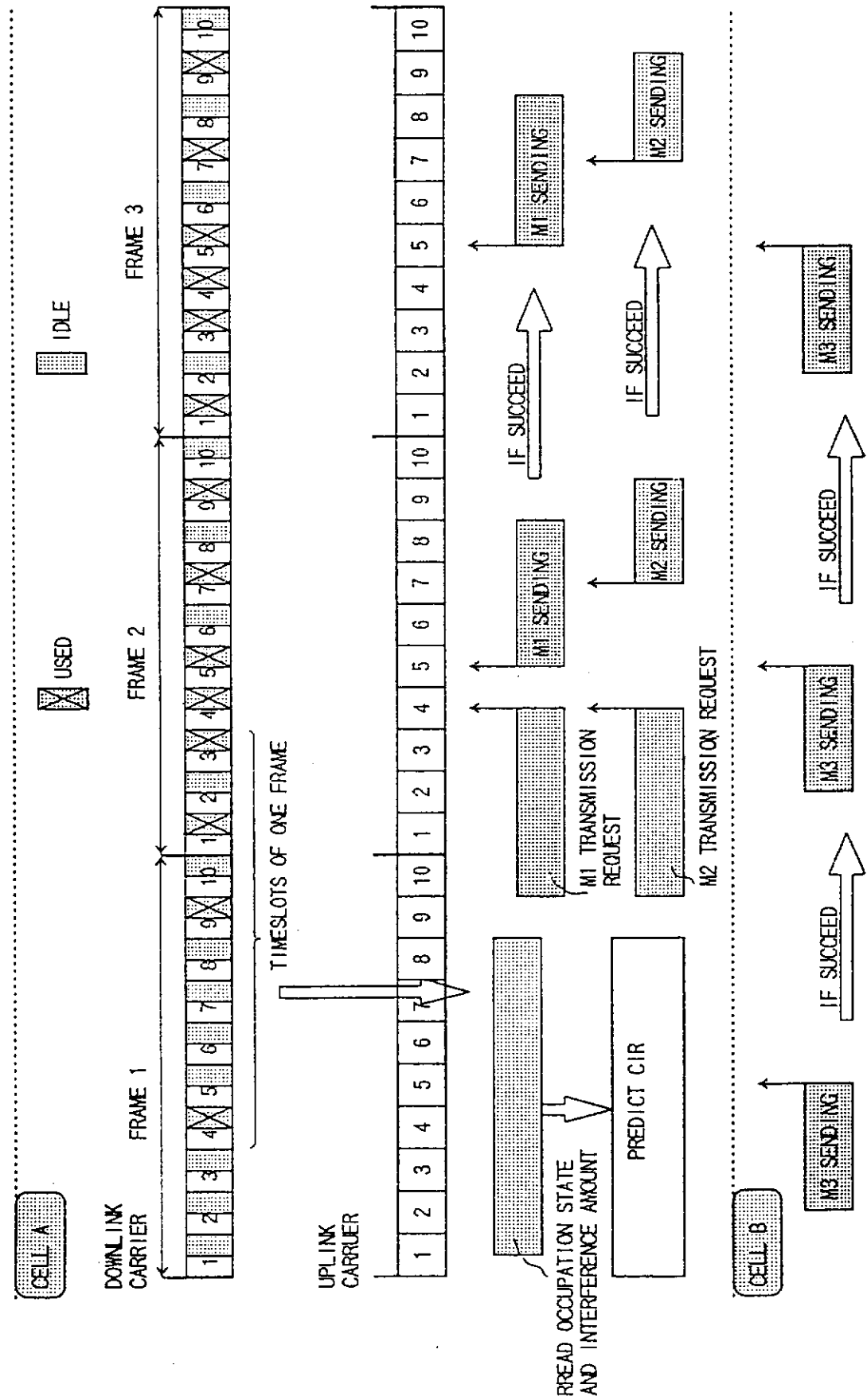


FIG. 7

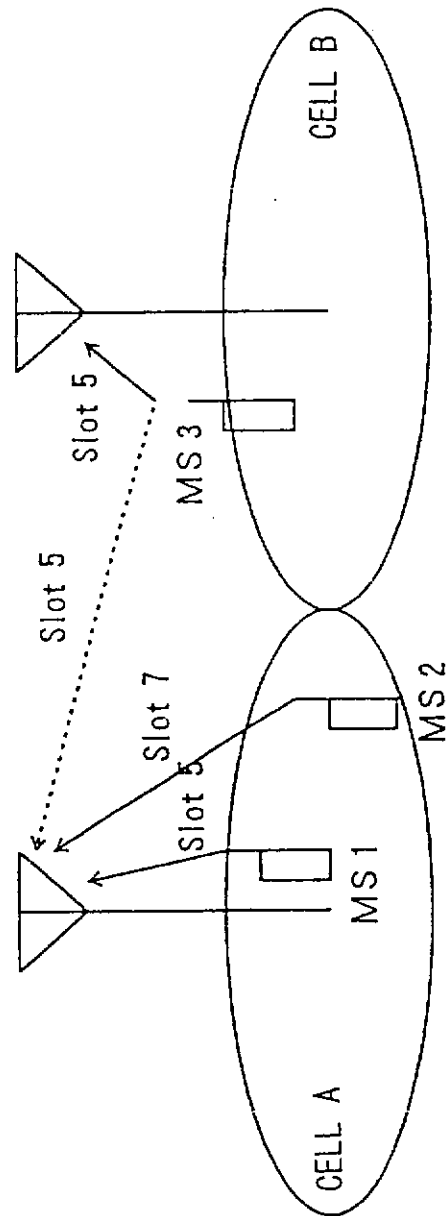
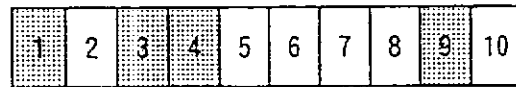


FIG. 8A

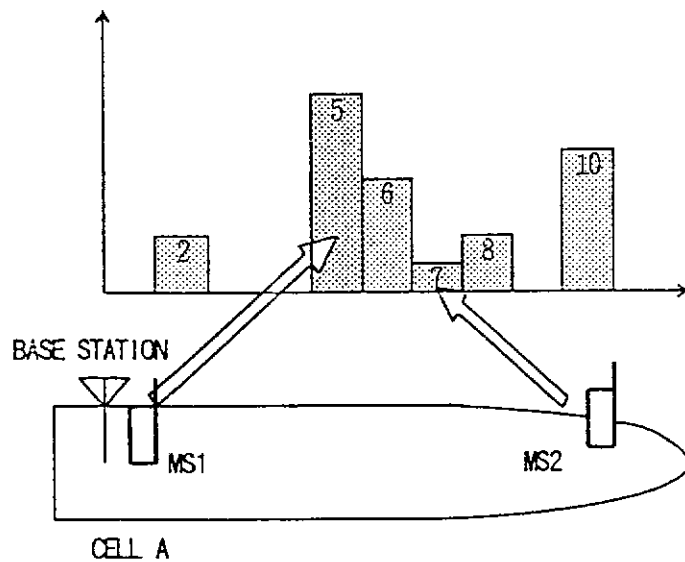


IDLE TIMESLOT



OCCUPIED TIMESLOT

FIG. 8B



SELECT IDLE SLOT SUCH THAT
PREDICTED CIR BECOMES SMALLEST
WHILE SATISFYING REQUIRED CIR

MS1: SMALL PROPAGATION LOSS →
SELECT TIMESLOT OF LARGE
INTERFERENCE

MS2: LARGE PROPAGATION LOSS →
SELECT TIMESLOT OF SMALL
INTERFERENCE

FIG. 9

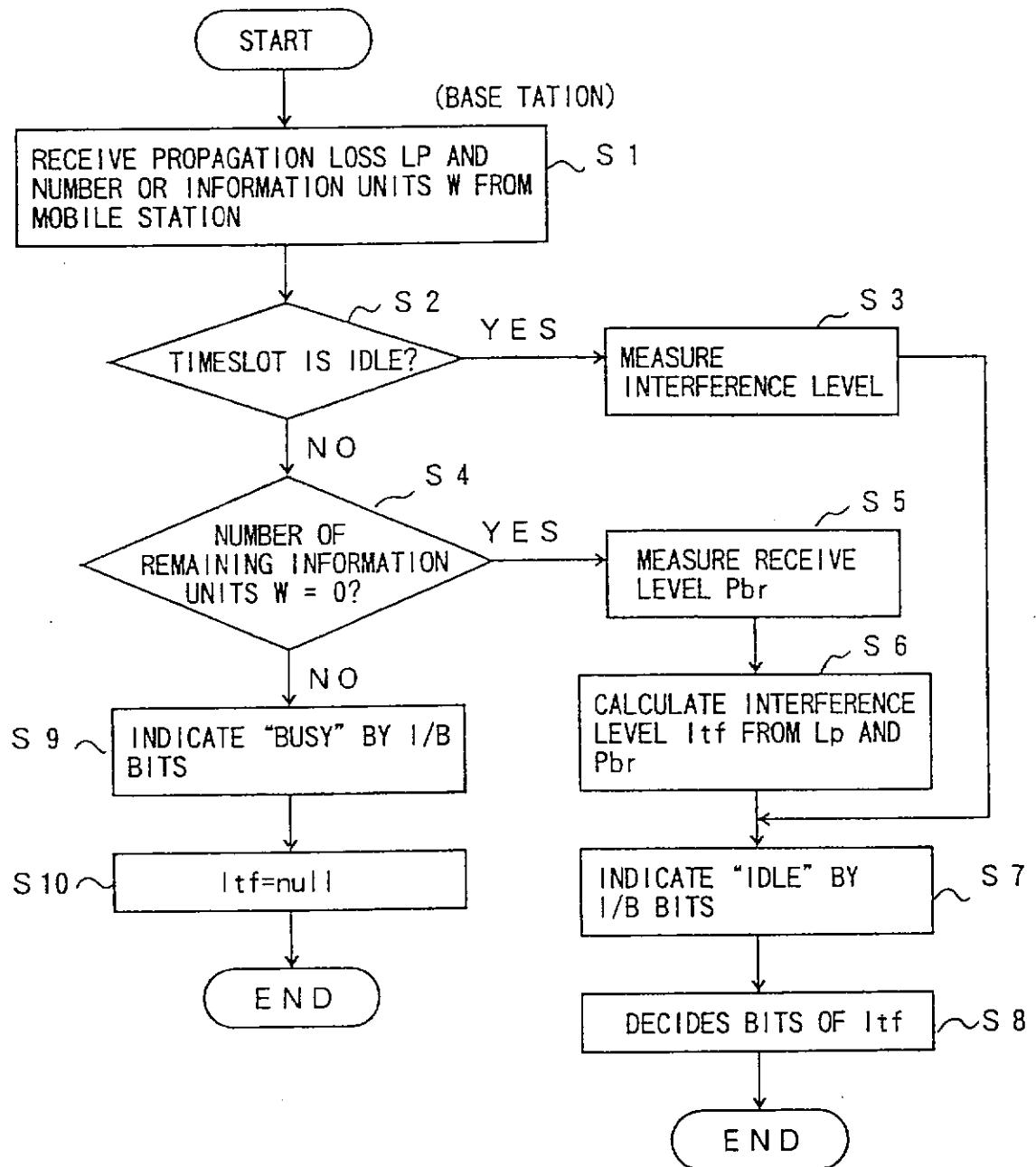


FIG. 10

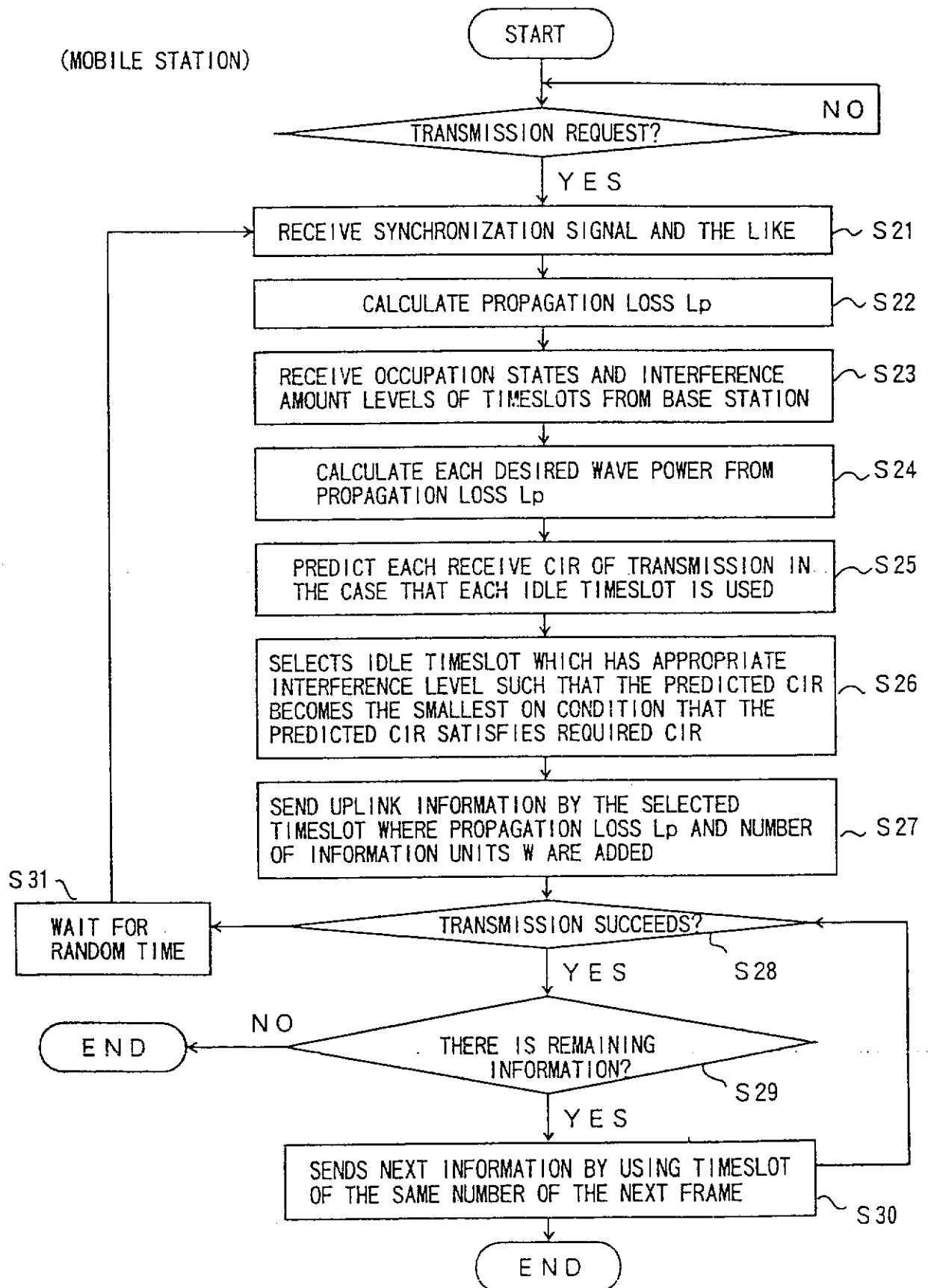


FIG. 11

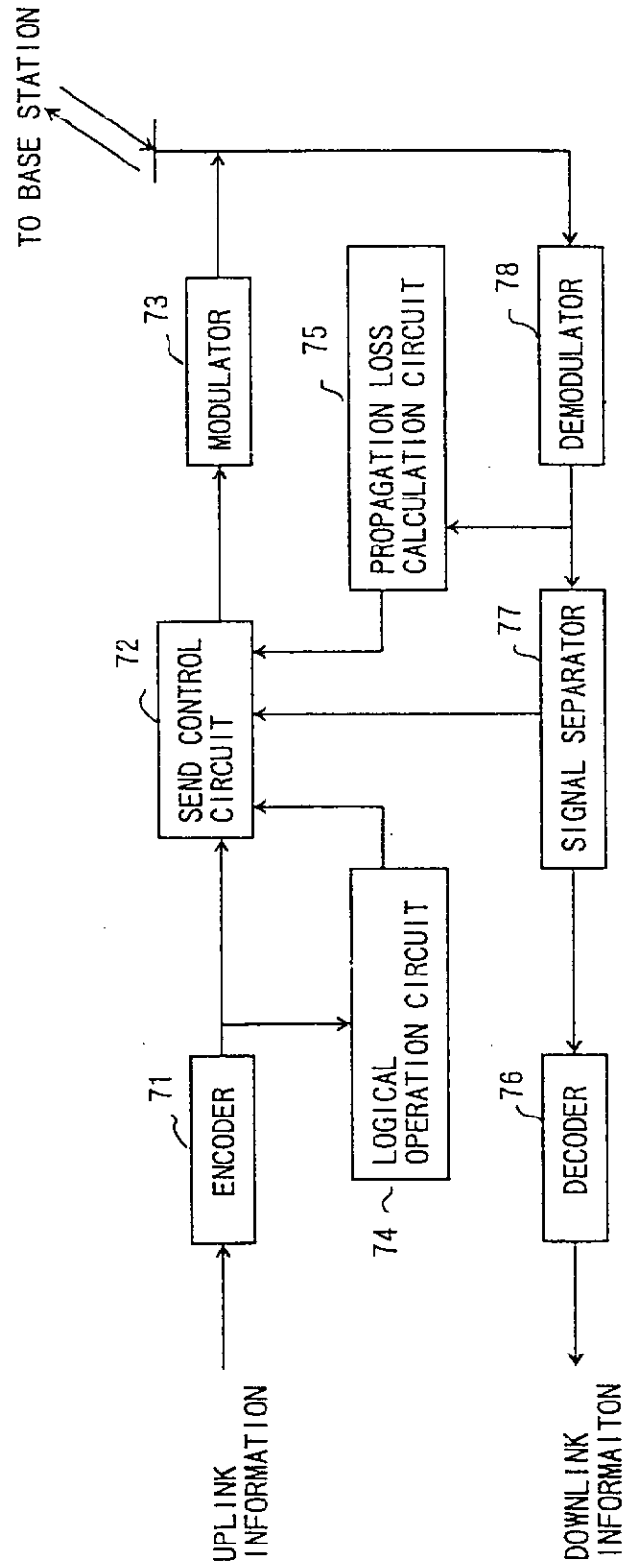


FIG. 12

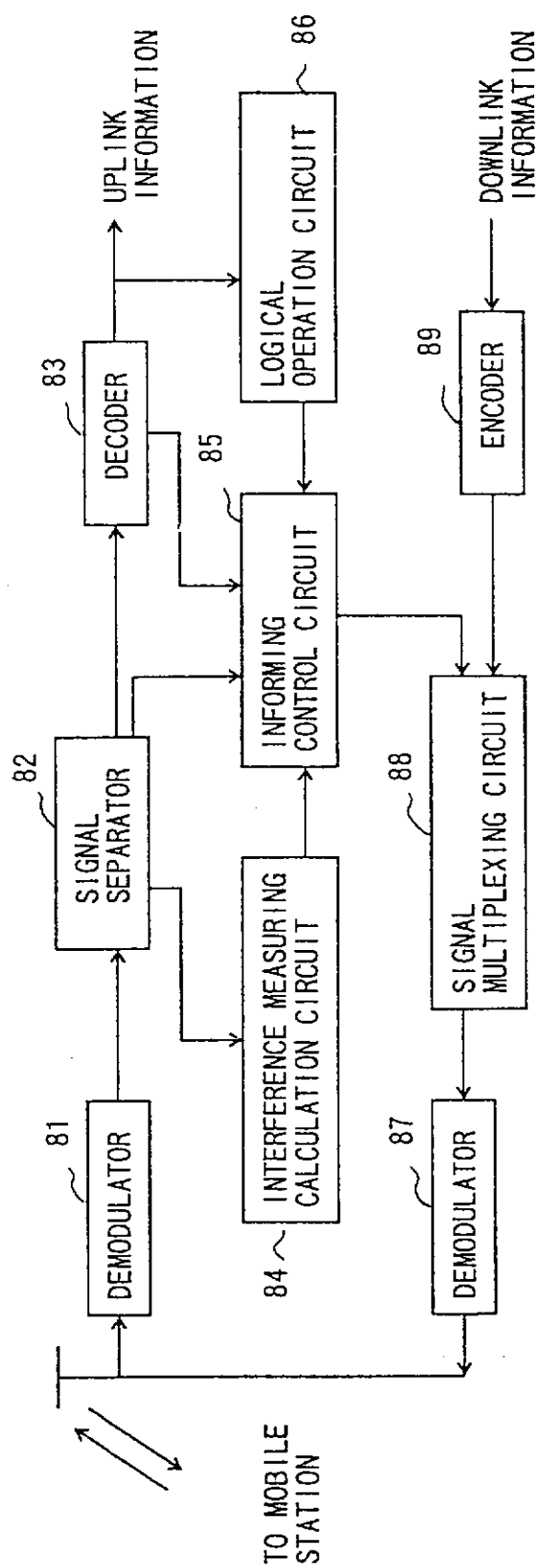


FIG. 13

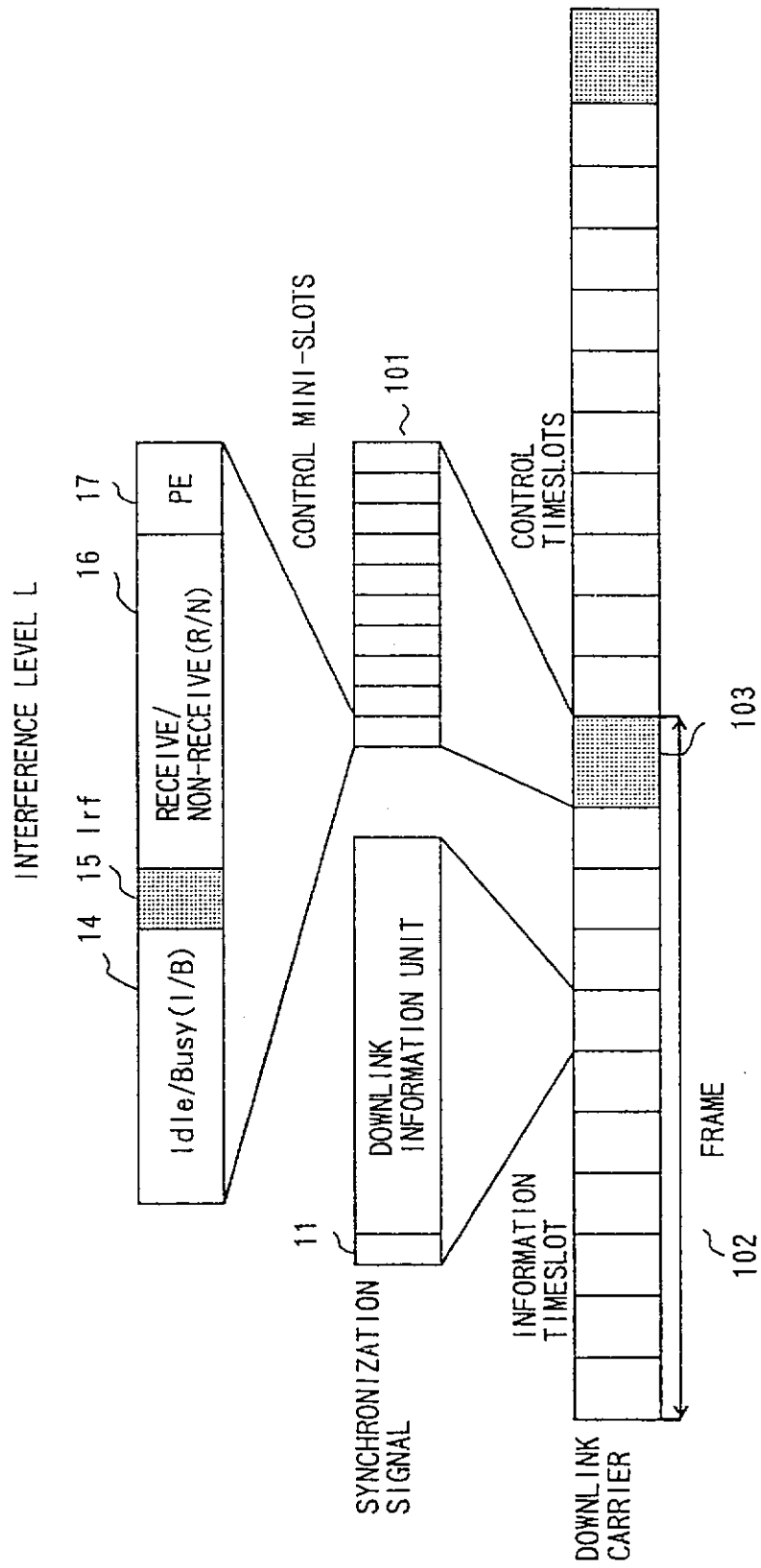


FIG. 14A

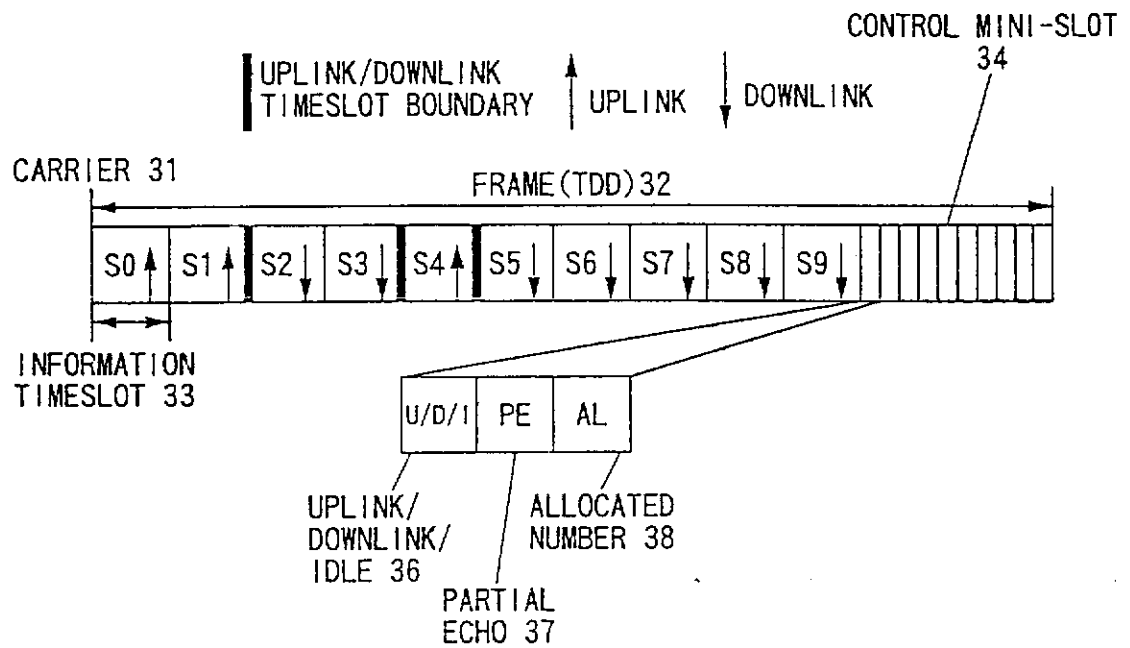


FIG. 14B

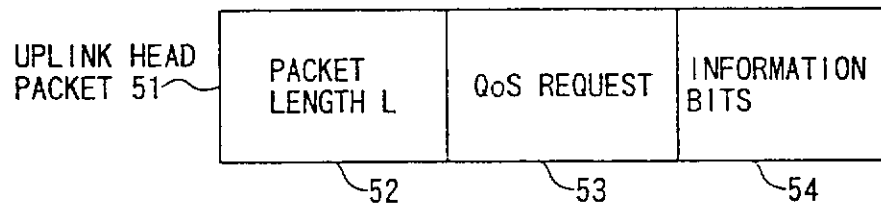


FIG. 15

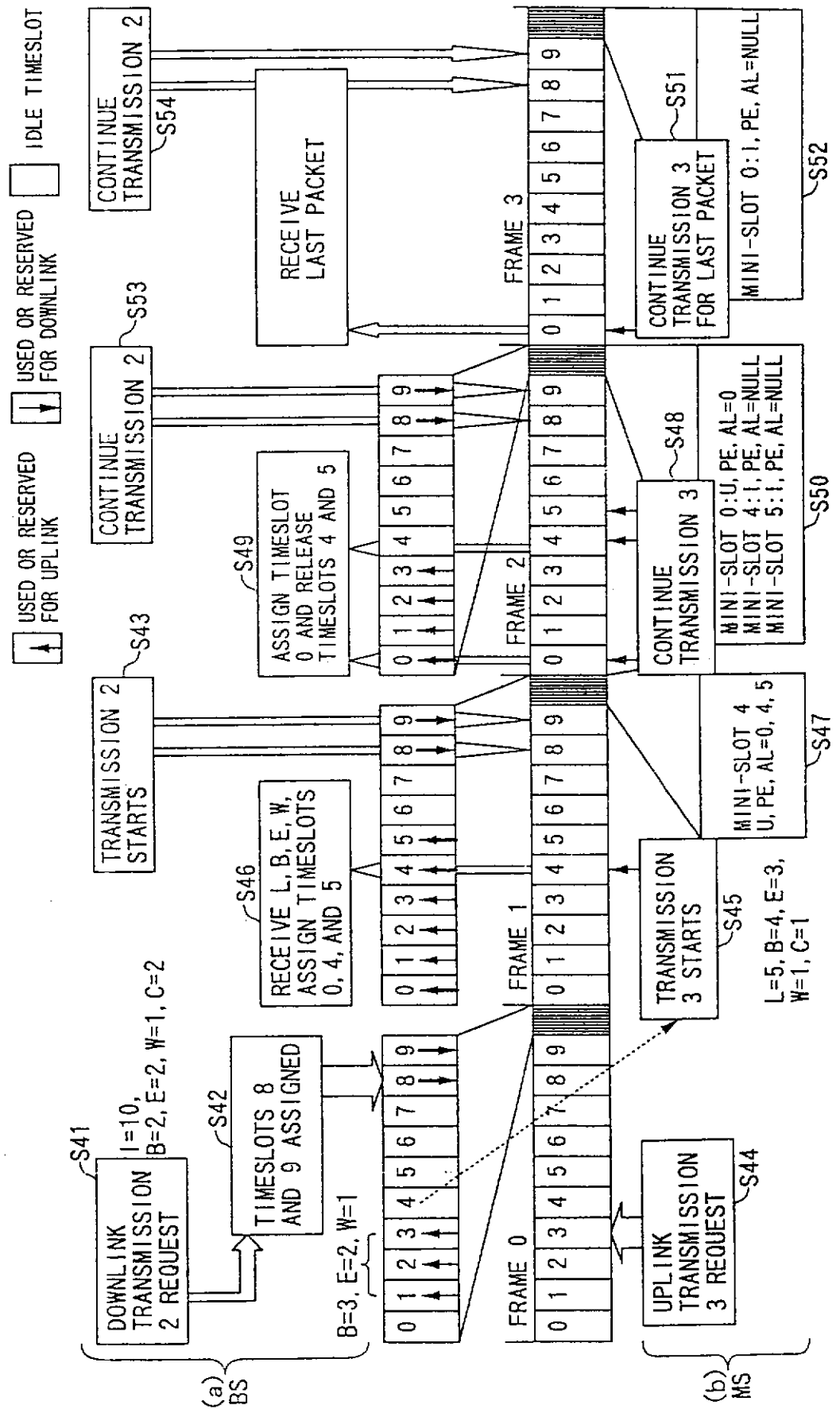


FIG. 16

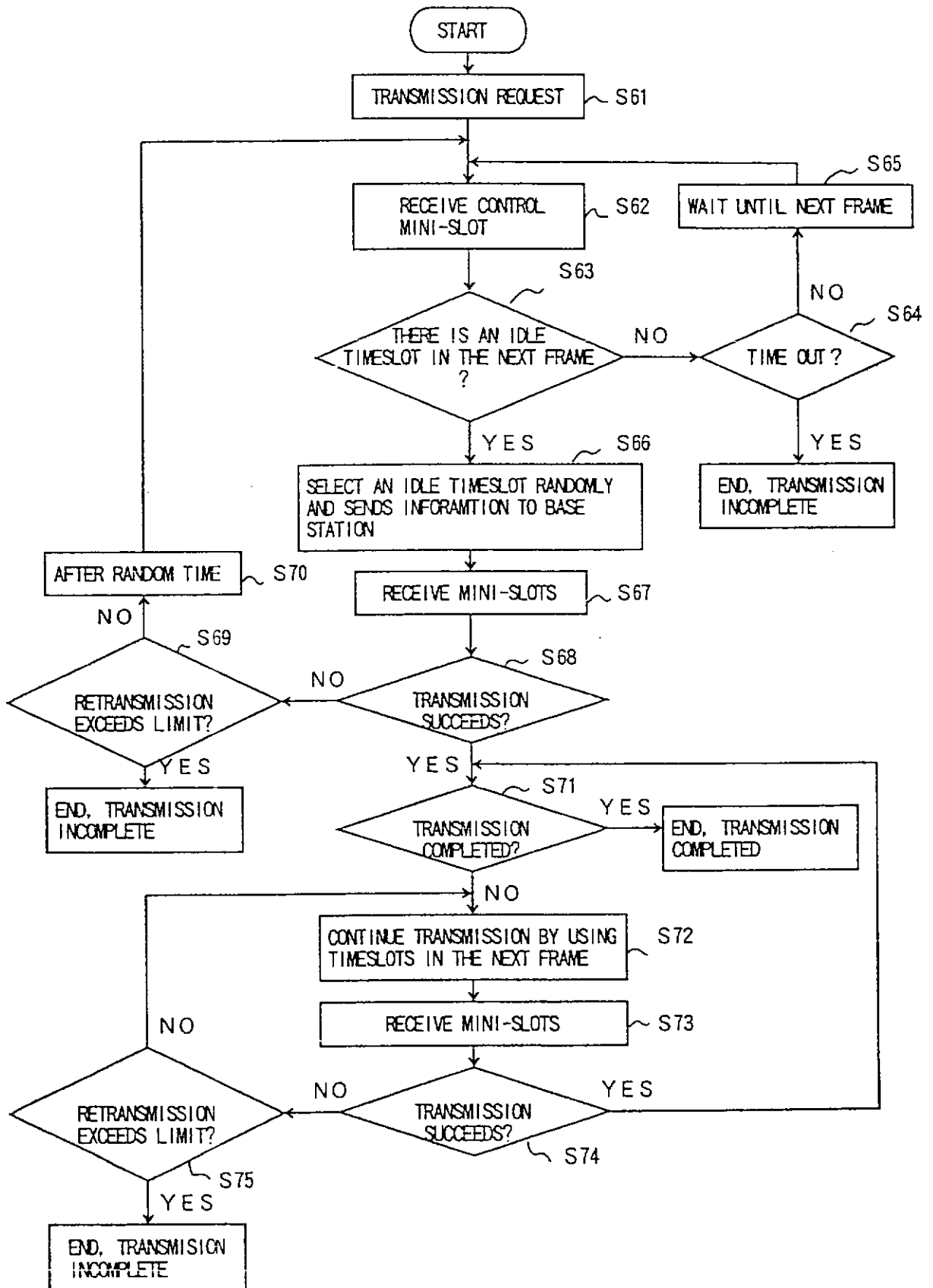


FIG. 17

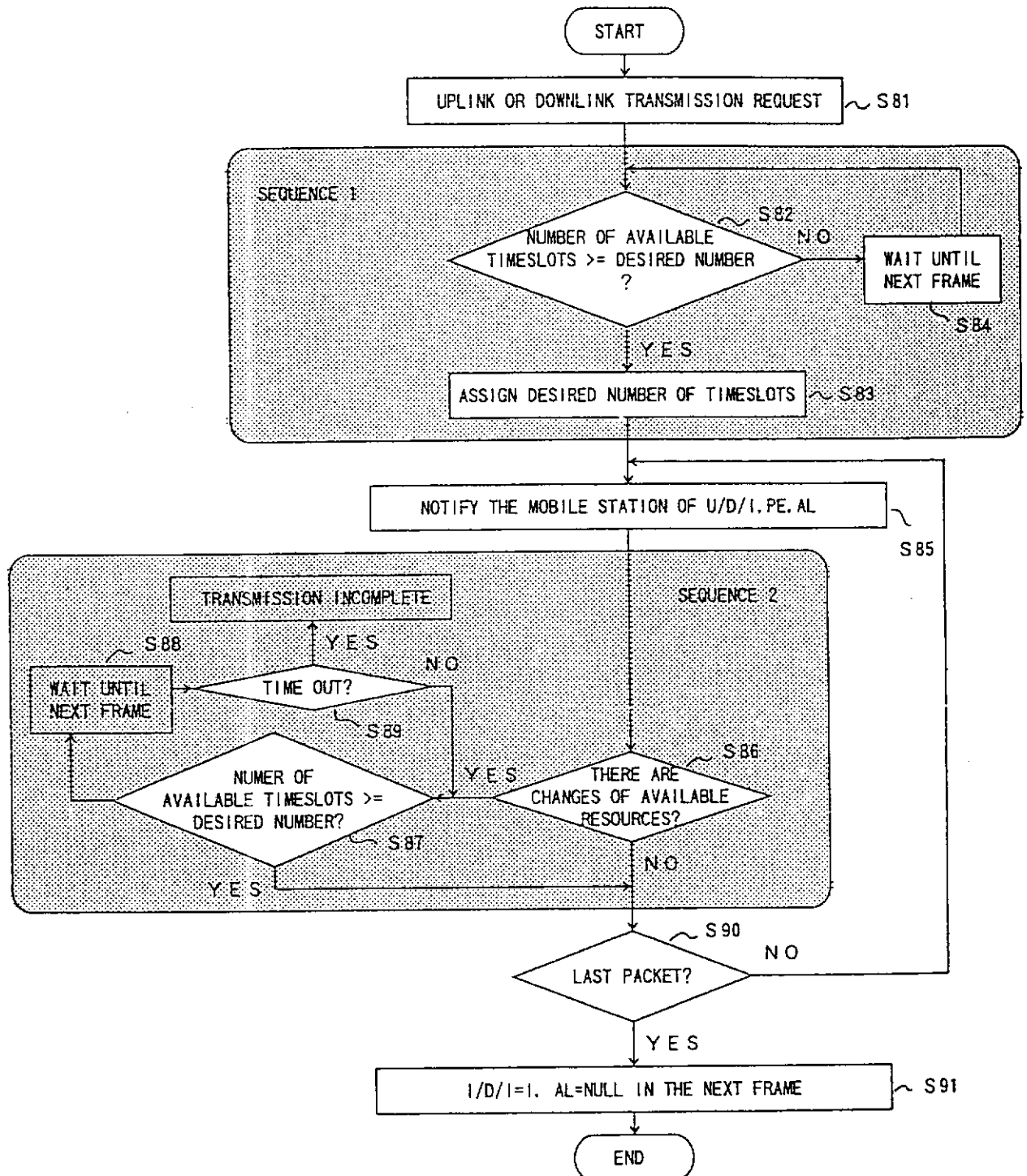


FIG. 18

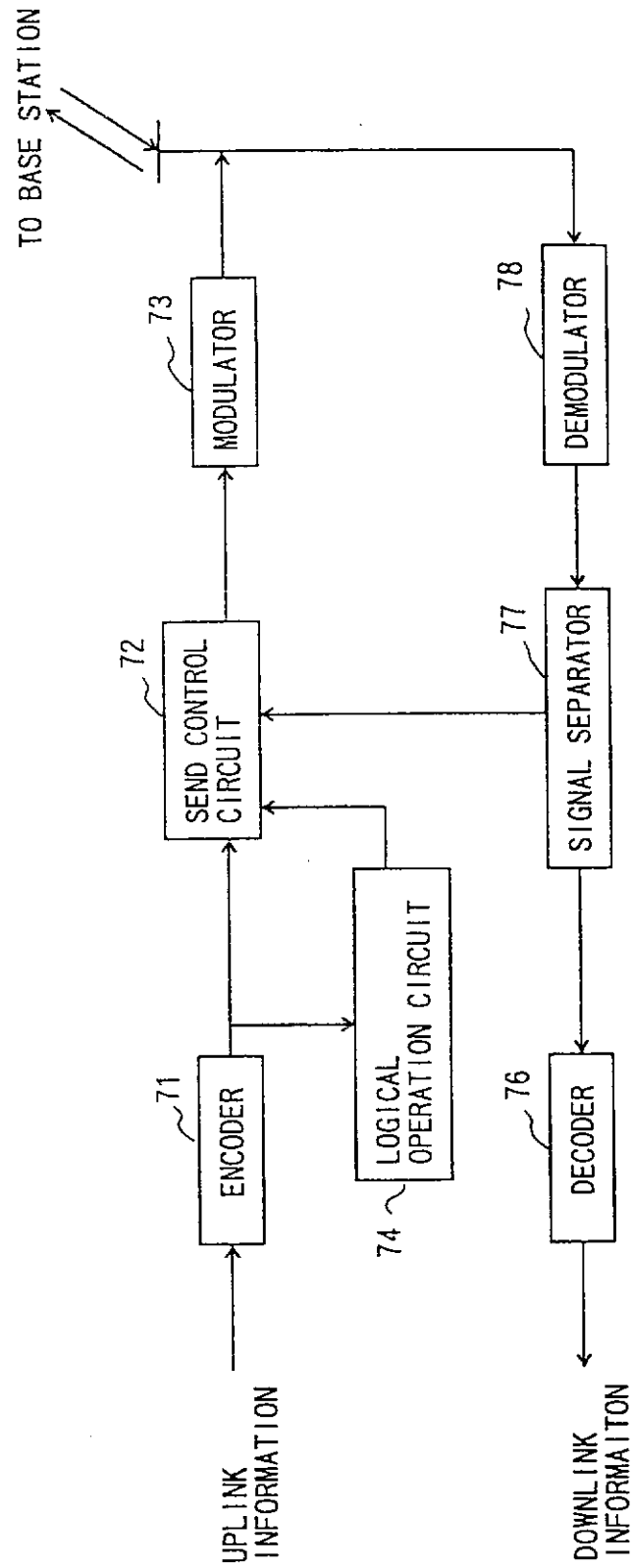


FIG. 19

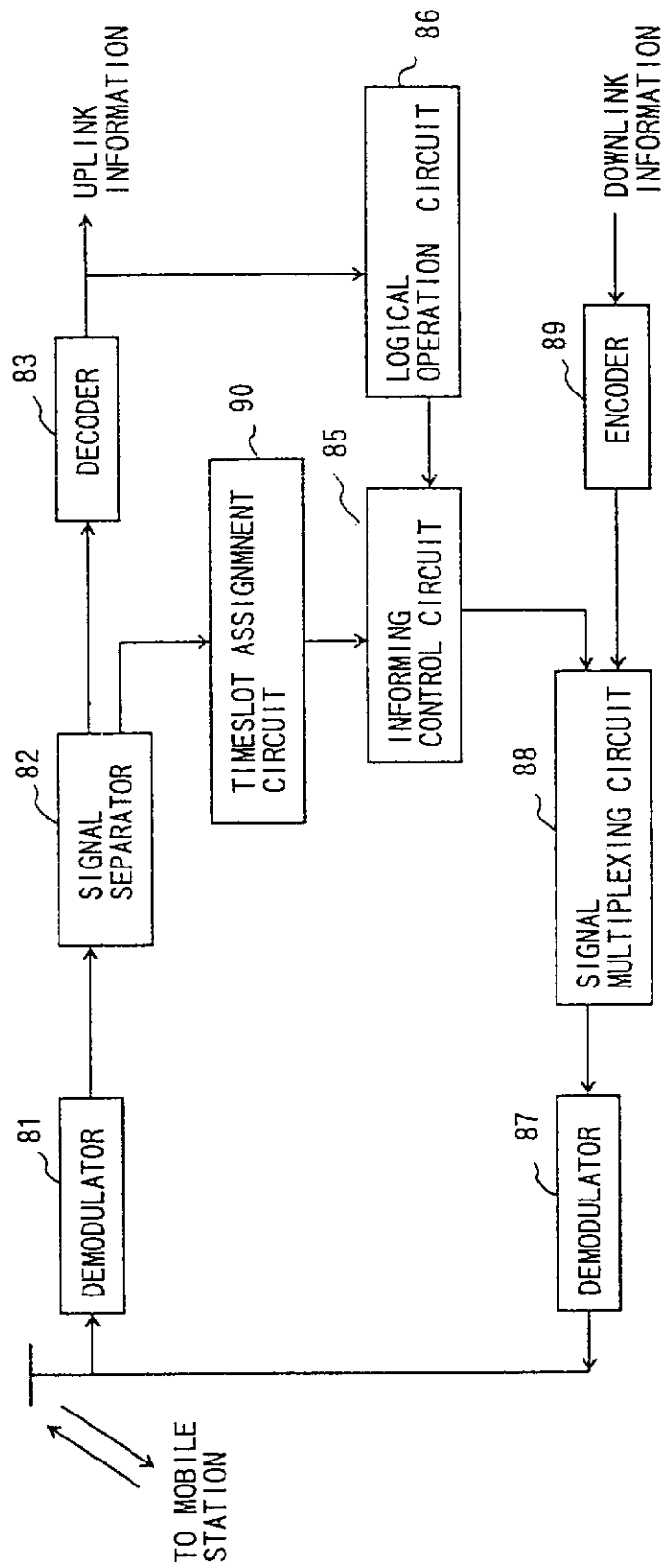


FIG. 20

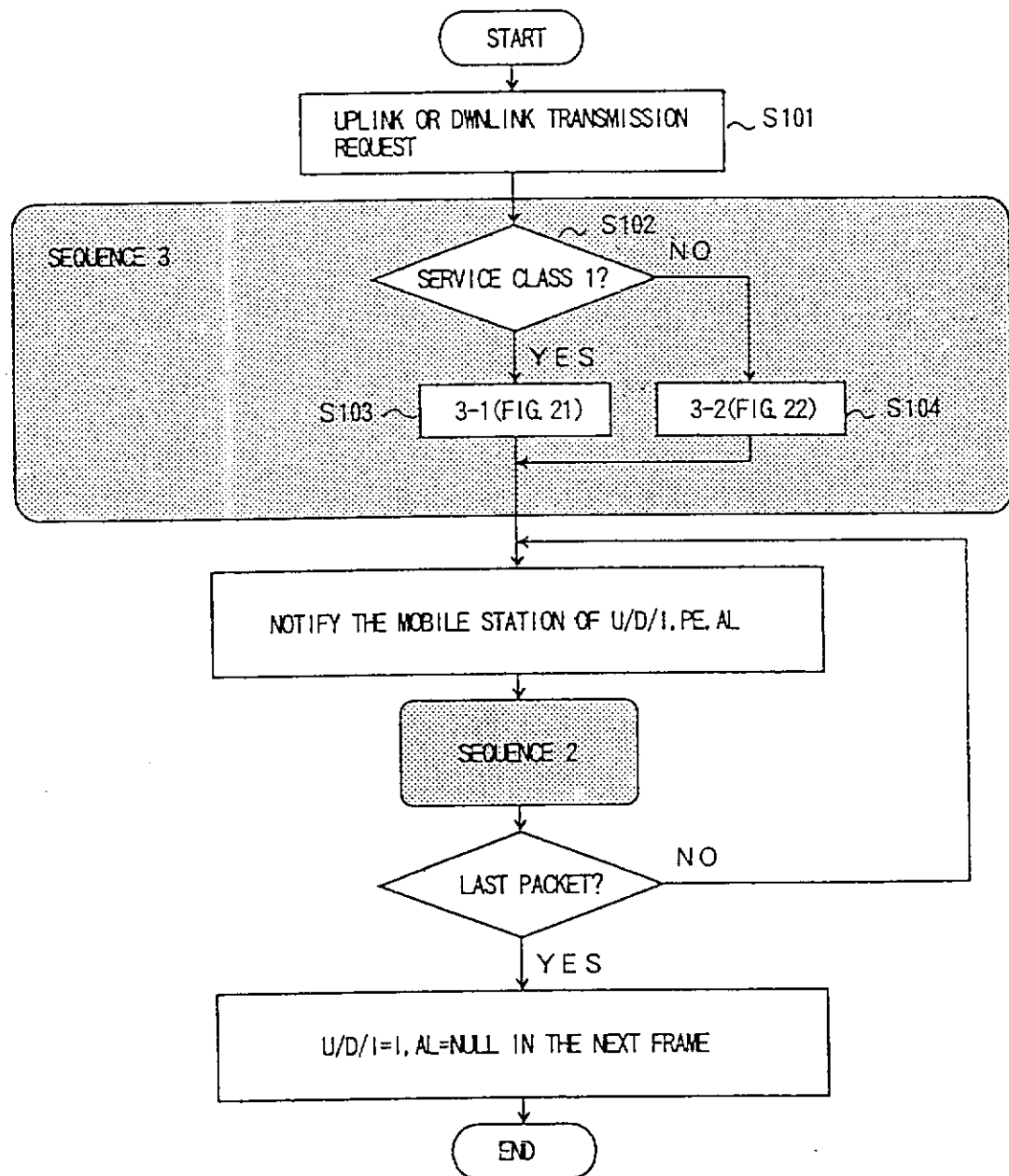


FIG. 21

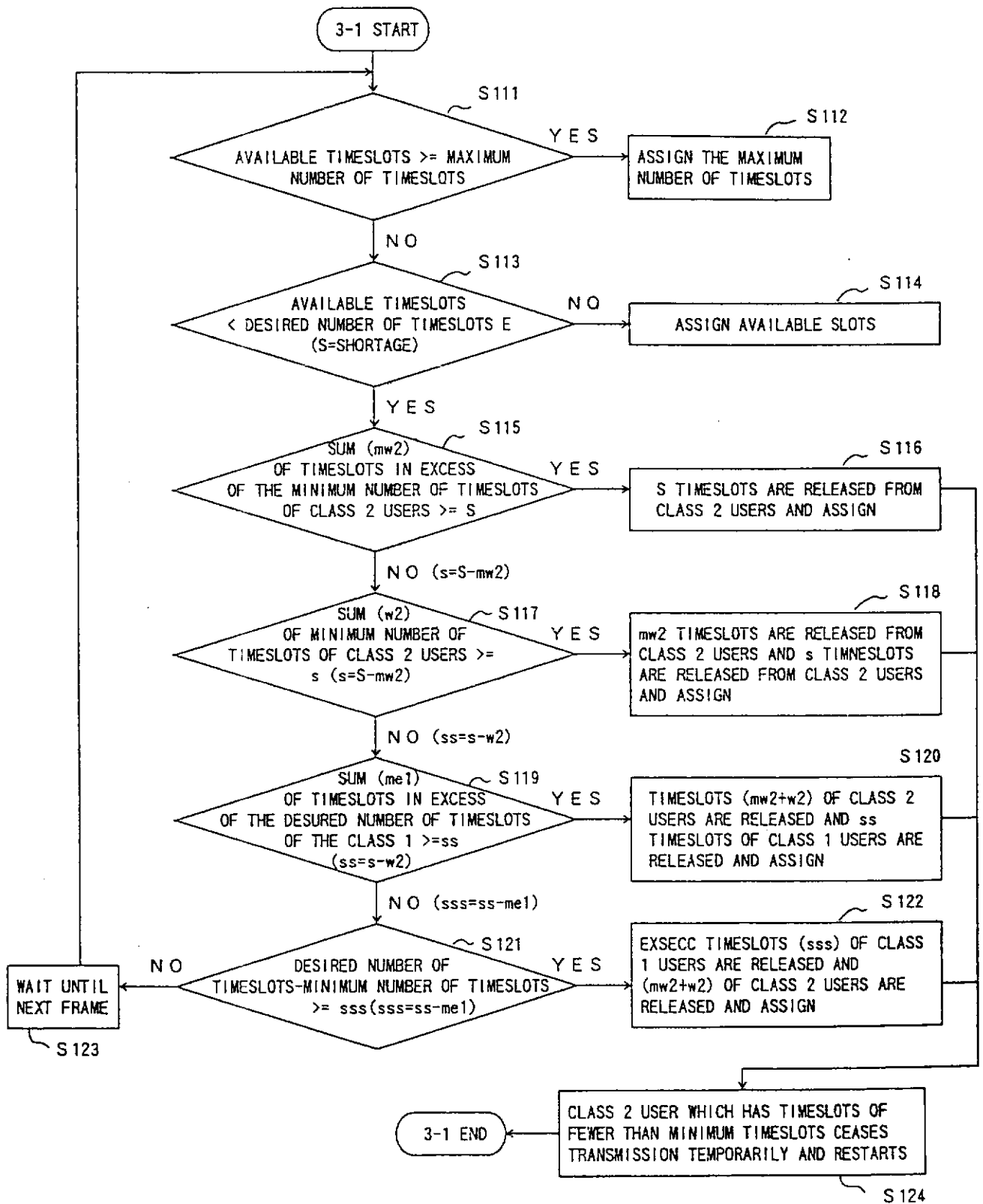


FIG. 22

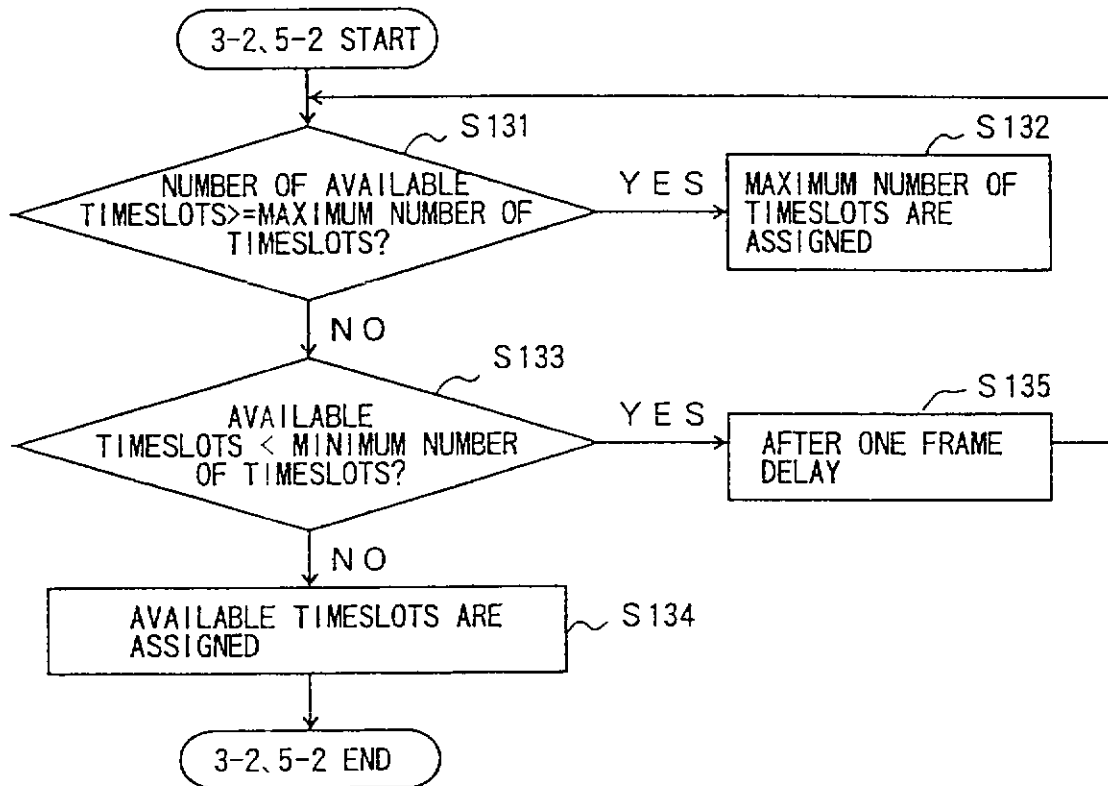


FIG. 23

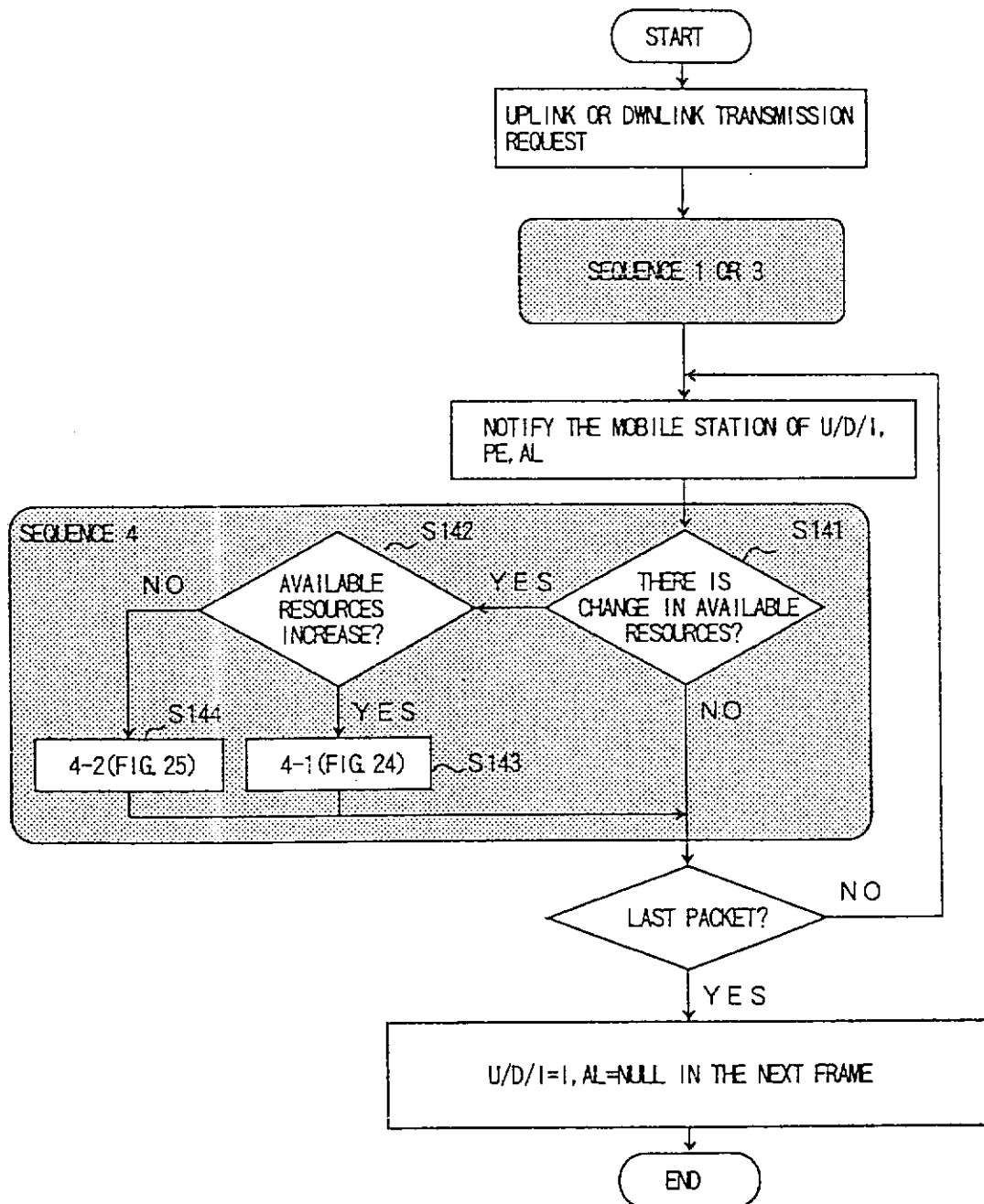


FIG. 24

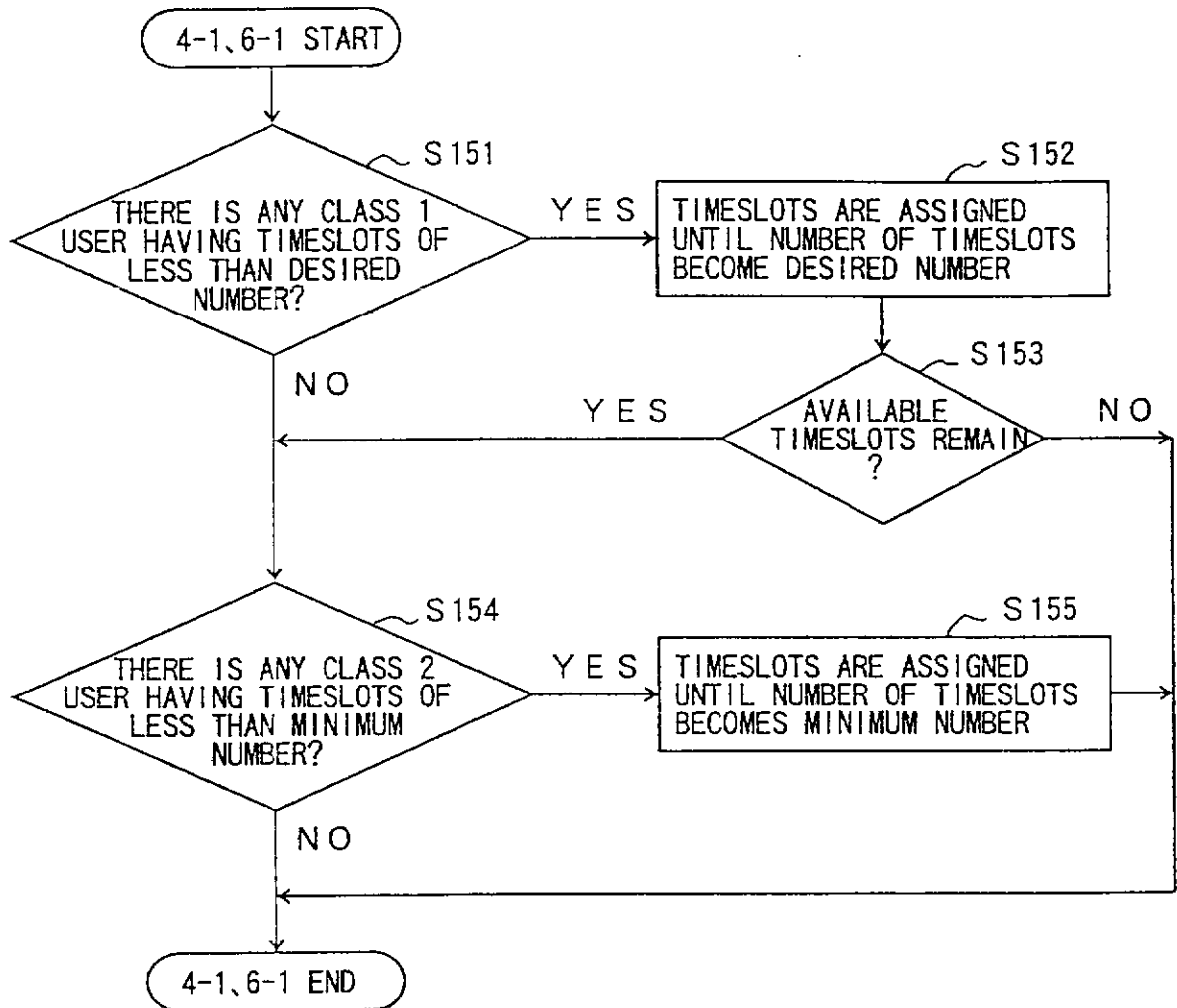


FIG. 25

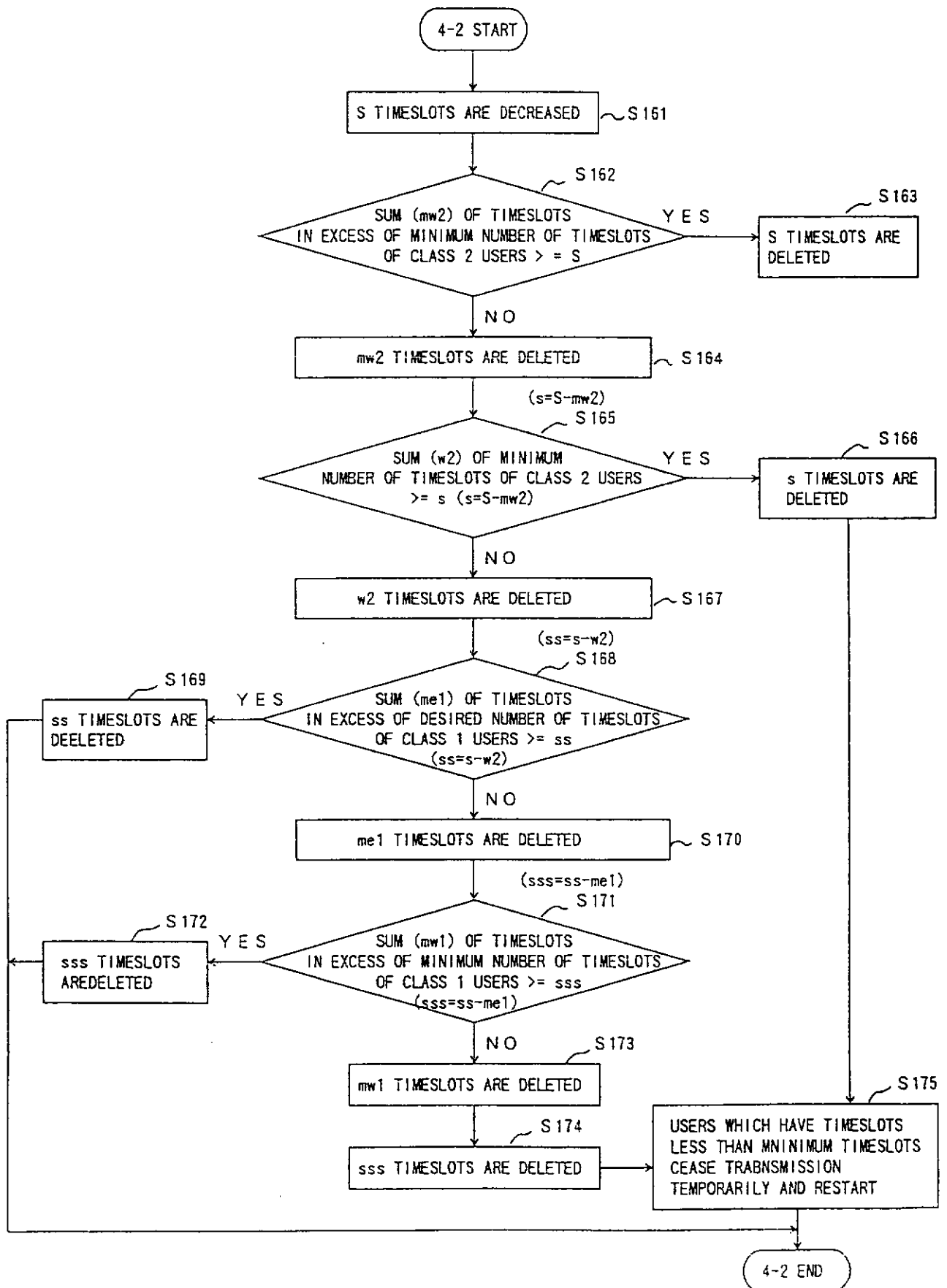


FIG. 26

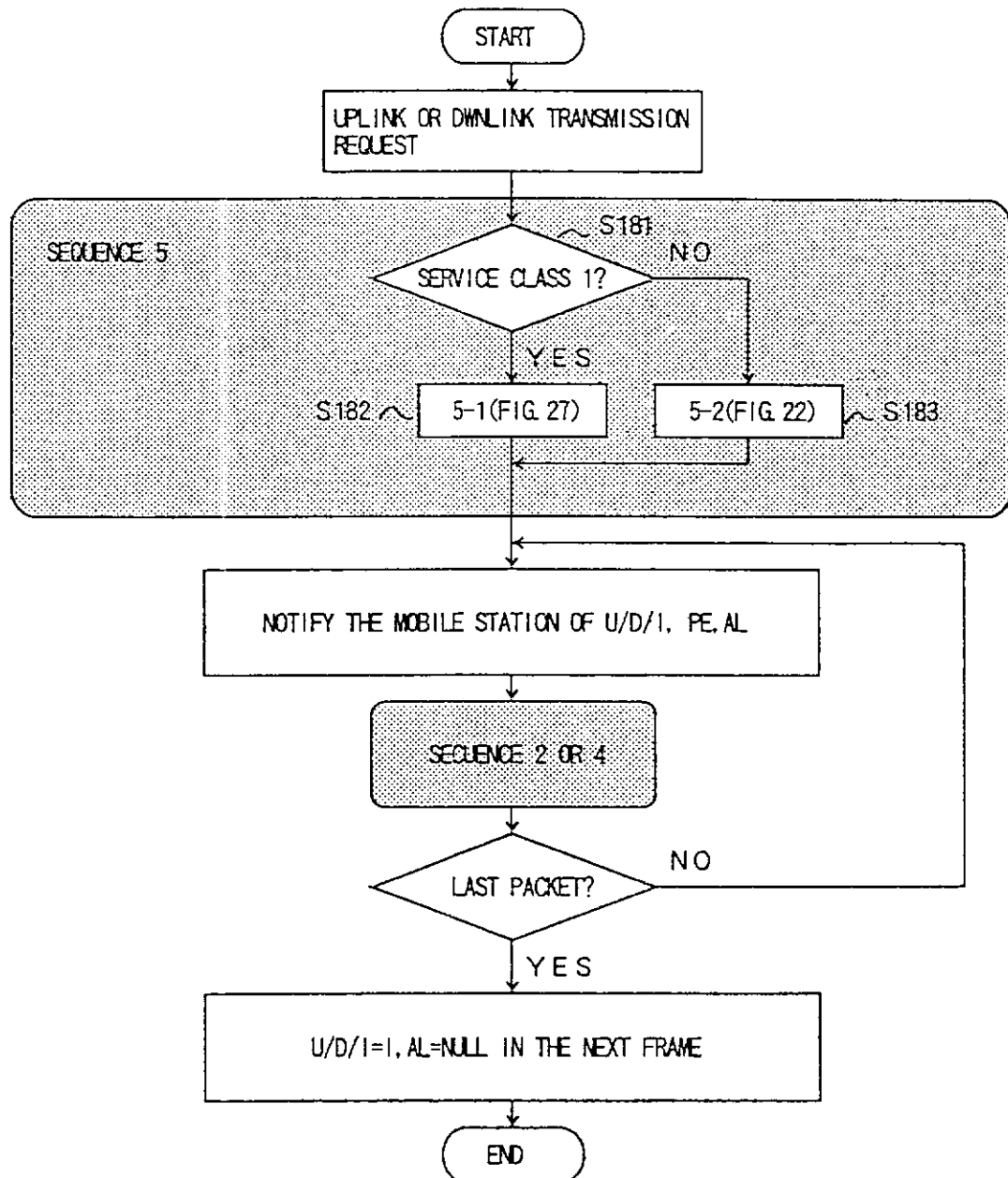


FIG. 27

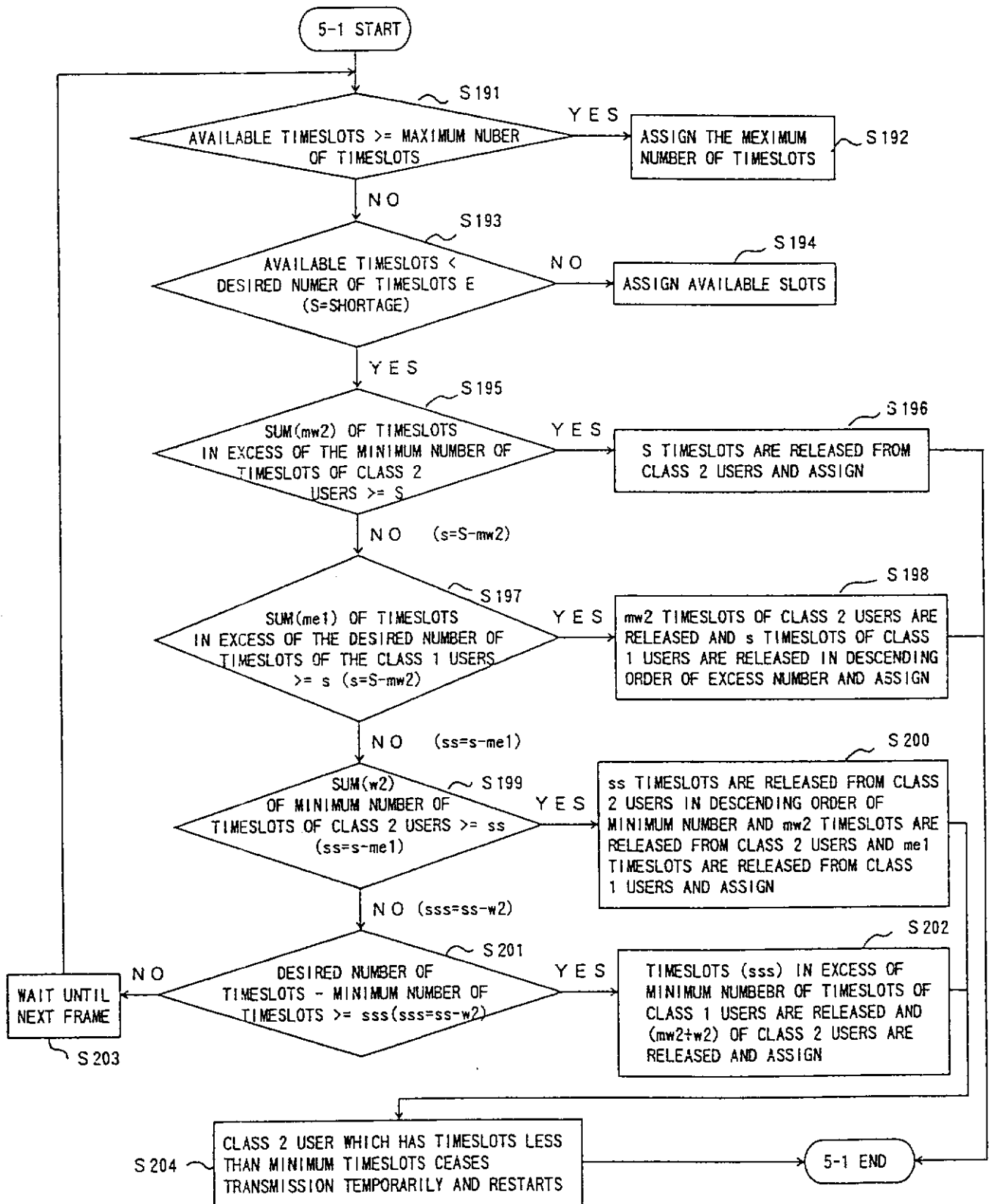


FIG. 28

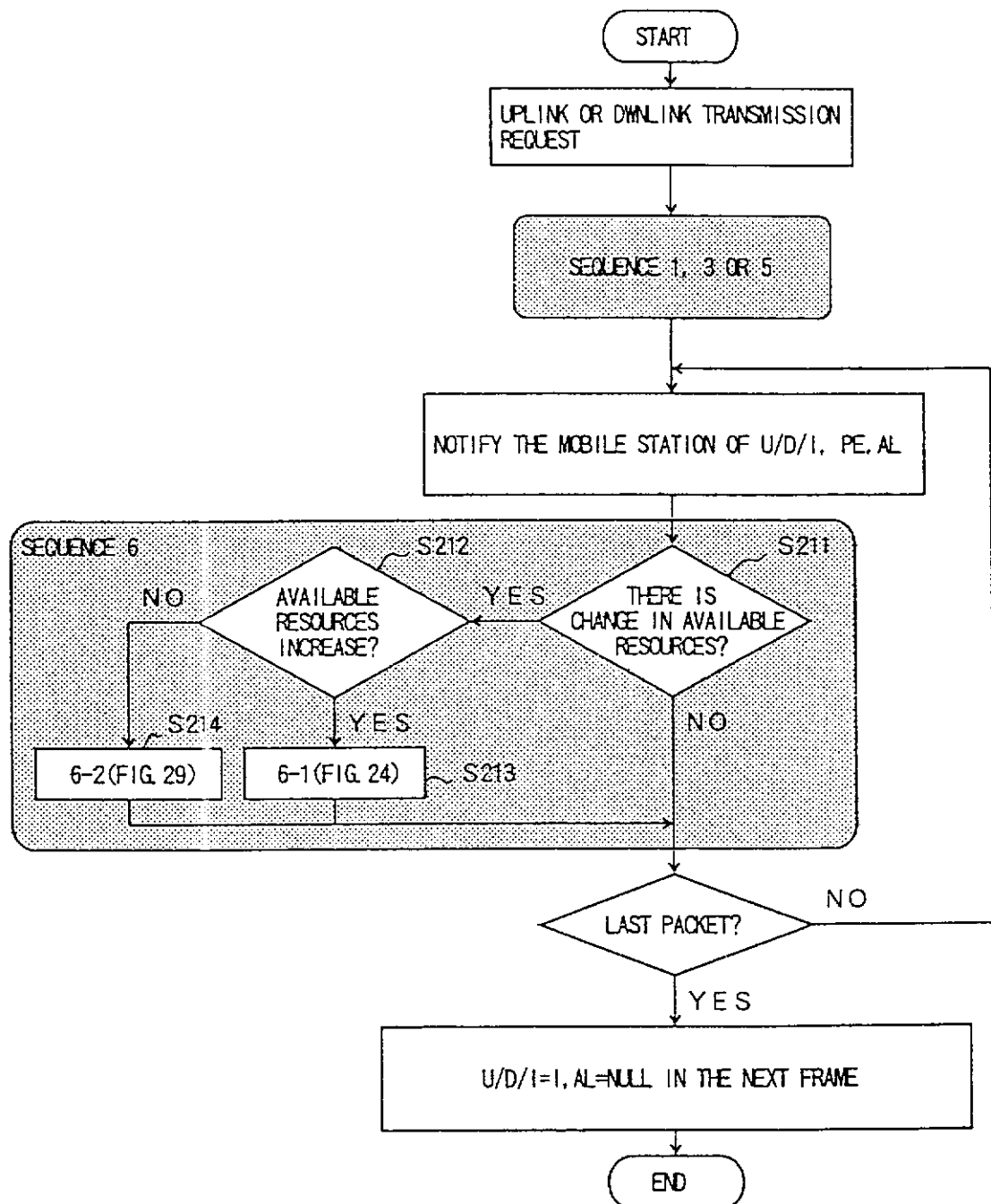


FIG. 29

