

By application of a method and a circuit for retiming a digital data signal (D_{in}) consisting of a number of successive bits, wherein the data signal is sampled by an internal clock signal (CK_{int}) generated from an external clock signal (CK_{ref}), the internal clock signal (CK_{int}) is phase locked to the data signal (D_{in}) so that the latter is sampled approximately in the centre of every bit. By generating the internal clock signal from the external clock signal, and at the same time phase locking it to the data signal, the internal clock signal will automatically adjust itself so that the data signal is sampled at the appropriate point in time, i.e. in the centre of the bit period. As a result, there are no strict requirements as to the synchronisation between the data signal and the clock signal, and an individual adjustment of the synchronisation in preceding circuits is thus avoided.