CLAIMS

~~1.~~ 1. An apparatus, comprising:

an analog phase change memory array, the phase change memory array comprising an array of cells addressable and accessible through first lines and second lines; and

at least one device coupled to one or more of the first lines, the at least one device able to be coupled to or decoupled from the one or more first lines to compensate for phase change memory resistance drift in resistance of at least one of the cells in the one or more first lines, the at least one device being resistive and compensating for resistance drift based at least on a voltage divider between the at least one device and corresponding at least one of the cells when the at least one device is coupled to the corresponding at least one of the cells.

~~2.~~ 2. The apparatus of claim ~~1,~~1, wherein one or more of the at least one devices comprise a resistor.

~~3.~~ 3. The apparatus of claim ~~2,~~2, wherein the apparatus comprises one or more switches, and wherein the at least one device comprises a single resistor for all of the one of the one or more switches, wherein the single resistor is coupled to or uncoupled from each of the one or more first lines via a corresponding one of the one or more switches.

~~4.~~ 4. The apparatus of ~~either of claims~~claim 2 ~~or 3~~, wherein the at least one device comprises a resistor for each corresponding one of the one or more first lines.

~~5.~~ 5. The apparatus of ~~any of claims~~claim 2 ~~to 4, ~~, wherein a value of one of the resistors is about 3.8 KOhm.

~~6.~~ 6. The apparatus of ~~any of the preceding claims~~claim 1, wherein the apparatus comprises one or more switches, and wherein the at least one device comprises a single transistor for all of the one ~~of the one~~ or more switches, wherein the single transistor is coupled to or uncoupled from each of the one or more first lines via a corresponding one of the one or more switches.

~~The~~7. An apparatus ~~of claim 6, further,~~ comprising~~:~~:

an analog phase change memory array, the phase change memory array comprising an array of cells addressable and accessible through first lines and second lines;

one or more switches;

at least one device coupled to one or more of the first lines, the at least one device able to be coupled to or decoupled from the one or more first lines to compensate for phase change memory resistance drift in resistance of

at least one of the cells in the one or more first lines, wherein the at least one device comprises a single transistor for all of the one or more switches, wherein the single transistor is coupled to or uncoupled from each of the one or more first lines via a corresponding one of the one or more switches;

~~7.~~ control circuitry ~~and,~~ wherein the control circuitry is configured to use the transistor as a tunable resistor at least by adjusting gate voltage of the transistor to adjust a resistance of the transistor.

~~8.~~ 8. The apparatus of ~~any of the preceding claims~~claim 1, wherein the cells able to be connected to a device have a phase change memory resistance having a value that can be set to more than two states.

~~9.~~ 9. The apparatus of claim ~~8,~~8, wherein the phase change memory resistance values can vary from about 10 KOhm to about 100 KOhm.

~~10.~~ 10. The apparatus of claim ~~8,~~8, further comprising control circuitry and wherein the control circuitry is configured to reduce phase change memory resistance drift of the phase change resistance by sending a same set pulse to individual phase change memory resistors sequentially once each period.

~~11.~~ 11. The apparatus of claim ~~10,~~10, wherein the period is every few minutes.

~~12.~~ 12. The apparatus of claim ~~10,~~10, wherein the period is every tens of minutes.

~~13.~~ 13. The apparatus of claim ~~10,~~10, wherein the set pulse satisfies following conditions:

the set pulse is a voltage pulse that crystalizes the phase change memory resistor and reduces the resistance to compensate the resistance drift toward a high resistance value; and

the set pulse voltage is automatically divided between the at least one device and phase change memory resistor so that an actual pulse voltage applied to the phase change memory resistor is tailored to the resistance value of that phase change memory resistor.

~~14.~~ 14. The apparatus of claim ~~13,~~13, wherein a pulse height of the voltage pulse is about 2.1 Volts.

~~15.~~ 15. The apparatus of ~~any of the preceding claims~~claim 1, wherein ~~either~~one of the following is true: the first lines are word lines and the second lines are bit lines; or the first lines are bit lines and the second lines are word lines.

~~16.~~ ~~The~~16. An apparatus ~~of any of the preceding claims further,~~ comprising:

an analog phase change memory array, the phase change memory array comprising an array of cells addressable and accessible through first lines and second lines; and

at least one device coupled to one or more of the first lines, the at least one device able to be coupled to or decoupled from the one or more first lines to compensate for phase change memory resistance drift in resistance of at least one of the cells in the one or more first lines, the at least one device being resistive and compensating for resistance drift based at least on a voltage divider between the at least one device and corresponding at least one of the cells when the at least one device is coupled to the corresponding at least one of the cells; and

control circuitry configured to send, using the first lines and second lines, a same set pulse through the at least one device to a plurality of individual phase change memory resistors in the phase change memory array sequentially once every period.

~~17.~~ 17. The apparatus of claim ~~16, wherein the control circuitry comprises one or more processors and one or more memories comprising computer readable code, wherein the one or more processors, in response to loading and executing the computer readable code, causes the sending of the same pulse.~~

~~18. A method for operating an apparatus of any of claims 1 to 17, comprising:~~

~~addressing and accessing an array of cells of an analog phase change memory array, through first lines and second lines of the array; and~~

~~compensating for phase change memory resistance drift in resistance of at least one of the cells in the one or more first lines, by coupling or decoupling from the one or more first lines of at least one device are capable of being coupled to one or more of the first lines.~~

~~19. The method of claim 18, wherein one or more of the at least one devices comprise a resistor.~~

~~20. The method of claim 19, wherein the apparatus comprises one or more switches, and wherein the at least one device comprises a single resistor for all of the one of the one or more switches, wherein the single resistor is coupled to or uncoupled from each of the one or more first lines via a corresponding one of the one or more switches.~~

~~21. The method of either of claims 19 or 20, wherein the at least one device comprises a resistor for each corresponding one of the one or more first lines.~~

~~22. The method of any of claims 19 to 21, wherein a value of one of the resistors is about 3.8 KOhm.~~

~~23. The method of any of the preceding claims, wherein the apparatus comprises one or more switches, and wherein the at least one device comprises a single transistor for all of the one of the one or more switches, wherein the single transistor is coupled to or uncoupled from each of the one or more first lines via a corresponding one of the one or more switches.~~

~~24. The method of claim 23, further comprising control circuitry, the method further comprising configuring the control circuitry to use the transistor as a tunable resistor at least by adjusting gate voltage of the transistor to adjust a resistance of the transistor.~~

~~25. The method of any of the preceding claims, the method further comprising connecting the cells to a device have a phase change memory resistance having a value that can be set to more than two states.~~

~~26. The method of claim 258, wherein the phase change memory resistance values can vary from about 10 KOhm to about 100 KOhm.~~

~~27. The method of claim 25, further comprising control circuitry, the method comprising configuring the control circuitry to reduce phase change memory resistance drift of the phase change resistance by sending a same set pulse to individual phase change memory resistors sequentially once each period.~~

~~28.~~ ~~The method of claim 10,~~16, wherein the period is every few minutes.

~~29.~~ 18. The ~~method~~apparatus of claim ~~27~~16, wherein the period is every tens of minutes.

~~30.~~ 19. The ~~method~~apparatus of claim ~~27~~16, wherein the set pulse satisfies following conditions:

the set pulse is a voltage pulse that crystalizes the phase change memory resistor and reduces the resistance to compensate the resistance drift toward a high resistance value; and

the set pulse voltage is automatically divided between the at least one device and phase change memory resistor so that an actual pulse voltage applied to the phase change memory resistor is tailored to the resistance value of that phase change memory resistor.

~~31.~~ 20. The ~~method~~apparatus of claim ~~30, wherein a pulse height of the voltage pulse is about 2.1 Volts.~~

~~32. The method of any of the preceding claims, wherein either the first lines are word lines and the second lines are bit lines; or the first lines are bit lines and the second lines are word lines.~~

~~33. The method of any of the preceding claims further comprising:~~

~~configuring the control circuitry to send, using the first lines and second lines, a same set pulse through the at least one device to a plurality of individual phase change memory resistors in the phase change memory array sequentially once every period.~~

~~34. The method of claims 33~~16, wherein the control circuitry comprises one or more processors and one or more memories comprising computer readable code, wherein the one or more processors, in response to loading and executing the computer readable code, ~~send~~cause the sending of the same pulse.