

DESCRIPTION

TITLE: Superlattice obtained by layer transfer, structure and fabrication process

TECHNICAL FIELD OF THE INVENTION

The invention generally relates to superlattices, which consist of at least one periodic stack of thin layers. The invention more particularly relates to superlattices including semiconductor layers.

TECHNOLOGICAL BACKGROUND

Superlattices have attracted attention because of their mechanical and semiconducting properties and also because they may be used to form quantum dots.

They have also been employed to develop what are known as nanosheet transistors or gate-all-around field-effect transistors (GAAFETs), the conduction channels of which are formed by a stack of layers of nanoscale thickness each encircled by a gate metal, as described in patents US 10,249,739 B2 and US 11,018,222 B1. The gate of these semiconductor structures surrounds the channel, hence the expression "gate-all-around".

This principle has been applied to form complementary field-effect transistors (CFETs) having a three-dimensional structure formed using a pair of stacked superlattices: a first superlattice formed on a substrate is used to form a p-type transistor while a second superlattice formed on the first superlattice is used to form an n-type transistor, or vice versa. This three-dimensional structure is advantageous in terms of integration compared to conventional approaches used to implement CMOS technology, which typically employs p-type transistors and n-type transistors fabricated side-by-

side in the same plane. In particular, the CFET approach in principle makes it possible to halve the footprint of a pair of p- and n-type transistors, or to shorten the connections between the two transistors and therefore decrease the electrical resistance of the corresponding connections. This approach is for example described in documents US 2019/0319095 A1, US 2021/0104523 A1 and US 2023/0326925 A1.

The document US 2021/082901 A1 discusses joining multilayer stacks formed on substrates that may or may not be different.

The document FR 2 857 983 A1 discloses a process for fabricating an epitaxial layer, including removal of the carrier substrate.

Regardless of whether nanosheet transistors or CFETs are concerned, the fabrication processes in question involve fabrication of superlattices comprising stacks of two types of alternating materials: one is intended to form the channel regions of the transistors, the other to form sacrificial layers that will be removed and replaced by a gate-dielectric and gate-metal structure during the fabrication of the transistors.

Fabrication of CFETs requires two types of transistors, one n-type and one p-type, to be stacked on top of each other. Two approaches are possible.

The first approach is said to be "sequential", in the sense that the transistors of two types are formed sequentially, in separate steps. In this approach, a semiconductor structure made of silicon or another semiconductor, or indeed a superlattice intended to form second nanosheet transistors, is transferred to a semiconductor substrate already carrying, for example, first nanosheet transistors. Initially, the first transistors are formed on the substrate, then the semiconductor structure is transferred thereto, second transistors then being formed in

the semiconductor structure. The thermal budget for the process of transferring the semiconductor structure and for forming the second transistors is limited by the need to not degrade the first transistors. Furthermore, the alignment of the second transistors with the first transistors must be extremely exact and specific electrical contact structures must be provided between the two stages.

The second approach is said to be "monolithic", in the sense that the first and second transistors are formed on the same substrate, at least some of the fabrication steps being applied simultaneously to all the layers in which the first and second transistors are formed. Reference may be made to document US 2019/0319095 A1. One of the main advantages of this approach is the self-alignment of the second transistors with the first transistors, which allows a higher density of transistors on the substrate, and decreases parasitic capacitances and resistances between the first and second transistors.

The monolithic approach requires thicker superlattices as starting structure than the sequential approach, since these superlattices form the base structure of two simultaneously fabricated superposed transistors. The superlattices are generally fabricated by epitaxy. However, the number of layers that can be stacked to form these superlattices is limited by the critical epitaxy thickness, beyond which the quality of the layers deposited degrades as a result of elastic relaxation and/or plastic relaxation. The monolithic approach is getting close to the critical epitaxy thickness and could require it to be exceeded.

Thus, there is a need for superlattice structures comprising layers of sufficient number and quality to guarantee the uniformity and performance of transistors formed from these layers. Furthermore, CFET fabrication processes require base structures that will increase the ease and

reliability of CFET fabrication and, if possible, improve the characteristics of the obtained devices, in particular their footprint, parasitic capacitance, or indeed the electrical resistance of their interconnects.

SUMMARY OF THE INVENTION

The objective of the applicant is to provide a process for fabricating a structure apt to facilitate integration and production of nanosheet transistors, and optionally of CFETs, i.e. of superposed p-type and n-type transistors. More generally, the aim of the process according to the invention is to form superlattices having an arbitrary thickness or number of layers.

With a view to achieving this goal, one aspect of the invention is a process for fabricating a structure comprising at least one superlattice, comprising the steps of: forming a first superlattice on a first substrate, by stacking a plurality of first channel layers in alternation with a plurality of first sacrificial layers; forming a first cap layer on the first superlattice; forming at least one second sacrificial layer on a second substrate; forming a second cap layer on the at least one second sacrificial layer; forming a weakening plane in the carrier substrate by implanting ions of a light species into the donor substrate through the at least one second sacrificial layer and the second cap layer, and joining the at least one sacrificial layer to the first superlattice by placing the second cap layer in contact with the first cap layer, which together form a bonding layer, the first superlattice, the bonding layer and the at least one sacrificial layer being stacked in this order, splitting the donor substrate in the weakening plane and withdrawing part of the donor substrate after the joining step,

wherein the first cap layer and the second cap layer each have a thickness of less than 2 nm.

A first advantage of the process is that it provides a stack of superlattices that may be either identical or distinct in composition and/or orientation.

A second advantage of the process is the ability of the structures obtained to exceed the critical epitaxy thickness, which limits the number and thickness of layers able to be grown epitaxially on top of one another without the crystal structures of these layers losing their quality.

A third advantage of the process lies in the provision within the stack of a bonding layer between two superlattices, this layer potentially being removed in the same process as that used to remove sacrificial layers included in the superlattices.

Thus, the fabrication process according to the invention is suitable for producing structures able to serve as base for a monolithic process for producing an electronic circuit integrating nanosheet transistors or CFETs.

According to additional non-limiting features of the process according to the invention, which may be implemented individually or in any technically feasible combination:

- the step of forming at least one second sacrificial layer on the second substrate may consist in forming a second superlattice by stacking a plurality of second channel layers in alternation with a plurality of second sacrificial layers;

- the step of forming at least one second sacrificial layer on the second substrate may consist in forming a seed layer, the process potentially further comprising a step of forming a second superlattice on the seed layer after the joining step, by stacking a plurality of second channel layers in alternation with a plurality of second sacrificial layers;

- the bonding layer may be continuously formed in a plane parallel to a surface of the first substrate on which the first superlattice is formed;

- the first channel layers and second channel layers may each be formed from a semiconductor, and the first sacrificial layers and second sacrificial layers may each be formed from a material that is liable to have a faster etch rate than the first channel layers and second channel layers, respectively;

- the sacrificial layers in direct contact with the bonding layer may each have a thickness equal to or less than half the thicknesses of the other sacrificial layers;

- the process may further comprise a step of removing at least one part of the second substrate after the joining step;

- the process may further comprise a step of uncovering a channel layer of the second superlattice after the step of withdrawing the second substrate;

- the first cap layer and the second cap layer may each be formed from silicon;

- one of the first cap layer and the second cap layer may be formed from amorphous silicon and the other may be formed from crystalline silicon;

- the process may further comprise a step of forming at least one etch-stop layer on the second substrate prior to forming the seed layer;

- the at least one etch-stop layer may comprise a layer of the same material as the seed layer;

- the first channel layers may be formed from silicon; the first sacrificial layers may be formed from a first silicon-germanium alloy; the first cap layer may be formed on and in direct contact with one of the sacrificial layers of the first superlattice; the second sacrificial layer may be formed from a second silicon-germanium alloy; the second cap layer may be formed on and in direct contact with the at least one second sacrificial layer; and the first cap layer and the second cap layer may each be formed from silicon.

The invention extends to a structure for a superlattice stack, comprising: a carrier substrate; a first superlattice

on the carrier substrate; a bonding layer on the first superlattice, said bonding layer being formed from a first cap layer and from a second cap layer; and a second superlattice on the bonding layer, wherein the first cap layer and the second cap layer each have a thickness of less than 2 nm.

According to additional non-limiting features of the structure according to the invention, which may be implemented individually or in any technically feasible combination:

- the bonding layer may be continuously formed in a plane parallel to a surface of the carrier substrate bearing the first superlattice;

- the first superlattice may be formed from a stack of a plurality of first channel layers in alternation with a plurality of first sacrificial layers; the second superlattice may be formed from a stack of a plurality of second channel layers in alternation with a plurality of second sacrificial layers; the first channel layers and second channel layers may each be formed from a semiconductor, and the first sacrificial layers and the second sacrificial layers may each be formed from a material that is capable of having a faster etch rate than the first channel layers and the second channel layers, respectively;

- one of the first cap layer and the second cap layer may be formed from crystalline silicon and the other of the first cap layer and the second cap layer may be formed from amorphous silicon; and

- the sacrificial layers in direct contact with the bonding layer may each have a thickness equal to or less than half the thicknesses of the other sacrificial layers.

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will become apparent from the following detailed description of the invention, this description being given with reference to the appended figures, in which:

[Fig. 1] Figure 1 illustrates a first fabrication process according to the invention;

[Fig. 2] Figure 2 shows a continuation of the process of Figure 1;

[Fig. 3] Figure 3 illustrates variants of structures able to be obtained with the process of Figures 1 and 2;

[Fig. 4] Figure 4 shows a detail of one of the variants of the bonding layer of Figure 3;

[Fig. 5] Figure 5 illustrates one advantage of the structures of Figure 3 in the fabrication of nanosheet transistors or CFETs;

[Fig. 6] Figure 6 is a diagram summarizing the fabrication process of Figures 1 and 2;

[Fig. 7] Figure 7 illustrates a second fabrication process according to the invention;

[Fig. 8] Figure 8 shows a continuation of the process of Figure 7; and

[Fig. 9] Figure 9 is a flowchart summarizing the fabrication process of Figures 7 and 8.

DETAILED DESCRIPTION OF THE INVENTION

First embodiment

A first embodiment of the present invention is described by means of Figures 1 to 6 and the associated description below.

Figure 3 illustrates in (A) a structure Strc formed from a carrier substrate Car, from a first superlattice Stck1, from a bonding layer Bnd, and from a second superlattice Stck2, stacked in this order. The first superlattice Stck1 comprises

a plurality of first layers Ch1 stacked in alternation with a plurality of first layers Sac1, preferably so that each first layer Ch1 is interposed between and in direct contact with two of the first layers Sac1. The second superlattice Stck2 comprises a plurality of second layers Ch2 stacked in alternation with a plurality of second layers Sac2, preferably so that each second layer Ch2 is interposed between and in direct contact with two of the second layers Sac2.

The first layers Ch1 and second layers Ch2 are layers formed from at least one semiconductor intended to form transistor channel regions and may be designated the first channel layers Ch1 and second channel layers Ch2, respectively. These channel layers may be formed from the same material, or from different materials.

The first layers Sac1 and second layers Sac2 are layers formed from at least one material capable of having faster etch rates than the first layers Ch1 and second layers Ch2, and may be designated the first sacrificial layers Sac1 and second sacrificial layers Sac2, respectively. These sacrificial layers may be formed from the same material, or from different materials. In particular, the layers Sac1 may have a $\text{Si}_{1-x}\text{Ge}_x$ composition and the layers Sac2 may have a $\text{Si}_{1-y}\text{Ge}_y$ composition where x and y represent the proportions of germanium in the layers Sac1 and Sac2, respectively, with x possibly being different from or equal to y . These layers Sac1 and Sac2 of SiGe alloy may be associated with silicon layers Ch1 and Ch2 by virtue of the epitaxial growth compatibility of these two materials, which possess a fairly similar lattice parameter. The proportions x and y are preferably less than 40%, and for example between 15% and 35%.

The second layers Sac1 and Sac2 are intended to serve as sacrificial layers in a procedure for forming nanosheet transistors, in which the layers Sac1 and Sac2 are removed by etching, possibly chemical etching, so as to obtain a

structure with floating strips formed from the layers Ch1 and Ch2. These floating strips will subsequently be encircled by a layer of gate dielectric and by a gate metal so as to form nanosheet transistors.

Figures 1, 2 and 6 illustrate a process for fabricating the structure Strc, which process is advantageously based on separate fabrication of two superlattices Stck1 and Stck2 on two respective substrates, then transfer of the second superlattice Stck2 to the first superlattice Stck1. The first and second superlattices each comprise at least two channel layers Ch1 and Ch2, respectively. Figure 6 is a flowchart schematically showing the steps of the fabrication process 600.

Figure 1 illustrates in (A) formation of the first superlattice Stck1 on a carrier substrate Car, in a step 610_{Car}. In this example, the carrier substrate Car is a single-crystal silicon wafer. On a surface S_{car} of the substrate Car, layers Ch1 of silicon Si that are from 5 to 15 nm thick, and preferably from 7 to 10 nm thick, are grown by epitaxy, in alternation with layers Sac1 of a first silicon-germanium alloy of formula Si_{1-x}Ge_x that are from 5 to 10 nm thick, and preferably from 6 to 9 nm thick, where x is the percentage of germanium in the alloy, the layers preferably starting and ending with a layer Sac1.

On and in direct contact with the last layer Sac1, in a step 620_{Car}, a cap layer Cap1 is formed, here formed from silicon Si of crystalline or amorphous structure, which layer has the function of preventing oxidation of the last layer Sac1. The layer Cap1 may have a thickness of less than 2 nm or 3 nm, for example a thickness between 0.5 and 2 nm, and preferably between 1 and 2 nm, for reasons that will be explained below, by means of Figure 5.

Figure 1 illustrates in (B) formation of the second superlattice Stck2 on a donor substrate Don, in a step 620_{Don}.

In this example, the donor substrate Don is a single-crystal silicon wafer.

On a surface S_{Don} of the substrate Don, layers Ch2 of silicon Si that are from 5 to 15 nm thick, and preferably from 7 to 10 nm thick, are grown by epitaxy, in alternation with layers Sac2 of the first silicon-germanium alloy of formula $Si_{1-x}Ge_x$ that are from 5 to 10 nm thick, and preferably from 6 to 9 nm thick. Preferably, the growth is carried out so that it begins and ends with a sacrificial layer Sac2. On and in direct contact with the last layer Sac2, a cap layer Cap2, made of silicon of amorphous or crystalline structure, is formed in a step 630_{Don}. Preferably, one of the silicon layers Cap1 and Cap2 has an amorphous structure while the other has a crystalline structure in order to facilitate their subsequent assembly by direct contact. The function of the layer Cap2 is to prevent oxidation of the last layer Sac2. This layer Cap2 is however optional, its advantageousness depending on the ease with which the material from which the last layer of the second superlattice Stck2 is made oxidises. The layer Cap2 may have a thickness of less than 2 nm or 3 nm, for example a thickness between 0.5 and 2 nm, and preferably between 1 nm and 2 nm, for reasons that will be explained below, by means of Figure 5.

Optionally, before the second superlattice Stck2 is formed, it is possible to form, on the donor substrate Don, a layer Stp, which is for example formed from the first silicon-germanium alloy of formula $Si_{1-x}Ge_x$ and has a thickness between 5 and 10 nm, in a step 610_{Don}. This layer is an etch-stop layer and is intended to protect the integrity of the layers of the second superlattice Stck2 in the fabrication steps that come after the donor substrate has been split as described below, these steps being illustrated in (B) and (C) of Figure 2.

Figure 1 illustrates in (C) implantation of light species (such as hydrogen, helium, or a combination of such species)

into the donor substrate Don through the surface S_{Don} , the second superlattice Stck2 and the cap layer Cap2, so as to form a weakening plane Imp in the donor substrate Don, in a step 640_{Don}.

The implantation is carried out here after the second superlattice Stck2 has been formed. This order of the operations has a number of advantages over the reverse order. In particular, the temperature of formation by epitaxy of the layers of the second superlattice is not limited by the presence of the weakening plane Imp, it is therefore possible to optimise the growth parameters of the layers and to limit the time necessary for the epitaxy, this limiting diffusion of germanium into the structure. If the implantation was carried out before the second superlattice was formed, a risk would be run of the second superlattice unintentionally detaching during its formation as a result of the thermal budget applied to the weakening layer, and this would require temperature to be limited during growth of the layers. Furthermore, the two superlattices may be formed using the same parameters, and not using two sets of parameters, one of which would need to take into account the presence of a weakening plane, this promoting the uniformity of their characteristics and simplifying the fabrication process.

Following formation of the weakening plane Imp, the donor substrate Don is flipped and the cap layer Cap2 is brought into close contact with the silicon layer Cap1 and is joined thereto, for example by direct bonding or any other bonding technique in which surfaces of elements to be joined are placed in direct contact, so as to obtain the structure illustrated in (A) of Figure 2, in a joining step 660. The bonding layer Bnd is formed in this step by bonding the last layers formed on the carrier substrate Car and on the donor substrate Don, respectively, and corresponds to the assembly formed from the layers Cap1 and Cap2 separating the first

superlattice Stck1 and the second superlattice Stck2, as illustrated in Figure 3. This bonding layer Bnd preferably completely covers the donor substrate Don. Furthermore, the bonding layer Bnd is continuously formed in a plane parallel to the surface S_{Car} of the carrier substrate Car bearing the first superlattice Stck1. Even if the bonding layer does not rigorously cover the entirety of the carrier substrate Car, it is at least continuously formed on a region in which a set of semiconductor components such as transistors, possibly a set of nanosheet transistors or CFETs, is intended to be formed.

Preferably, the carrier and donor substrates comprising the first and second superlattices, respectively, are substantially identical. This advantageously makes it possible to easily produce them on a large scale, thus facilitating their industrialisation. Moreover, substantially identical carrier and donor substrates advantageously makes it possible to obtain a joined structure that is symmetrical and that has similar coefficients of thermal expansion, which advantageously prevents problems with mechanical deformation following the bonding steps and subsequent heat treatments.

At this stage of fabrication, the superlattices Stck1 and Stck2 are sandwiched between the carrier substrate Car and the donor substrate Don. These superlattices must be uncovered in order to make them accessible. This uncovering operation 670 is carried out in two successive steps 670A and 670B which will allow direct access to the second superlattice Stck2. Step 670A here consists in removing most of the donor substrate while step 670B consists in removing the remainder of the donor substrate and revealing the upper part of the second superlattice Stck2.

Figure 2 illustrates in (B) the donor substrate Don being split in the weakening plane Imp obtained by ion implantation, so that part Don_b is removed from the structure illustrated in (A) while part Don_a remains fastened thereto, in the splitting

and withdrawing step 670A. This split may be obtained by heat treatment, optionally assisted by a split-initiating mechanical force, using conventional layer-transfer techniques that are well known in the field of microelectronics.

Following assembly and splitting of the donor substrate, a heat treatment may be applied so as to consolidate the joint and heal the joined layers. The heat-treatment temperature and time are limited to avoid exceeding the permitted thermal budget, so as to avoid or at least limit diffusion of germanium from one layer of the superlattices to another, and in particular contamination of the entire thickness of the channel layers with germanium. The heat treatment may typically consist of an anneal of 2 h or less at a maximum temperature of 750°C and preferably of less than 700°C.

One alternative to the formation of a weakening plane and splitting of the donor substrate Don in this plane may consist in thinning the donor substrate Don after it has been joined, for example by etching, grinding and/or chemical-mechanical polishing (CMP). This thinning may be used to completely remove the second substrate Don if it is continued, for example, to the stop layer Stp.

Figure 2 illustrates in (C) the structure illustrated in (B) after it has been subjected to mechanical and/or chemical attacks to remove the part Don_a of the donor substrate Don, and the etch-stop layer Stp, in step 670B. Thus, the layer Ch2 of the second superlattice furthest from the carrier substrate Car is uncovered in this step.

The structure in (C) of Figure 2 shows the structure Strc formed from the carrier substrate Car, the first superlattice Stck1, the cap layer Cap1 formed from silicon, the cap layer Cap2 formed from silicon, and from the second superlattice Stck2, stacked in this order. The cap layer Cap1 and the cap layer Cap2 form a bonding layer Bnd between the first superlattice Stck1 and the second superlattice Stck2, as

indicated in (A) of Figure 3. This structure is ready to be subjected to a monolithic process for forming CFETs.

The figures contain the indications "Si" or "SiGe" in the locations of certain layers, and in particular those forming the superlattices Stck1 and Stck2, in order to make them easier to read by indicating the compositions thereof for a given example. However, these indications should not be interpreted as limiting the nature of the layers thus annotated. Other materials, and in particular those mentioned in this description, may be used to form these layers.

Figure 3 illustrates in (A') a structure Strc' with one possible particularity of the layers surrounding and in direct contact with the bonding layer Bnd.

In (A) and in (A'), the bonding layer Bnd is formed by bonding the cap layer Cap1 to the cap layer Cap2, which layers are the last layers formed on the carrier substrate Car and on the donor substrate Don, respectively, in direct contact with the last sacrificial layer Sac1 or Sac1₀ formed on the carrier substrate Car and with the last sacrificial layer Sac2 or Sac2₀ formed on the donor substrate Don, respectively. The thicknesses of the latter sacrificial layers Sac1 (denoted Sac1₀ for Strc') and Sac2 (denoted Sac2₀ for Strc') may for example be of same thickness as the other layers Sac1 and Sac2, respectively.

In the example shown in (A), all the layers Sac1 and Sac2 are of same thickness. In this configuration, the distance separating the layers Ch1 and Ch2 closest to each other and separated by the layer Bnd is greater than the distances separating two consecutive layers Ch1 or two consecutive layers Ch2 in the stack, since this distance corresponds to the sum of the thicknesses of a layer Sac1, of a layer Sac2 and of the layer Bnd.

In A', the sacrificial layers in direct contact with the bonding layer Bnd, identified as Sac1₀ and Sac2₀, are

respectively of thicknesses t_{Sac10} and t_{Sac20} less than the thicknesses of the other sacrificial layers Sac1 and Sac2 respectively of thicknesses t_{Sac1} and t_{Sac2} . The layers Sac1_0 and Sac2_0 may thus each have a thickness equal to or less than half the thicknesses of the other sacrificial layers Sac1 and Sac2 , respectively. In this way, the total thickness t_{tot} separating the layers Ch1 and Ch2 closest to each other and separated by the layer Bnd of thickness t_{Bnd} may be close to or even equal to the thicknesses t_{Sac1} and t_{Sac2} , as illustrated in Figure 4 ($t_{\text{tot}} = t_{\text{Sac10}} + t_{\text{Bnd}} + t_{\text{Sac20}}$). One advantage of this geometry is explained with reference to Figure 5.

As explained above, a process for fabricating nanosheet transistors or CFETS employs a semiconductor superlattice having sacrificial layers inserted between layers of a semiconductor intended to form the channel regions of transistors.

According to the invention, in the present embodiment, the silicon layers Cap1 and Cap2 are sufficiently thin for the germanium of the layers Sac1_0 and Sac2_0 to diffuse right through the layers Cap1 and Cap2 in the fabrication process. This diffusion may be ensured by a dedicated heat treatment, by suitably choosing the parameters of a bonding heat treatment carried out when joining the two stacks Stck1 and Stck2 , or by suitably choosing the parameters of a heat treatment used to split the donor substrate Don , the parameters of a heat treatment used to consolidate the joint and repair the joined layers, or indeed by parameterising these various operations so as to ensure diffusion of germanium into the layers Cap1 and Cap2 . Of course, it is advisable not to exceed the required thermal budget in order to prevent the germanium from diffusing all the way through the channel layers. Thus, the thickness of the channel layers may be set so as to take account of this diffusion. Thus, the layers Cap1 and Cap2 of the structures illustrated in Figure 3

are in fact made of a silicon-germanium alloy, and may therefore be considered to be sacrificial layers with respect to the channel layers Ch1 and Ch2, in the same way as the sacrificial layers Sac1, Sac1₀, Sac2 and Sac2₀.

Figure 5 illustrates the structure Strc' of Figure 3 after the sacrificial layers Sac1, Sac1₀, Sac2 and Sac2₀ have been etched away leaving the channel layers Ch1 and Ch2 suspended. In view of the comments in the preceding paragraph, it will be understood that the layers Cap1 and Cap2 forming the bonding layer will also have been etched. In the general case of the structure Strct, a structure with suspended channel layers Ch1 and Ch2 of good crystal quality may be obtained with a thickness and/or number of layers exceeding what is attainable starting with a structure obtained using a conventional epitaxy process, such a process being limited by the critical epitaxy thickness.

Furthermore, in the particular case of the structure Strc', the environment of each of the channel layers Ch1 and Ch2 may be arranged so as to be substantially identical to that of the other channel layers, including in respect of the distances separating them: the distance t_{tot} separating the two channel layers closest to each other and previously separated by the bonding layer Bnd may be made similar to t_{Sac1} and t_{Sac2} or be made equal to these distances separating the other channel layers from each other, as illustrated in Figure 5. One advantage is the uniformity of the environment of the channel layers of the transistors formed on this basis.

The bonding layer Bnd, which is the layer bonding the two superlattices to each other, need not in principle be formed from crystalline silicon or amorphous silicon. The layer Bnd may be formed exclusively from crystalline silicon, exclusively from amorphous silicon, or from any other material compatible with the fabrication processes described in the present document, and optionally with the envisaged

fabrication processes using as base the assembly of the two superlattices Stck1 and Stck2.

The fabrication process illustrated in Figures 1 and 2 allows a superposition of two superlattices to be obtained. In addition, the process may be repeated to stack an arbitrary number of superlattices. Thus, the critical epitaxy thickness may be exceeded: each of the superlattices considered individually may respect this thickness so as to be formed from high-quality layers, and stacking them allows an assembly of superlattices exceeding the critical thickness to be obtained while maintaining the quality of their constituent layers. When the stacked superlattices have similar characteristics in respect of the layers forming them (nature, dimensions), it is possible to consider them to form a single superlattice, the thickness of which will potentially exceed the critical epitaxy thickness.

Forming the constituent layers of the superlattices by epitaxy requires the crystal structure to be reproduced from one layer to the next, and hence the layers Ch1 (or Ch2) and Sac1 (or Sac2), which are for example made of Si and SiGe, respectively, have the same crystal structure. Usually it is not possible to grow a semiconductor layer having characteristics that are acceptable for forming transistors epitaxially on an amorphous layer. Specifically, such a layer is unsuitable for epitaxy of a crystalline semiconductor layer of good quality. The bonding layer obtained by the layer transfer of the process according to the invention indeed makes it possible to join two superlattices formed from semiconductor layers of sufficient quality to produce transistors for commercial applications.

Furthermore, the bonding layer may be tailored (composition, thickness of the layer or layers forming it) to the intended use of the stacked superlattices. In particular, the bonding layer may be removed in a subsequent operation of

removing the sacrificial layers by virtue of an appropriate choice of the nature and thickness of its constituent layers.

The bonding layer between the two superlattices is continuously formed in a plane parallel to the upper surface of the substrate bearing it, covering substantially the entire surface of the substrate.

The carrier substrate Car and the donor substrate Don may comprise any semiconductor. Apart from silicon, the semiconductor may be germanium (GE), a silicon-germanium alloy (SiGe), silicon carbide (SiC), silicon-germanium carbide (SiGeC), III-V compound semiconductors or II-VI compound semiconductors, or it is possible to use SOI substrates (SOI standing for silicon-on-insulator) and more generally any type of semiconductor substrate comprising a layer of buried or surface dielectric. Such a dielectric layer may be used as an etch-stop layer when forming structures on the back side (same side as the carrier substrate Car) of the structure obtained by the process illustrated in Figures 1 and 2, or, in the case where it is located on the surface, as insulation in order to prevent latch-up of an integrated circuit fabricated based on this structure.

The layers Ch1 and Ch2 may be formed, for example, from silicon or from a III-V compound semiconductor. The layers Sac1 and Sac2 may be formed, for example, from silicon-germanium alloys (generically designated SiGe). The layers Ch1 and Ch2 may have the same composition in both superlattices Stck1 and Stck2, and likewise, the layers Sac1 and Sac2 may have the same composition $Si_{1-x}Ge_x$ in both superlattices Stck1 and Stck2. This last point makes it possible to remove the sacrificial layers Sac1 and Sac2 in the same step.

Alternatively, the superlattices Stck1 and Stck2 may have different natures and/or orientations. The orientation of the second superlattice relative to the first superlattice is defined in the joining step. The layers Sac1 and Sac1₀ (and

Ch1) on the one hand, and the layers Sac2 and Sac2₀ (and Ch2) on the other hand, may for example have different orientations, for example having crystallographic axes offset by 45°. It is also possible to consider using strained silicon, silicon-germanium alloys (SiGe) or germanium for the channel layers of either or both of the superlattices. When the two superlattices comprise silicon-germanium alloys, the proportions of germanium in the alloy may be the same or different in the two superlattices. Of course, the nature and characteristics of the sacrificial layers Sac1 and Sac2 must be tailored to those of the layers Ch1 and Ch2.

Likewise, the numbers of channel layers and sacrificial layers in the two superlattices may be the same, respectively, or may be different.

Second embodiment

A second embodiment of the present invention is described by means of Figures 3, 7, 8 and 9 and the associated description below.

In the first embodiment, the two superlattices Stck1 and Stck2 illustrated in Figure 3 are formed separately on two respective substrates, then the second superlattice Stck2 is transferred to the first superlattice Stck1. The second embodiment differs from this first embodiment in that instead of transferring a second superlattice to the first superlattice Stck1, a seed layer Init is transferred to the first superlattice Stck1, then the second superlattice Stck2 is formed on this seed layer Init by epitaxy. The seed layer Init is then integrated into the second superlattice Stck2. Apart from this aspect, reference may be made to the description of the first embodiment, the same elements and the same steps being identified by the same references. In particular, the structures obtained by the fabrication

processes of the two embodiments are conjointly illustrated in Figure 3.

Figures 7, 8 and 9 illustrate a process 900 for fabricating the structures Strc and Strc' of Figure 3, this process being based on sequential fabrication of the two superlattices Stck1, the second superlattice Stack2 being formed directly on the first superlattice Stck1. Figure 9 is a flowchart schematically showing the steps of the fabrication process 900.

Below, only the steps that differ from the corresponding steps of the first embodiment will be described. The steps 610_{car}, 620_{car}, 640_{Don}, 660, and 670A and their sequences remain unchanged in this second embodiment.

A step 910_{Don} replaces step 610_{Don}: before the seed layer Init is formed in the following step 920_{Don}, it is possible to form, on the donor substrate Don, the layer Stp of the first silicon-germanium alloy of formula $\text{Si}_{1-x}\text{Ge}_x$ having a thickness between 5 and 10 nm, then a protective silicon layer Cap2' having a thickness between 1 and 5 nm. These two layers are etch-stop layers and are intended to protect the integrity of the layer Init during the fabrication steps that come after the donor substrate has been split as described below and illustrated in (B) and (C) of Figure 8.

A step 920_{Don} replaces step 620_{Don}: instead of forming a superlattice on the donor substrate, a seed layer Init is formed. It may be a layer of the same nature and characteristics as one of the sacrificial layers Sac2. Figure 7 illustrates in (A), (B) and (C) how the fabrication process progresses after steps 620_{car}, 930_{Don} and 640_{Don}, respectively.

The step 930_{Don} is substantially identical to the step 630_{Don}. Simply put, instead of forming the layer Cap2 on a second superlattice, this layer Cap2 is formed on the seed layer Init.

The following steps are unchanged until step 970, which replaces step 670 of the first embodiment. This step is substantially identical to step 670, except that step 670B is replaced by a step 970B in which the seed layer Init is uncovered and revealed. Figure 8 illustrates in (C) the structure illustrated in (B) after it has been subjected to mechanical and/or chemical attacks to remove the part Don_a of the donor substrate Don, the etch-stop layer Stp, and the protective layer Cap2' in step 970B. Thus, the seed layer Init is uncovered in this step, and accessible in the remainder of the fabrication process.

The fabrication process ends with the implementation of a step 980 of forming the second superlattice Stck2 by epitaxy. In a preliminary step, in a thin-film deposition tool, any native oxide is removed from the surface of the layer Init by virtue of the "in-situ" etching function available in many epitaxy tools. This operation makes it possible to clean the layer Init and guarantee the quality of its surface, in order to ensure the quality of the growth of the layers deposited on it. The second superlattice Stck2 is then formed directly on the seed layer Init, in a step 980, according to the modalities described for step 620_{Don}, the seed layer Init being considered as one of the sacrificial layers Sac2 of the second superlattice Stck2 and as the layer on which the epitaxial growth begins. Layers Ch2 are thus successively formed in alternation with layers Sac2.

The operation of cleaning the layer Init prior to layer deposition is conventional and considered to form part of the step of forming the layers Ch2 and Sac2 by epitaxy. Alternatively, other known methods for cleaning the surface of the layer Init could be envisaged, such as complete oxidation of the layer Cap2' and its removal by HF directly in the tool. The main thing is to obtain a clean, non-oxidised surface before proceeding with the deposition of thin layers on this

surface, whether the deposition sequence is started with a layer Sac2 or a layer Ch2. Following this step, either of the structures illustrated in Figure 3 are obtained.

The above embodiments implemented, by way of example, associations between layers of silicon in alternation with layers of silicon-germanium alloy, to form the first superlattice and the second superlattice. However, the invention is not limited to this particular case, and could be applied for example (i) to superlattices made up of layers of germanium in alternation with layers of a silicon-germanium alloy, (ii) to superlattices made up of layers formed from a first silicon-germanium alloy having a germanium content for example lower than 20% in alternation with layers formed from a second silicon-germanium alloy having a high germanium content, for example higher than 75%, (iii) to superlattices having layers of different crystallographic orientations, or (iv) to superlattices comprising layers of III-V semiconductors

The embodiments described above relate to an association of superlattices intended to form transistors, and more specifically nanosheet transistors or CFETs. However, the scope of the invention extends beyond this field and comprises combination of superlattices in general, not only in the field of semiconductors.

The invention is not limited to the embodiments described above, and variants may be employed without departing from the scope of the invention as defined by the claims.

CLAIMS

1. Process (600; 900) for fabricating a structure (Strc, Strc') comprising at least one superlattice, comprising the
5 steps of:

- forming (610_{Car}) a first superlattice (Stck1) on a first substrate (Car), by stacking a plurality of first channel layers (Ch1) in alternation with a plurality of first sacrificial layers (Sac1);

- forming (620_{Car}) a first cap layer (Cap1) on the first superlattice (stck1);

- forming (620_{Don}; 920_{Don}) at least one second sacrificial layer (Stck2; Init) on a surface (S_{Don}) of a second substrate (Don);

- forming (630_{Don}; 930_{Don}) a second cap layer (Cap2) on the at least one second sacrificial layer (Stck2; Init);

- forming (640_{Don}) a weakening plane (Imp) in the carrier substrate by implanting ions of a light species into the donor substrate (Don) through the surface (S_{Don}) of the second
20 substrate (Don), at least one second sacrificial layer (Stck2; Init) and the second cap layer (Cap2);

- joining (660) the at least one sacrificial layer (Stck2; Init) to the first superlattice (Stck1) by placing the second cap layer (Cap2) in contact with the first cap layer (Cap1),
25 which together form a bonding layer (Bnd), the first superlattice (Stck1), the bonding layer (Bnd) and the at least one sacrificial layer (Stck2; Init) being stacked in this order; and

- splitting (670A) the donor substrate (Don) in the
30 weakening plane (Imp) and withdrawing part (Don_b) of the donor substrate (Don) after the joining step (660),

wherein the first cap layer (Cap1) and the second cap layer (Cap2) each have a thickness of less than 2 nm.

2. Process (600) according to Claim 1, wherein the step of forming at least one second sacrificial layer on the second substrate (Don) consists in forming (620_{Don}) a second superlattice (Stck2) by stacking a plurality of second channel layers (Ch2) in alternation with a plurality of second sacrificial layers (Sac2).

3. Process (900) according to Claim 1, wherein the step of forming at least one second sacrificial layer (Stck2) on the second substrate (Don) consists in forming (920_{Don}) a seed layer (Init), the process further comprising a step (980) of forming a second superlattice (Stck2) on the seed layer (Init) after the joining step (660), by stacking a plurality of second channel layers (Ch2) in alternation with a plurality of second sacrificial layers (Sac2).

4. Process according to any one of Claims 1 to 3, wherein the bonding layer (Bnd) is continuously formed in a plane parallel to a surface (S_{Car}) of the first substrate (Car) on which the first superlattice (Stck1) is formed.

5. Process according to any of Claims 2 to 4, wherein:

- the first channel layers (Ch1) and the second channel layers (Ch2) are each formed from a semiconductor material, and

- the first sacrificial layers (Sac1) and the second sacrificial layers (Sac2) are each formed from a material that is liable to have a faster etch rate than the first channel layers (Ch1) and the second channel layers (Ch2), respectively.

6. Process according to Claim 5, wherein the sacrificial layers (Sac1₀, Sac2₀) in direct contact with the bonding layer (Bnd) each have a thickness (t_{Sac10}, t_{Sac20}) equal to or less than

half the thicknesses (t_{Sac} , t_{Sac}) of the other sacrificial layers (Sac1, Sac2).

7. Process according to any of Claims 1 to 6, further comprising a step of removing (670A) at least one part (Don_b) of the second substrate (Don) after the joining step (660).

8. Process according to Claim 7, further comprising a step of uncovering (670B) a channel layer (Ch2) of the second superlattice (Stck2) after the step of withdrawing (670A) the second substrate (Don).

9. Process according to any of Claims 1 to 8, wherein the first cap layer (Cap1) and the second cap layer (Cap2) are each formed from silicon.

10. Process according to Claim 9, wherein one of the first cap layer and the second cap layer is formed from amorphous silicon and the other is formed from crystalline silicon.

11. Process according to Claim 3, further comprising a step of forming (610_{Don}) at least one etch-stop layer (Stp) on the second substrate (Don) prior to forming the seed layer (Init).

12. Process according to Claim 11, wherein the at least one etch-stop layer comprises a layer (Stp) of the same material as the seed layer (Init).

13. Process according to any of Claims 1 to 12, wherein:

- the first channel layers (Ch1) are formed from silicon;
- the first sacrificial layers (Sac1) are formed from a first silicon-germanium alloy;

- the first cap layer (Cap1) is formed on and in direct contact with one of the sacrificial layers (Sac1) of the first superlattice;
- the second sacrificial layer (Stck2; Init) is formed from a second silicon-germanium alloy;
- the second cap layer (Cap2) is formed on and in direct contact with the at least one second sacrificial layer (Stck2; Init); and
- the first cap layer (Cap1) and the second cap layer (Cap2) are each formed from silicon.

14. Structure (Strc, Strc') for a superlattice stack, comprising:

- a carrier substrate (Car);
 - a first superlattice (Stck1) on the carrier substrate;
 - a bonding layer (Bnd) on the first superlattice (Stck1), said bonding layer being formed from a first cap layer (Cap1) and from a second cap layer (Cap2); and
 - a second superlattice (Stck2) on the bonding layer (Bnd),
- wherein:
- the first superlattice is formed from a stack of a plurality of first channel layers (Ch1) formed from silicon in alternation with a plurality of first sacrificial layers (Sac1) formed from a first silicon-germanium alloy;
 - the second superlattice is formed from a stack of a plurality of second channel layers (Ch2) formed from silicon in alternation with a plurality of second sacrificial layers (Sac2) formed from a second silicon-germanium alloy;
 - the first cap layer (Cap1) and the second cap layer (Cap2) are each formed from silicon, in direct contact with one of the respective sacrificial layers of the first superlattice and of the second superlattice, and each have a thickness of less than 2 nm.

15. Structure for a superlattice stack according to Claim 14, wherein the bonding layer (Bnd) is continuously formed in a plane parallel to a surface (S_{Car}) of the carrier substrate (Car) bearing the first superlattice (Stck1).

5

16. Structure for a superlattice stack according to Claim 14 or 15, wherein:

- the first channel layers (Ch1) and the second channel layers (Ch2) are each formed from a semiconductor material,
10 and

- the first sacrificial layers (Sac1) and the second sacrificial layers (Sac2) are each formed from a material that is liable to have a faster etch rate than the first channel layers (Ch1) and the second channel layers (Ch2),
15 respectively.

17. Structure for a superlattice stack according to any of Claims 14 to 16, wherein one of the first cap layer (Cap1) and the second cap layer (Cap2) is formed from crystalline silicon
20 and the other of the first cap layer (Cap1) and the second cap layer (Cap2) is formed from amorphous silicon.

18. Structure according to any of Claims 14 to 17, wherein the sacrificial layers ($Sac1_0$, $Sac2_0$) in direct contact with the
25 bonding layer (Bnd) each have a thickness (t_{Sac1_0} , t_{Sac2_0}) equal to or less than half the thicknesses (t_{Sac} , t_{Sac}) of the other sacrificial layers ($Sac1$, $Sac2$).