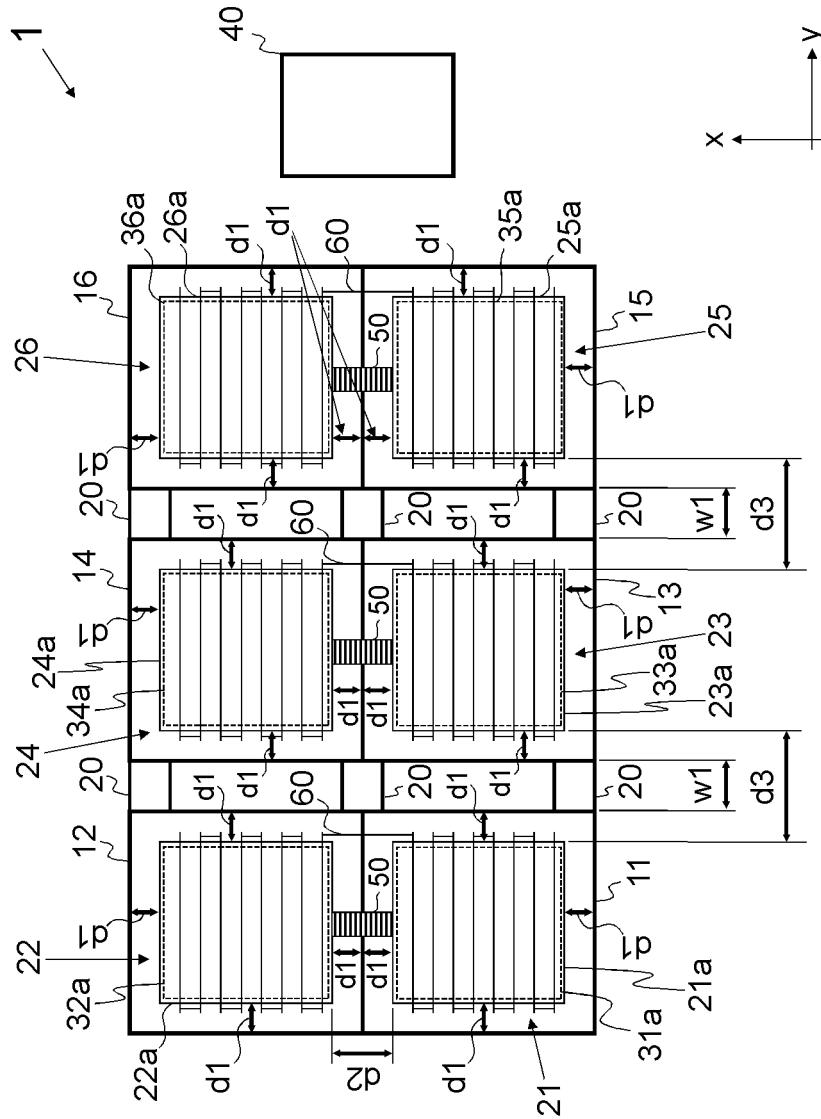




[図2]







[図5]

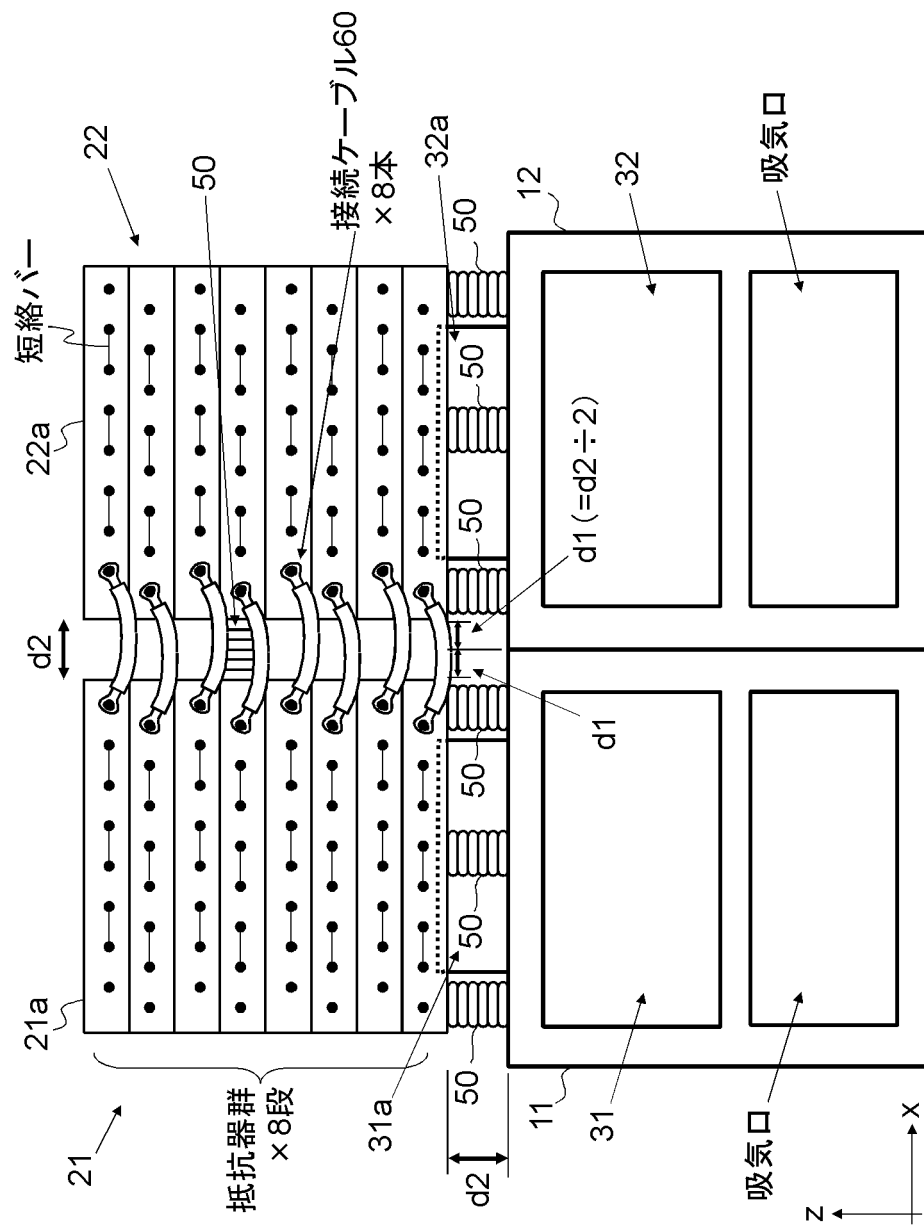
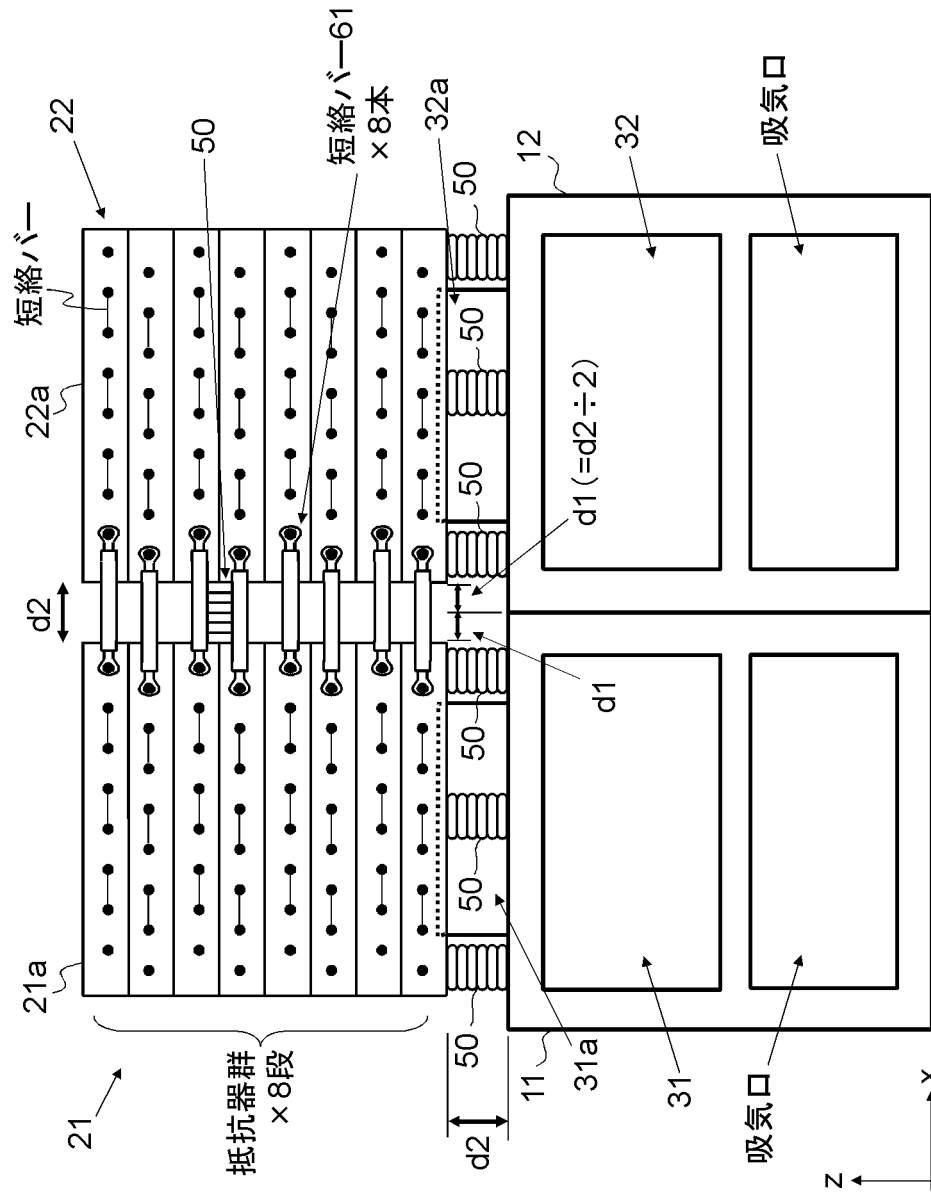


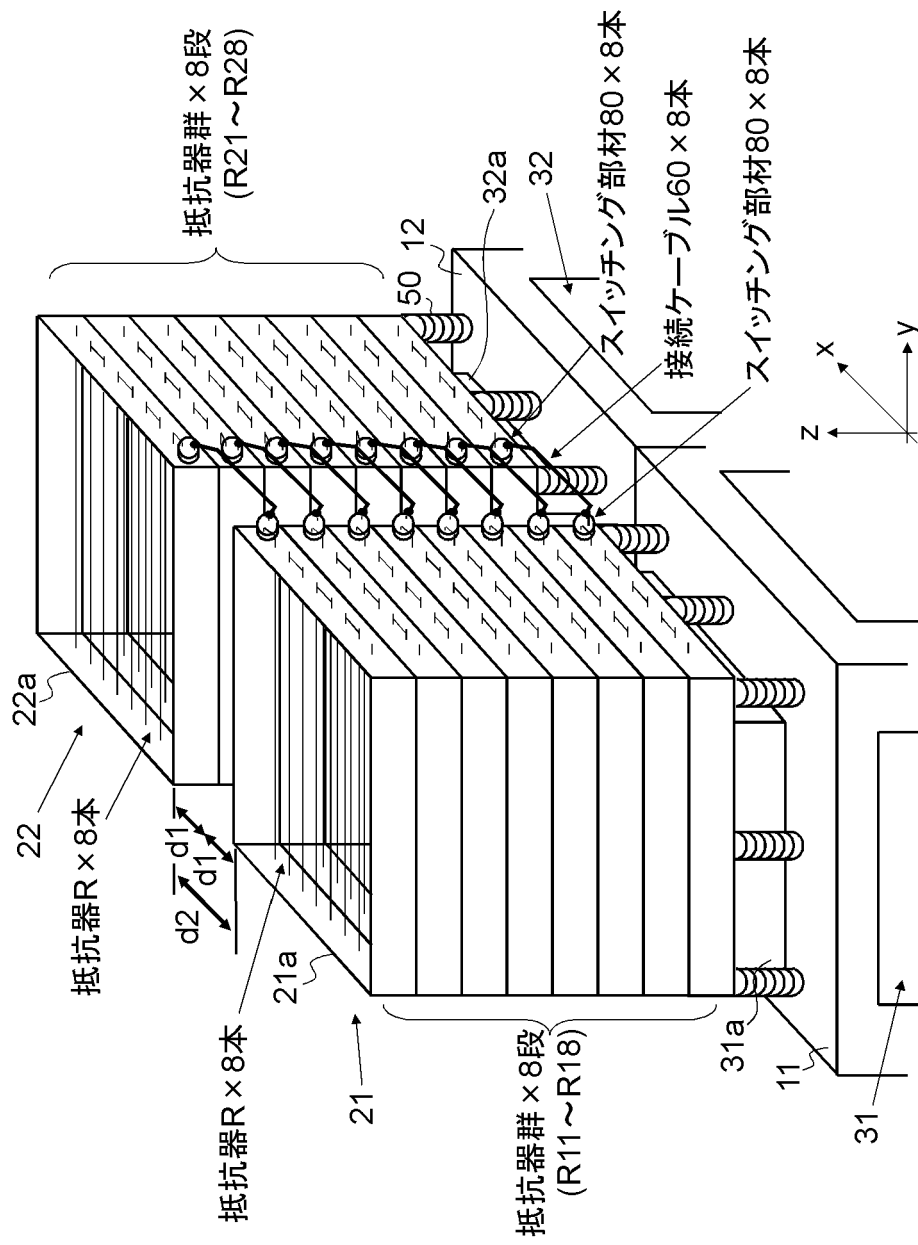


Figure 1 is a plan view of a semiconductor device 1. The device is defined by a boundary 1. It features a central region 20 containing three vertical strips of semiconductor material 22, 24, and 26. Each strip is divided into three sections 22a, 24a, and 26a. The strips are separated by insulating regions 21, 23, and 25. The strips are connected to a common bus 20. The device is mounted on a substrate 40. A coordinate system (x, y) is shown in the upper right corner.

[図8]

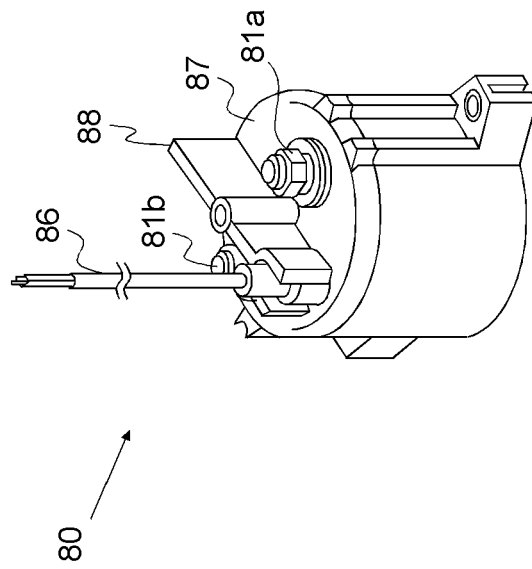


[図9]

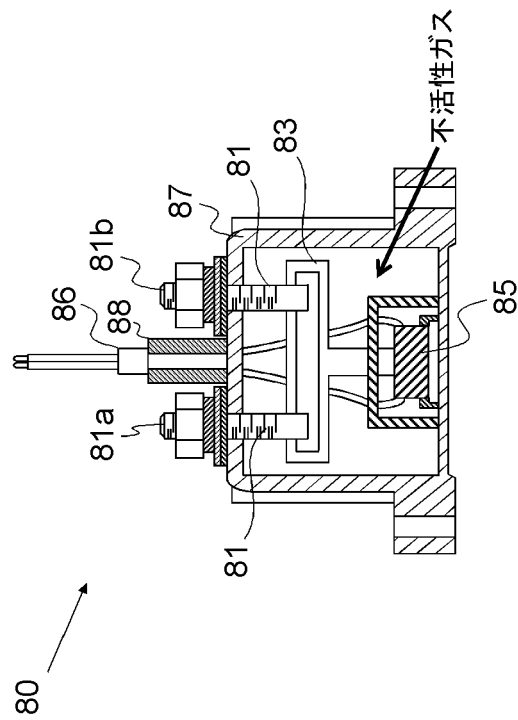




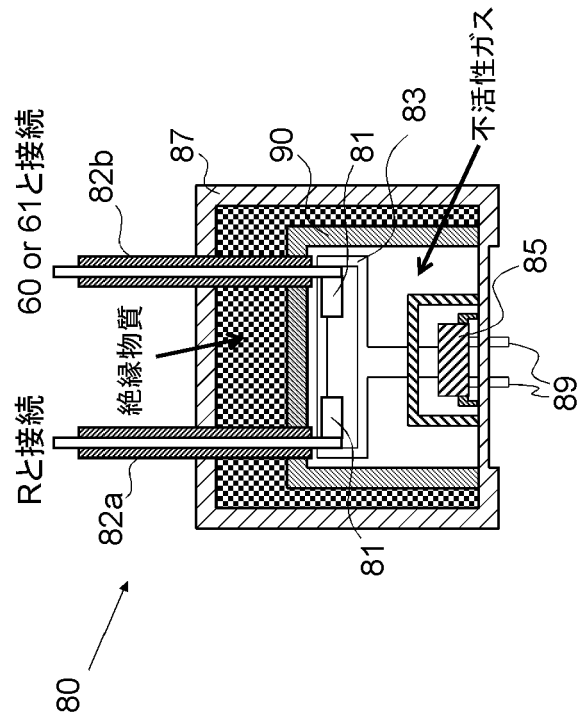
[図11]



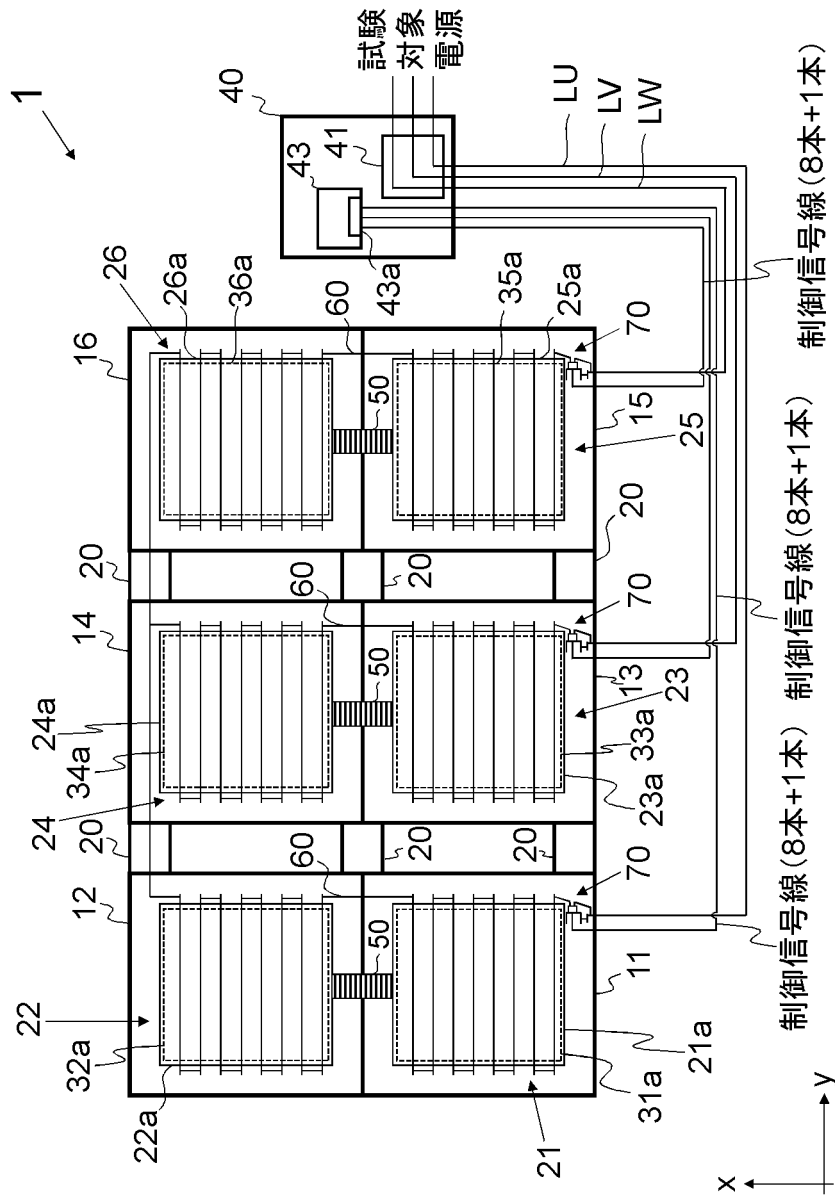
[図12]



[図13]



[図14]



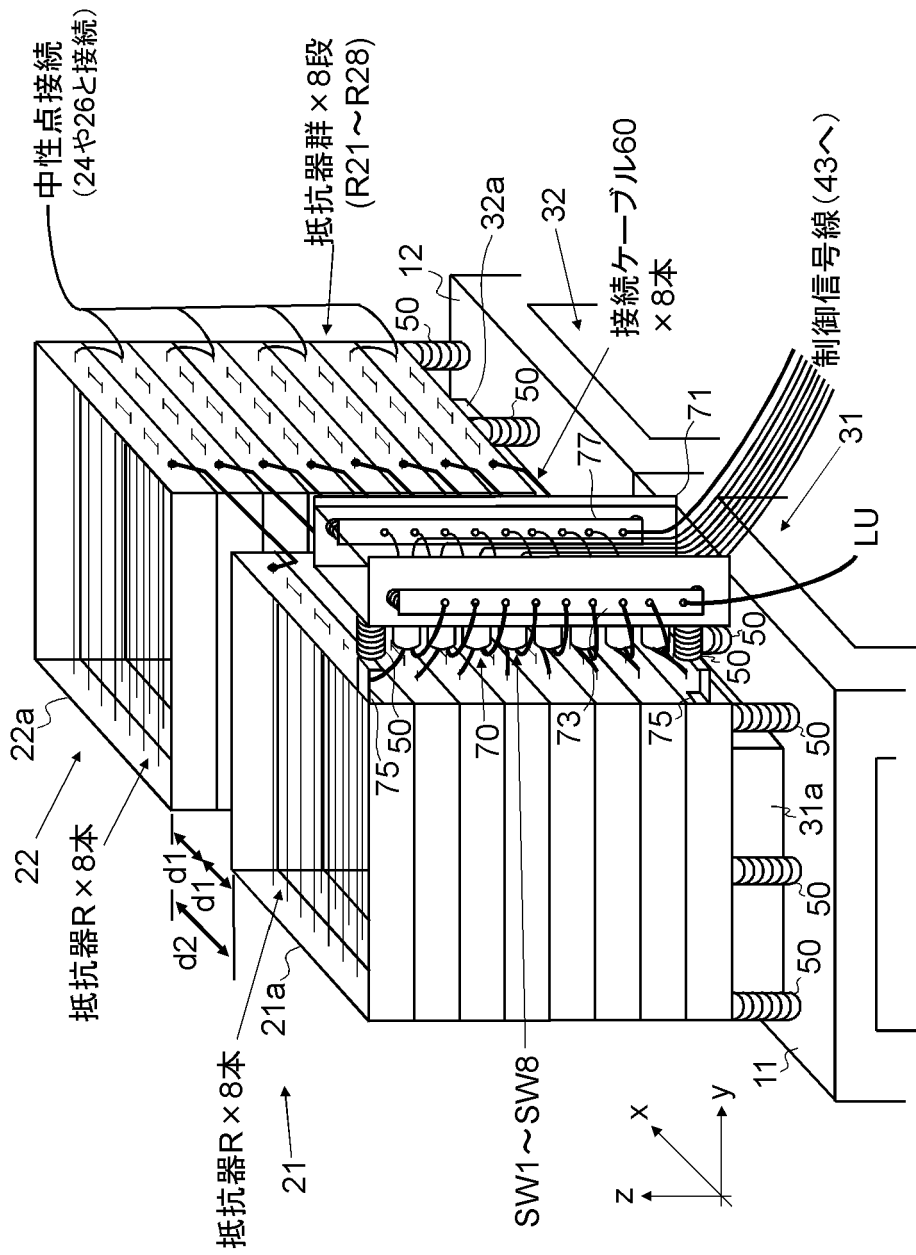






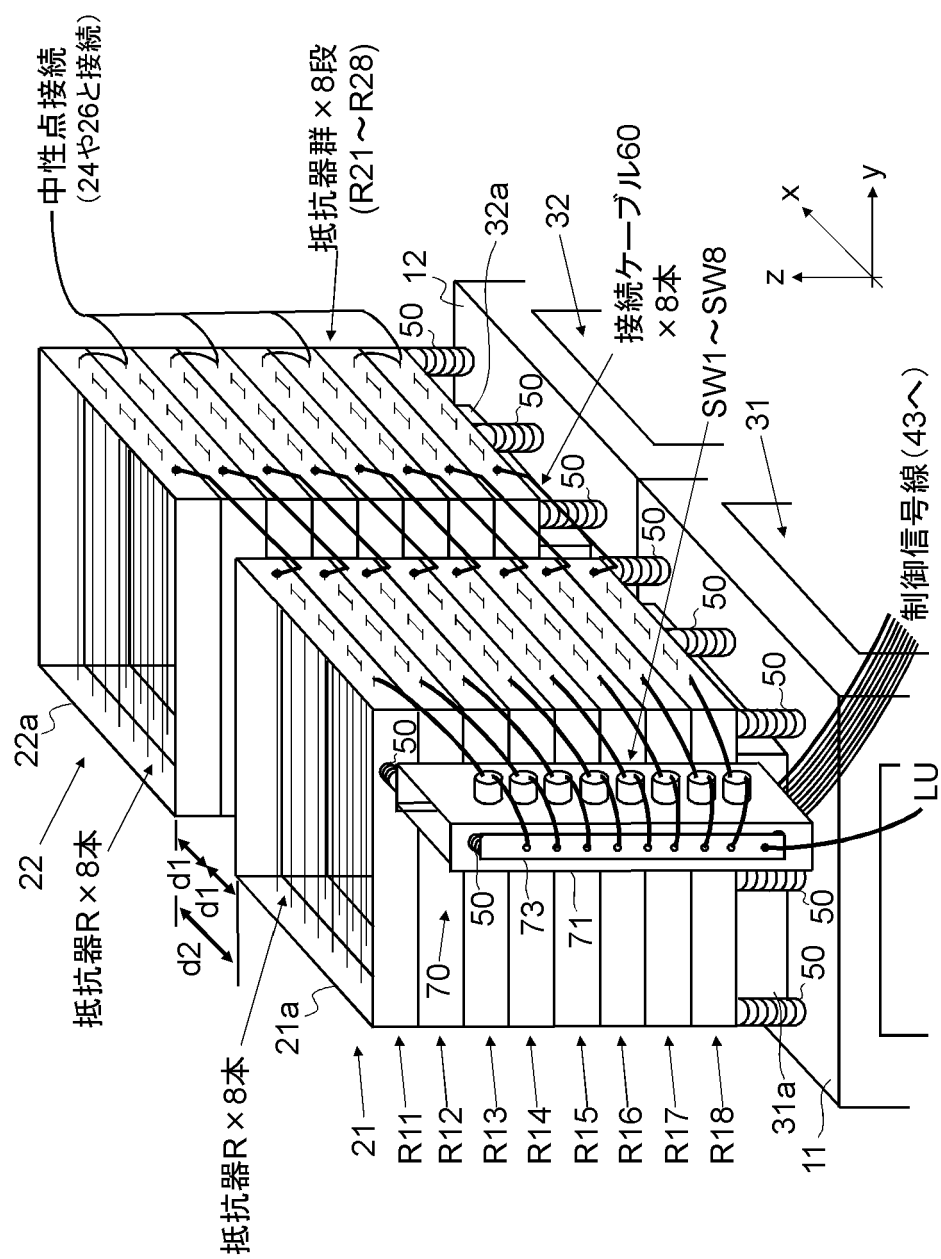


[図19]



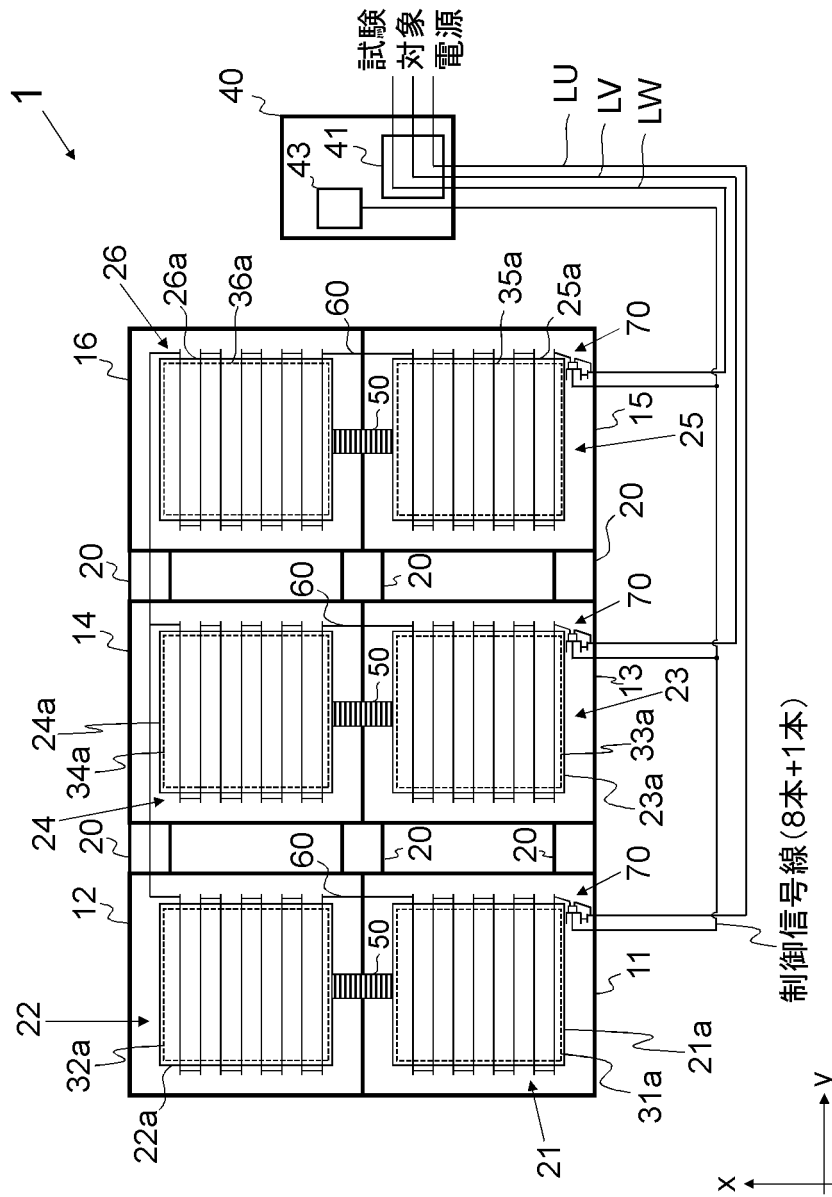


[図21]



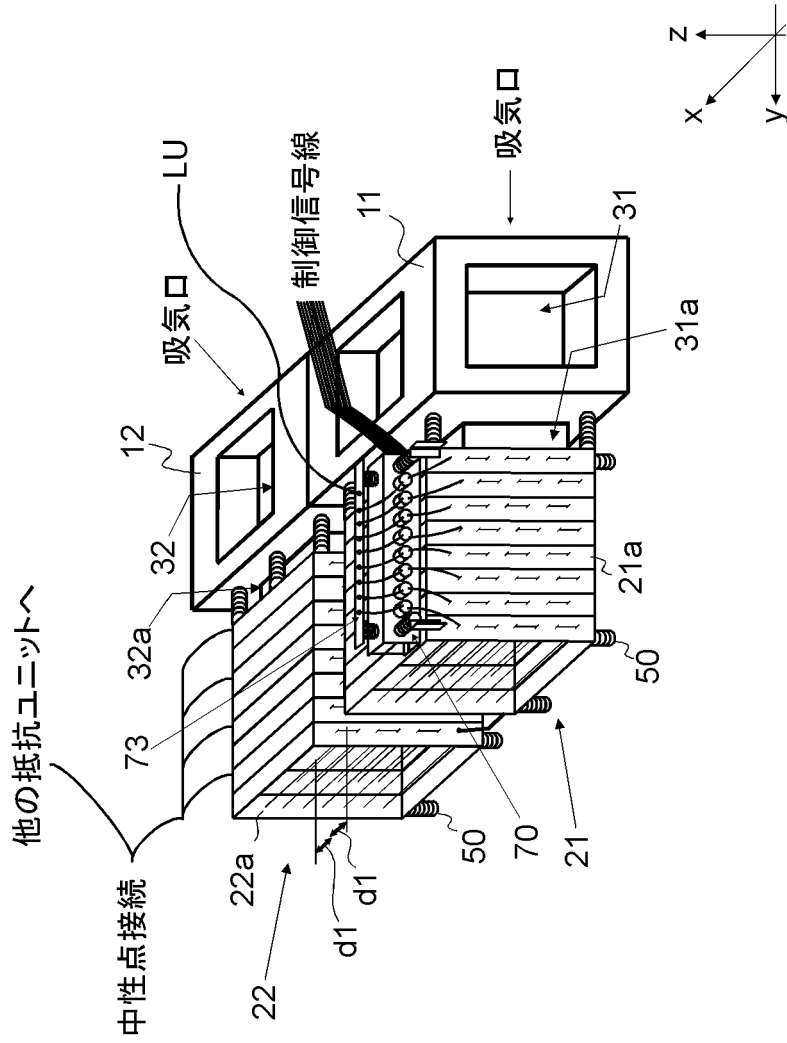


[図23]

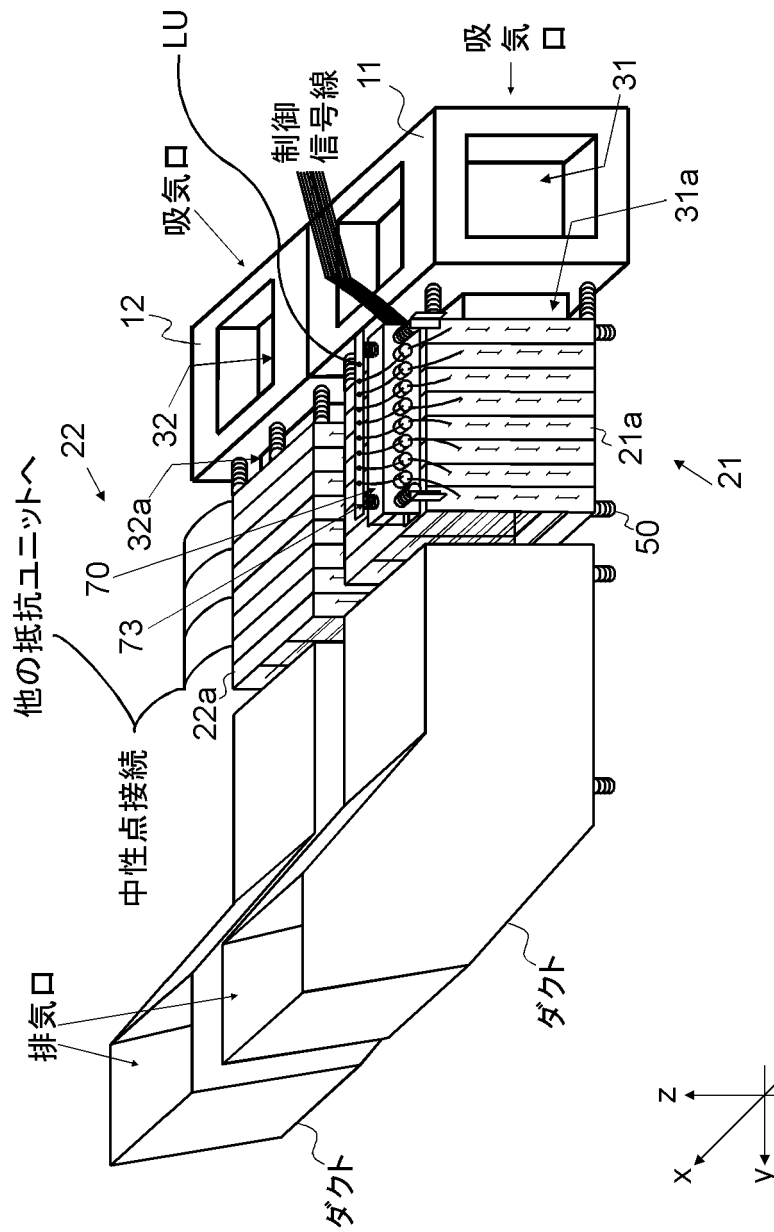




[図25]



[図26]



[図27]

