Claims

1. Method for treatment of a product wafer temporarily bonded on a carrier wafer with the following steps:

- bonding a processed side of the product wafer to the carrier wafer,
- grinding and/or backthinning of the product wafer on one flat side facing away from the carrier wafer to a product wafer thickness D of < 150 μm, especially < 100 μm, preferably < 75 μm, even more preferably < 50 μm, especially preferably < 30 μm, and
- surface treatment of the flat side with means for reducing an especially structural intrinsic stress of the product wafer.

2. Method as claimed in Claim 1, wherein surface treatment takes place in an independent process which is separated, especially in space, from backthinning.

3. Method as claimed in one of Claims 1 or 2, wherein the means for reducing the intrinsic stress are characterized by at least one of the following features:

- dry polishing of the flat side
- wet etching of the flat side
- dry etching of the flat side.

4. Method as claimed in one of the preceding claims, wherein the intrinsic stress of the product wafer can be set by the means for reducing the intrinsic stress.

5. Method as claimed in one of the preceding claims, wherein the carrier wafer, especially at a certain and/or over a temperature range of the temperature of the carrier wafer has a coefficient of expansion which is essentially identical to the coefficient of expansion of the product wafer.

6. Method as claimed in one of the preceding claims, wherein the product wafer with its contact side which is opposite the flat side is temporarily connected to the carrier wafer using an at least in part, especially predominantly, thermoplastic adhesive.

7. Method as claimed in one of the preceding claims, wherein the means for reducing the intrinsic stress are made such that they remove at least partially a defined layer thickness S of a crystal structure of the flat side which has been damaged especially by grinding and/or backthinning.

8. Method as claimed in one of the preceding claims, wherein the intrinsic stress of the product wafer is set by the means for reducing the intrinsic stress such that the product wafer arches toward the carrier wafer during a following thermal process.

9. Method as claimed in Claim 6, wherein the product wafer of the contact side has topographies which are embedded into the adhesive.

10. Method as claimed in one of the preceding claims, wherein after surface treatment a thermal process step follows especially at temperatures > 50°C, preferably > 75°C, preferably > 100°C.

11. Method as claimed in one of the preceding claims, wherein the thermal method step is an especially chemical gas phase deposition method step.

12. Method as claimed in Claim 7, wherein the layer thickness is S < 10 μm, especially < 5 μm, preferably < 3 μm, even more preferably < 1 μm, especially preferably < 0.5 μm.

13. Device for treatment of a product wafer temporarily bonded on a carrier wafer with the following features:

- means for bonding a processed side of the product wafer to the carrier wafer,
- means for grinding and/or backthinning of the product wafer, and
- means for reducing an especially structural intrinsic stress of the product wafer.

14. Device for executing a method as claimed in one of claims 1 to ~~11~~12.