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RECORDING/REPRODUCING APPARATUS, RECORDING METHOD, AND RECORDING/REPRODUCING METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to recording/reproducing apparatuses, recording methods and recording/reproducing methods, and in particular, to a recording/reproducing apparatus, a recording method and a recording/reproducing method which are capable of reproducing high-quality images when performing reproduction at an N-fold speed.

2. Description of the Related Art

In an analog videocassette recorder, an image signal is recorded on tracks in units of fields. In the normal reproducing mode, sequential reproduction from the field unit tracks is performed to reproduce normal moving pictures.

In addition, in reproduction (variable speed reproduction) at an N-fold speed, such as a double speed or a triple speed, reproduction from N tracks is performed during the period of one field. Accordingly, when N-fold speed reproduction is performed, images locally reproduced from the tracks are combined, which generates much noise, so that high quality images cannot be reproduced.

Conversely, for example, on an analog videodisc one

frame (two fields) of image data is recorded for one rotation. Thus, even when N-fold speed reproduction from the videodisc is performed, high quality images with less noise can be obtained by performing complete reproduction from the desired field or frame.

Accordingly, by recording video signals not on a magnetic tape but on a disc like a hard disc or an optical disc, images with less noise can be obtained even if the N-fold speed reproduction is performed because reproduction at an arbitrary position, which is random access, can be performed on the disc.

Concerning the recording media such as the hard disc and the optical disc, their standard is not determined on the assumption that a video signal is recorded. A sector as the unit of recording to or reproduction from the media does not correspond to a frame or field. Thus, the recording media have a problem in which, when variable speed reproduction is performed, the calculation for finding the address of the start frame is complicated and the operation consumes much time.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a recording/reproducing apparatus, a recording method and a recording/reproducing method in which address

calculation in variable speed reproduction can be easily performed, whereby facilitating variable speed reproduction.

To this end, according to an aspect of the present invention, the foregoing object has been achieved through provision of a recording/reproducing apparatus for recording data on a disc recording medium in units of sectors, and reproducing the recorded data, the recording/reproducing apparatus including recording control means for performing control so that the start of predetermined units of a coded video signal is recorded at the start of one of the sectors of the disc recording medium.

Preferably, the recording control means performs further control so that the predetermined units of the coded video signal are recorded in m consecutive sectors, being a data recording region.

The predetermined units may be frames, and the recording control means may perform control so that the start of the frames of the coded video signal is recorded at the start of one of the sectors of the disc recording medium.

According to another aspect of the present invention, the foregoing object has been achieved through provision of a recording method for recording a coded video signal in units of sectors on a disc recording medium, in which the start of predetermined units of a coded video signal is recorded at the start of the sectors of the disc recording

medium.

Preferably, the predetermined units of the coded video signal are recorded in m consecutive sectors being a data recording region, and dummy data is recorded in the section of a data recording region in which the predetermined number of units of the coded video signal are not recorded.

According to a further aspect of the present invention, the foregoing object has been achieved through provision of a recording/reproducing method for recording on a disc recording medium a video signal coded in units of sectors, and reproducing the recorded coded video signal, in which the recording/reproducing method controls recording so that the start of predetermined units of the coded video signal is recorded at the start of the sectors of the disc recording medium, and the predetermined units of the coded video signal are recorded in m consecutive sectors, and the recording/reproducing method controls reproduction so that, when the recorded coded video signal is reproduced at a speed N times the normal speed, a value obtained by adding m × N to a readout-start sector number for reproducing the L-th predetermined unit of the coded video signal is used as a readout-start sector number for reproducing the (L+1)-th predetermined unit of the coded video signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an example of a recording/reproducing apparatus to which an image data reproducing apparatus of the present invention is applied.

Fig. 2 is a chart showing the structure of a packet in an IEEE 1394 bus.

Fig. 3 is a chart showing the condition of image data recorded on the hard disc in Fig. 1.

Fig. 4 is a flowchart illustrating the operation of the recording/reproducing apparatus in Fig. 1.

Fig. 5 is a flowchart illustrating the details of a readout sector calculating process in step S2 in Fig. 4.

Fig. 6 is a flowchart illustrating the details of an updating timing determination process in step S3 in Fig. 4.

Fig. 7 is a timing chart illustrating the operation of the example in Fig. 1 when it performs variable speed reproduction.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a recording/reproducing apparatus according to an embodiment of the present invention. A digital video cassette recorder (DVCR) 2 is connected to this recording/reproducing apparatus 1 via an Institute of Electrical and Electronics Engineers (IEEE) 1394 bus. A monitor 3 is also connected to the DVCR 2.

The recording/reproducing apparatus 1 includes a hard

disc drive (HDD) 11, to which or from which image data is recorded or reproduced. An integrated drive electronics (IDE) controller 12 is used to control recording to or reproduction from the hard disc drive 11. A first-in first-out unit (FIFO) 13 is used as a buffer in which data supplied from the IDE controller 12 is temporarily stored and output to a LINK 14, while it is used as a buffer in which image data supplied from the LINK 14 is temporarily stored and output to the IDE controller 12. The LINK 14 transforms the image data supplied from the LINK 14 to packets having an isochronous mode before outputting the packets to a PHY 15, and de-packets image data supplied from the PHY 15 before outputting it to the FIFO 13.

The PHY 15 performs data-strobe(DS)-coding modulation/demodulation. In other words, the PHY 15 performs the DS-coding of the packet data supplied from the LINK 14, and outputs the DS-coded data to a 1394 terminal 16. The PHY 15 also performs the DS-coding demodulation of data supplied from the 1394 terminal 16, and outputs the demodulated data to the LINK 14.

The PHY 15 outputs the packets supplied from the LINK 14 as packets having the IEEE 1394 isochronous mode from the 1394 terminal 16 to the DVCR 2 via the IEEE 1394. A CPU 17 is used to control the operations of the IDE controller 12, the FIFO 13, the LINK 14, the PHY 15, etc. An operation

unit 18 is used to output signals corresponding to operations by a user to the CPU 17.

Next, the operation of the CPU 17 will be described. By controlling the operation unit 18 to command recording, the CPU 17 executes, for example, the process of recording to the hard disc drive 11 image data supplied from the DVCR 2 via the IEEE 1394 bus.

In other words, in this case, image data in the form of IEEE 1394 isochronous mode packets is input from the DVCR 2 via the IEEE 1394 bus. The image data is input to the PHY 15 via the 1394 terminal 16. The PHY 15 performs the DS-coding demodulation of the image data before supplying the demodulated data to the LINK 14. The LINK 14 de-packets the input image data packets to extract image data excluding a header portion, and supplies it to the FIFO 13 for temporary storage. The IDE controller 12 properly reads the image data stored in the FIFO 13, and supplies the read image data to the hard disc drive 11 for recording.

Fig. 2 shows the structure of an IEEE 1394 isochronous data-block packet. That is, as shown in Fig. 2, in the IEEE 1394 isochronous data-block packet are set firstly an 8-byte 1394 isochronous packet header and secondarily an 8-byte common isochronous packet (CIP) header. Subsequently thereto, a DVCR standard definition (SD) data block is set. This data block is composed of six blocks, and one block is

80 bytes in length. Accordingly, the total length of the data block is 480 bytes. Next to the data block, a 4-byte CRC as an error correcting code is set. The whole is 500 bytes in length.

The LINK 14 extracts only the DVCR SD data block in the packet, and supplies it to the hard disc drive 11 for recording.

In addition, in one block (80 bytes) among 25 data blocks (among 150 (= 25 × 6) blocks), image data is not set but control data including a time stamp is set, and image data is set in the remaining 149 blocks. The control data is extracted by the LINK 14 before is supplied to the CPU 17.

In the case of an NTSC method, one frame of image data is transmitted with ten data blocks. In other words, as described above, control data is set in the ratio of one to 150 blocks. Thus, one frame of image data is transmitted with 1490 (= 1500 - 10) blocks (119200 (= 1490 × 80) bytes). The one-frame image data transfer amount as the data transfer amount of 1394 isochronous data-block packets themselves is 125000 bytes (= 500 × 25 × 10).

Concerning the hard disc drive 11, data is recorded or reproduced in units of sectors. The capacity of one sector is 512 bytes. Therefore, for example, the number of sectors necessary for recording one frame (119200 bytes) of image data based on the NTSC method is 232.8 (= 119200/512).

Image data can be sequentially recorded to the hard disc drive 11, with 232.8 sectors for one frame used as one unit. This however complicates the process of calculating the start sector of the image data when variable-speed reproduction is performed. Accordingly, this recording/reproducing apparatus records the image data for one frame, using 256 sectors as one unit.

Fig. 3 shows the schematic condition that the image data is recorded to the hard disc drive 11 in the above manner. As shown in Fig. 3, the first one frame of image data is recorded in a total of 233 sectors from the 0th sector to the 232nd sector. In the 232nd sector the image data ends halfway, and from the position to the 255th sector is recorded dummy data. The second frame of image data is recorded from the 256th sector.

Recording is thereafter performed in the same manner. The start of the third frame of image data is the 512th sector, and the start of the fourth image data is the 768th sector.

Next, the reproducing operation will be described with reference to the flowchart shown in Fig. 4. When reproduction is commanded by operating the operation unit 18, the CPU 17 requests reproduction of image data from the hard disc drive 11 by controlling the IDE controller 12. When the IDE controller 12 receives this request and when reading

from the hard disc drive 11 is enabled, it outputs a reading-request interruption signal to the CPU 17. When the CPU 17 receives this reading-request interruption signal in step S1, it proceeds to step S2, in which it executes the process of calculating a readout sector. The details of the calculation of the readout sector are illustrated by the flowchart in Fig. 5.

Specifically, initially, in step S11, the CPU 17 determines whether single speed reproduction (reproduction at the normal speed) is commanded from the operation unit 18. If it has determined that the single speed reproduction is not commanded, it proceeds to step S12, in which it determines whether or not double speed reproduction is commanded. Thereafter, in the same manner, in steps S13 to S16, it determines whether the presently commanded reproducing speed is a triple, a 1/2-fold speed, a 1/3-fold speed, or a 0-fold speed (still picture reproduction).

In step S11 it has determined that the reproducing speed is a single speed, it proceeds to step S17, in which the value C of a calculating counter for calculating the position of a sector at which reading from the hard disc 17 is started is incremented by 256 × 1 by the CPU 17. The initial value of the counter value C is set at a value (e.g., 0) representing the sector in which the start of the first frame of the image data is recorded. Accordingly, in this

case, for example, numeral 0 is set as the counter value C.

Next, the CPU 17 proceeds to step S3 in Fig. 4, in which it determines whether or not it has timing for updating the value RC of a readout sector counter representing the number of a sector to be actually read. The details of this updating timing determination process are illustrated by the flowchart in Fig. 6.

In the flowchart in Fig. 6, initially, in step S31, the CPU 17 determines whether the presently set reproducing speed is either of a single speed to a triple speed. Since a single speed is set in the present case, the CPU 17 proceeds to step S34, in which it performs YES determination (namely, determining that it has updating timing).

Accordingly, it proceeds from step S3 to step S4 in Fig. 4 (since it has the updating timing), in which it performs the process of updating the value RC of the readout sector counter. In other words, in the present case, the calculating counter value C calculated in step S2 is zero. Thus, this value 0 is read and set as the sector counter value RC such that RC = 0. The CPU 17 proceeds to step S5, in which it requests the IDE controller 12 to read one frame (25 sectors) of image data from the sector having the numeral of the value RC set in the readout sector counter. Thereby, in this case, it is requested that the IDE controller 12 read sectors number 0 to 255. In response to

this request, the IDE controller 12 reproduces data recorded in sector number 0 to 255 to the hard disc drive 11.

The one frame of image data read from the hard disc drive 11 is supplied to the FIFO 13 by the IDE controller 12 so as to be stored.

Completion of reproducing the one frame of image data in the above manner causes the IDE controller 12 to output a reading-request interruption signal again to the CPU 17. When the CPU 17 receives this reading-request interruption signal in step S1 in Fig. 4, it executes the process of calculating a readout sector again in step S2.

Since the CPU 17 determines that the present reproducing speed is a single speed in step S11 in Fig. 5, it proceeds to step S17, in which the calculating counter value C is incremented by 265 × 1, and in this case, C = 256 (= 0 + 256 × 1).

Subsequently, it proceeds to step S3 in Fig. 4, in which it determines whether it has updating timing. Concerning this determination, YES determination (determining that it has updating timing) is performed in steps S31, S34 in Fig. 6, similarly to the above-described case.

Accordingly, in step S4 in Fig. 4, the re-readout sector counter value RC is updated with the calculating counter value C calculated in step S2. In other words, in

this case, RC = 256.

Subsequently, the CPU 17 proceeds to step S5, in which it outputs to the IDE controller 12 a command for requesting the IDE controller 12 to reproduce 256 sectors from sector number 256 (up to sector number 511). In response to this command, the IDE controller 12 reproduces the second frame of image data recorded in sectors from number 256 to 511.

The above-described reproduced image data is supplied to the FIFO 13 via the IDE controller 12, and is written therein.

Similar operations are repeatedly executed thereafter, whereby each frame of image data is sequentially reproduced, as shown as normal reproduction in Fig. 7.

When the image data supplied from the hard disc drive 11 via the IDE controller 12 is stored by three frames in the FIFO 13, the CPU 17 causes the LINK 14 to transfer the stored image data. When the image data stored in the FIFO 13 decreases less than three frames, the CPU 17 issues a read command to the IDE controller 12. In this manner, the CPU 17 performs control so that three frames of image data are always stored in the FIFO 13. This prevents interruption of an image due to the overhead of the hard disc drive 11.

The LINK 14 converts the image data supplied from the FIFO 13 to IEEE-1394-isochronous-mode packets, and outputs

it to the PHY 15. The PHY 15 performs the DS coding of this image data before outputting the DS coded data to the DVCR 2 from the 1394 terminal 16 via the IEEE 1394 bus.

The DVCR 2 converts the supplied image data to an analog video signal, and outputs it to the monitor 3 for display. In this manner, an image reproduced in the normal reproducing mode from the hard disc drive 11 is displayed on the monitor 3.

The DVCR 2 substantially ignores dummy data included in the image data supplied from the 1394 terminal 16 via the IEEE 1394 bus.

In addition, when double speed reproduction is commanded, the following operations are performed. That is, when the CPU 17 determines in step S12 in Fig. 5 that the present reproducing speed is a double speed, it proceeds to step S18, in which the calculating counter value C is incremented by 256 × 2. Also, in this case, the initial value C is set at zero. The calculating process in step S2 in Fig. 4 is performed, and in step S3, the determination process of updating timing is performed. In the determination process of updating timing, it is determined in step S31 in Fig. 6 that the present reproduction is double speed reproduction. Thus, the CPU 17 proceeds to step S34, in which it performs YES determination (determining that it has updating timing).

Accordingly, the CPU 17 proceeds from step S3 to step S4 in Fig. 4, in which it sets the calculating counter value C to the readout sector counter value RC. Subsequently, it proceeds to step S5, in which it outputs to the IDE controller 12 a command for requesting the reading of 256 sectors from the sector having the numeral set as the counter value RC.

In this manner, in the case of double speed reproduction, the sector counter value C consecutively changes to, such as 0, 512 (= 0 + 256 × 2), and 1024 (= 0 + 256 × 2 + 256 × 2), and the value is set unchanged as the readout sector counter value RC, which performs double speed reproduction as shown in Fig. 7. In other words, after the reproduction of the first frame from number 0 to number 255 ends, the second frame of image data from the 256th sector to the 511th sector is skipped and the third frame of image data from number 512 to number 767 is reproduced. The fourth frame of image data from number 768 to number 1023 is skipped and the fifth frame of image data from successive number 1024 to number 1279 is reproduced.

As described above, consecutive reproduction with one frame skipped is performed to enable double speed reproduction.

In addition, in the case of triple speed reproduction, in step S13 in Fig. 5, YES determination is performed, and

in step S19, the calculating counter value is sequentially incremented by 256 × 3.

Moreover, in this case, in step S31 as the updating timing determination process in Fig. 6, YES determination (determining that the present reproduction is triple speed reproduction) is performed, and in step S34, YES determination (the CPU 17 has updating timing) is obtained. Thus, the counter value C calculated in step S2 in Fig. 4 is set as the readout sector counter value RC each time. Accordingly, as shown as the triple speed reproduction in Fig. 7, after the first frame from number 0 to number 255 is reproduced, the second and third frames of image data are skipped and the fourth frame of image data in sectors from number 768 (= 256 × 3) to number 1023 is reproduced. Subsequently, the seventh frame of image data from number 1536 (= 256 × 3 × 2) to number 1791 is reproduced.

In the above manner, the image data is reproduced in one in three frames, whereby triple speed reproduction is executed.

Next, the process of executing 1/2-fold speed reproduction will be described. In this case, in step S14 in Fig. 5, it is determined that the present reproducing speed is a 1/2-fold speed, and the process proceeds to step S20, in which, subsequent to 0 in the initial mode, the calculating counter value C is incremented by 256 × 1/2.

In the updating timing determination process in Fig. 6, the present reproducing speed is a 1/2-fold speed. Thus, in step S31, NO determination is performed, and in step S32, YES determination is performed. Subsequently, the process proceeds to step S36, in which determination of whether or not (n+1)mod 2 = 0 is performed.

The CPU 17 includes a counter in which variable n representing the number of frames to be reproduced is sequentially incremented by 1 from 1 when the CPU 17 requests the IDE controller 12 to read one frame of image data, and receives the interruption signal corresponding to its request from the IDE controller 12. Variable n corresponds to the number of frames from the initial frame to be reproduced. Accordingly, the result of operating (n+1)mod 2 = 0 means that, when (n+1) is divided by 2, the quotient is 0. Thus, when the number of frames to be reproduced is odd, (n+1) is even, which causes YES determination in step S36, and when the number is even, (n+1) is odd, which causes NO determination in step S36.

As a result, when the number n of frames is odd, the process proceeds to step S34, in which the updating timing determination (YES determination) is performed, and in step S4 in Fig. 4, the process of updating the readout sector counter value RC by using the calculating counter value C calculated in step S2. Conversely, the number n of frames

to be reproduced is even, the process proceeds to step S35 in Fig. 6, in which NO determination (determining that the CPU 17 has no updating timing) is performed, and the updating process in step S4 in Fig. 4 is skipped to perform no updating.

As a result, when n = 1, the initial value of C = 0 is set, and at this time, (1+1)mod 2 = 0 which performs the updating process. Thus, the counter value C is set as the counter value RC such that RC = 0, which reproduces the first frame of image data recorded in sectors from number 0 to number 255.

Next, when n = 2, the calculating counter value C is set to the value of 256 × 1/2, and (2+1)mod 2 = 1. Thus, NO determination is performed in step S35 in Fig. 6, which skips the updating process in step S4 in Fig. 4. Accordingly, although the calculation of C = 256 × 1/2 has been performed, this value is not set as the readout sector counter value RC, and the value RC is set similar to the previous time such that RC = 0. As a result, in the process of issuing a read command in the successive step S5, one frame of image data in sectors from number 0 to number 255 is reproduced. In other words, the same frame (the first frame) of image data is consecutively reproduced twice.

Next, when n = 3 (when frame reproduction in the third time is performed), C = 256 × 1/2 + 256 × 1/2 = 256. In

addition, (3+1)mod 2 = 0. Thus, YES determination is performed in steps S36 and S34 in Fig. 6, and the updating process is performed in step S4 in Fig. 4. As a result, the calculating counter value C is set as the readout sector counter value RC such that RC = 256. As a result, with a command from step S5 it is commanded that the second frame of image data from number 256 to number 511 be read.

Thereafter, in the same manner, each frame is consecutively reproduced twice, and 1/2-fold speed reproduction is realized, as shown in Fig. 7.

Next, when 1/3-fold speed reproduction is set, it is determined that the present reproducing speed is a 1/3-fold speed in step S15 in Fig. 5. Thus, the process proceeds to step S21, in which, after 0 is set in the initial value, the value C is incremented by 256 × 1/3.

Also, in this case, NO determination is performed in steps S31 and S32 in Fig. 6 because the present reproducing speed is a 1/3-fold speed, and in step S33, YES determination is performed. At this time, the process proceeds to step S37, in which determination of whether or not (n+2)mod 3 = 0 is performed. When, as a result of dividing (n+2) by 3 the quotient is 0, YES determination (determining that the CPU 17 has updating timing) is performed in step S34, and when the quotient is not 0 (1 or 2), the process proceeds to step S35, in which NO

determination (determining not to perform updating) is performed.

As a result, when n = 1, C = 0 and (1+2)mod 3 = 0, which performs updating, so that the calculating counter value C is set as the readout sector counter value RC such that RC = 0. Accordingly, as shown as 1/3-fold speed reproduction, the first frame of image data is initially reproduced.

Next, when n = 2, C = 0 + 256 × 1/3. Then, (2+2)mod 3 = 1, which does not perform updating, so that the value RC of 0 is unchanged. Accordingly, the first frame of image data from number 0 to number 255 is read again.

Next, when n = 3, C = 0 + 256 × 1/3 + 256 × 1/3 = 256 × 1/3 × 2. Then (3+2)mod 3 = 2. Accordingly, also, in this case, the updating process is not performed, so that RC = 0 is unchanged. As a result, the first frame of image data in sectors number 0 to number 255 is reproduced again.

Next, when n = 4, C = 256 × 1/3 × 3 = 256. Then (4+4)mod 3 = 3. As a result, in this case, the updating process is performed, so that the counter value C = 0 is set as the counter value RC. Accordingly, the second frame of image data in the 256th sector to the 511th sector is read and reproduced.

Thereafter, the same process is repeatedly performed, and the same frame is consecutively reproduced three times,

whereby reproduction as shown as 1/3-fold speed reproduction is performed.

In the case of 0-fold speed reproduction, the process proceeds from step S16 to step S22, in which the value C is incremented by 256 × 0. In other words, in this case, the value C is substantially not incremented. Also, in this case, in the updating timing process in Fig. 6, YES determination (determining that the present reproducing speed is 0-fold speed) is performed in step S38, and NO determination (determining that the CPU 17 has no updating timing) is always performed in step S35. Accordingly, in this case, the updating process is not performed each time. Thus, a still picture is reproduced.

The foregoing cases perform reproduction at N-fold speeds such as a double speed, a triple speed, a 1/2-fold speed, a 1/3-fold speed and a 0-fold speed. However, reproduction at N-fold speeds excluding the above speeds can be performed. Although the number m of sectors in the hard disc drive 11 in which one frame of image data is recorded is set at 256, another value may be set. In these cases, calculation in step S17 to S22 in Fig. 5 may be implemented as follows:

$$C = C + m \times N$$

In addition, in the case of image data based on a PAL method, one frame of image data can be transmitted using

143040 bytes (1788 blocks).

According to the present invention, in order that variable speed reproduction may be performed, when image data recorded on a recording medium is compressed, it needs to be composed of image data compressed in frames. This makes it possible to perform reproduction at an arbitrary frame to enable variable speed reproduction. In other words, frame differential compressed data in a moving picture expert groups (MPEG) method may not be used. Using the frame differential compressed data generates not I picture but P picture or B picture data, and when the preceding or subsequent frame of image data does not exist, the present frame of image data cannot be reproduced. As a result, it is difficult to perform variable speed reproduction.

The foregoing cases use a hard disc as a recording medium. However, when the medium is not limited thereto but a random accessible recording medium like an optical disc or a magneto-optical disc is used, the present invention may be applied.



WHAT IS CLAIMED IS:

1. A recording/reproducing apparatus for recording data on a disc recording medium in units of sectors, and reproducing the recorded data,

said recording/reproducing apparatus comprising recording control means for performing control so that the start of predetermined units of a coded video signal is recorded at the start of one of the sectors of said disc recording medium.

2. A recording/reproducing apparatus according to Claim 1, wherein said recording control means performs further control so that the predetermined units of the coded video signal are recorded in m consecutive sectors, being a data recording region.

3. A recording/reproducing apparatus according to Claim 2, wherein said recording control means performs further control so that dummy data is recorded in the sector of said data recording region in which the predetermined units of the coded video signal are not recorded.

4. A recording/reproducing apparatus according to

Claim 3, wherein said recording/reproducing apparatus further comprises a digital interface for receiving the coded video signal from an external apparatus.

5. A recording/reproducing apparatus according to Claim 1, wherein the predetermined units are frames, and said recording control means performs control so that the start of the frames of the coded video signal is recorded at the start of one of the sectors of said disc recording medium.

6. A recording/reproducing apparatus according to Claim 5, wherein the coded video signal has been processed by intra-frame coding.

7. A recording/reproducing apparatus according to Claim 6, wherein said recording/reproducing apparatus further comprises a digital interface for receiving the coded video signal from an external apparatus.

8. A recording/reproducing apparatus according to Claim 3, wherein said recording/reproducing apparatus further comprises reproducing control means in which, when the recorded coded video signal is reproduced at a speed N times the normal speed, a value obtained by adding $m \times N$ to

a readout-start sector number for reproducing the L-th predetermined unit of the coded video signal is used as a readout-start sector number for reproducing the (L+1)-th predetermined unit of the coded video signal.

9. A recording method for recording a coded video signal in units of sectors on a disc recording medium, in which the start of predetermined units of a coded video signal is recorded at the start of one of the sectors of said disc recording medium.

10. A recording method according to Claim 9, wherein the predetermined units of the coded video signal is recorded in m consecutive sectors being a data recording region, and dummy data is recorded in the section of the data recording region in which the predetermined number of units of the coded video signal are not recorded.

11. A recording method according to Claim 10, wherein the predetermined units are frames.

12. A recording method according to Claim 11, wherein the coded video signal has been processed by intra-frame coding.

13. A recording method according to Claim 12, wherein the coded video signal is data received from an external apparatus.

14. A recording/reproducing method for recording on a disc recording medium a video signal coded in units of sectors, and reproducing the recorded coded video signal,

in which said recording/reproducing method controls recording so that the start of predetermined units of the coded video signal is recorded at the start of the sectors of said disc recording medium, and the predetermined units of the coded video signal are recorded in m consecutive sectors, and

said recording/reproducing method controls reproduction so that, when the recorded coded video signal is reproduced at a speed N times the normal speed, a value obtained by adding m × N to a readout-start sector number for reproducing the L-th predetermined unit of the coded video signal is used as a readout-start sector number for reproducing the (L+1)-th predetermined unit of the coded video signal.