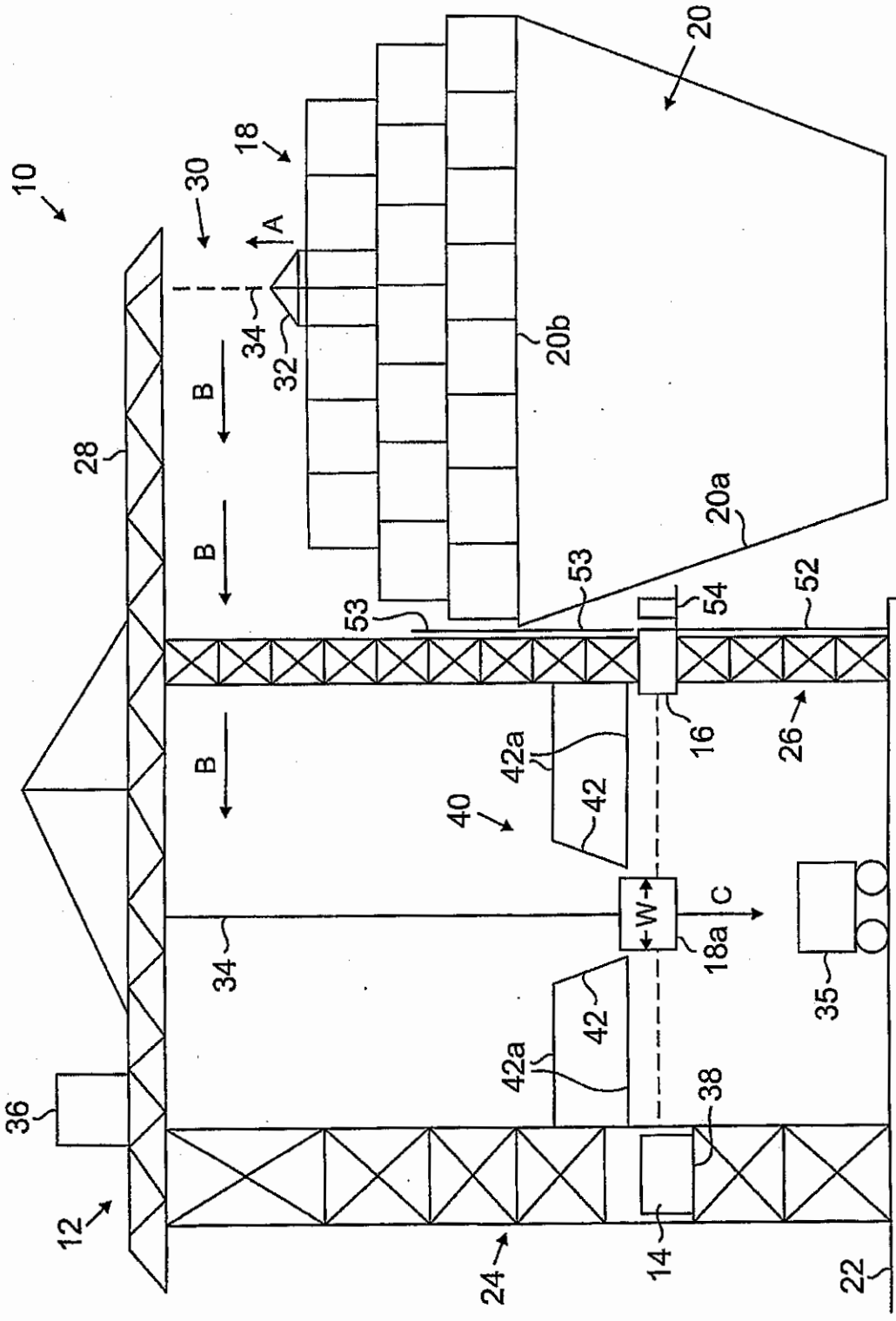

10
12
14
16
18
18a
20
20a
20b
22
24
26
28
30
32
34
35
36
38
40
42
42a
52
53
54
A
B
C
W

FIG. 1a

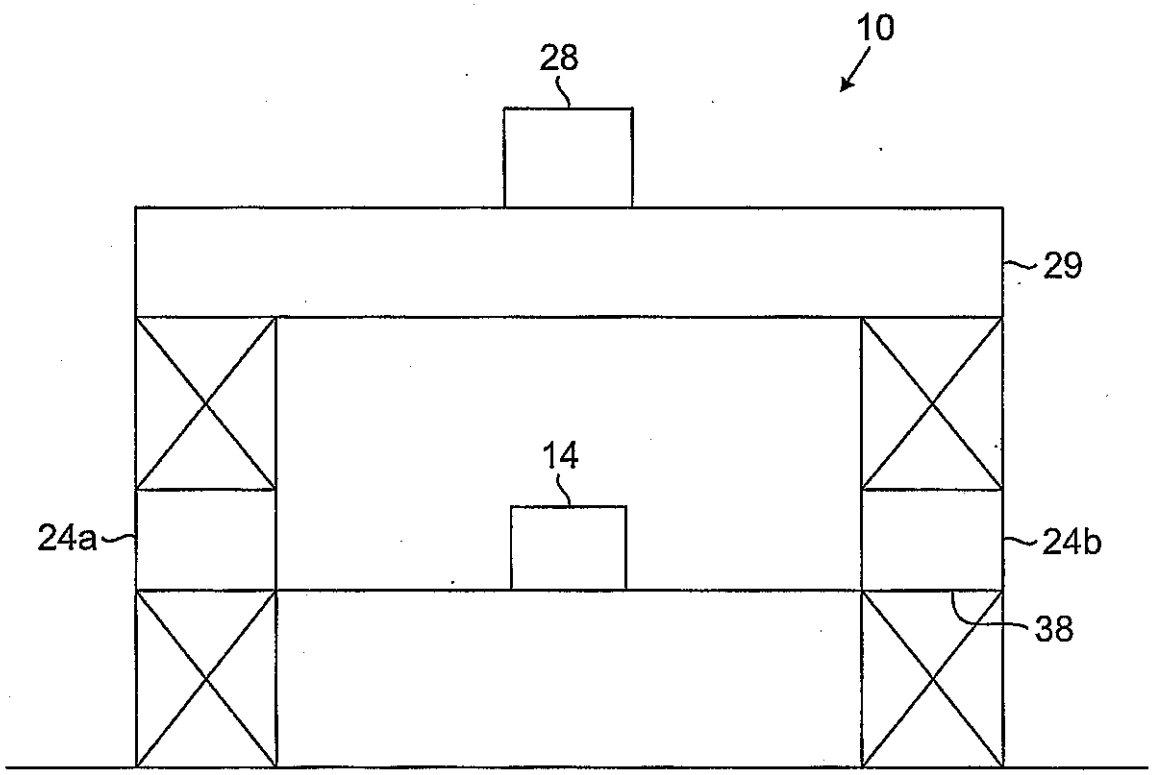


FIG. 1b

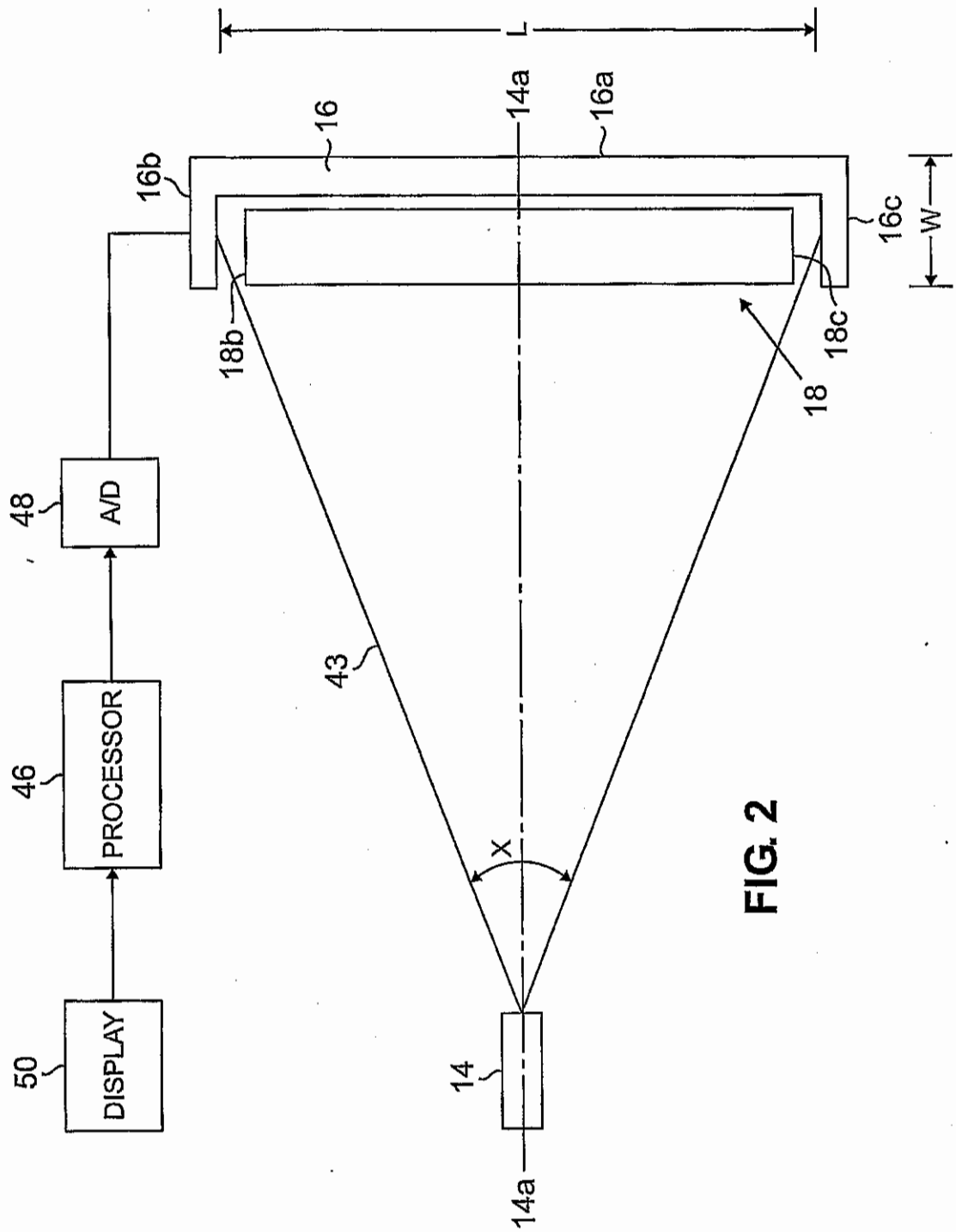

L
16
14a
16a
16b
16c
W
18b
18c
18
43
X
14
14a
48
A/D
46
PROCESSOR
50
DISPLAY

FIG. 2

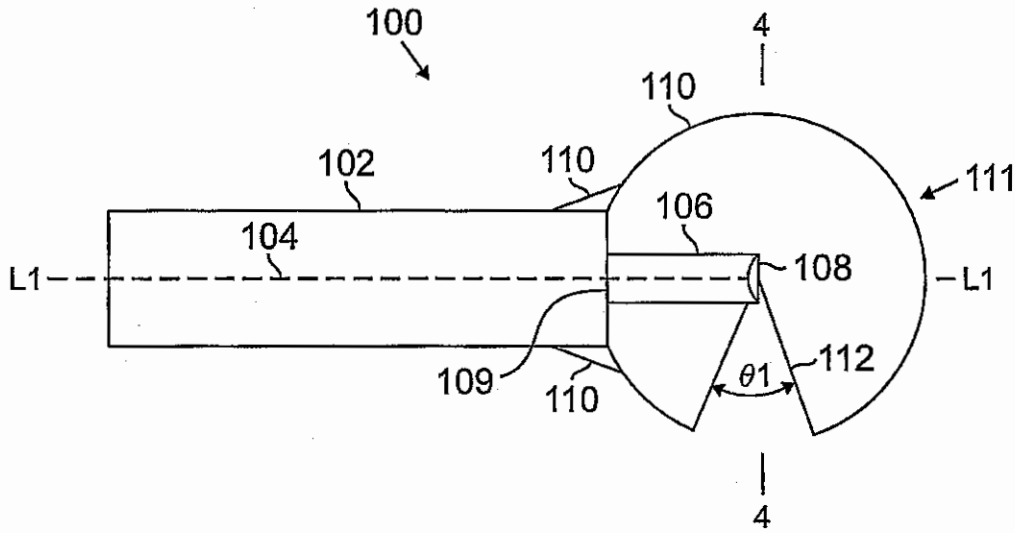

100
4
110
102
110
111
106
104
L1
108
L1
109
110
θ1
112
4

FIG. 3

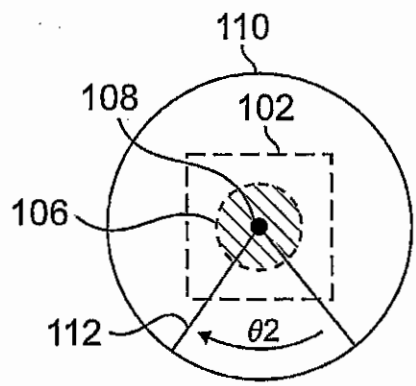

110
108
102
106
112
θ2

FIG. 4

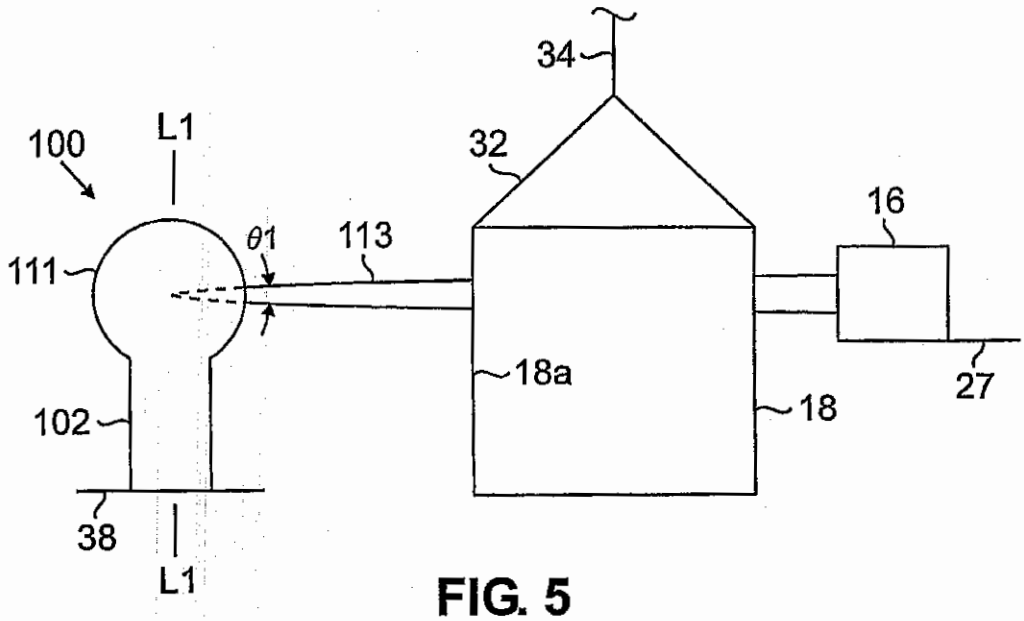


FIG. 5

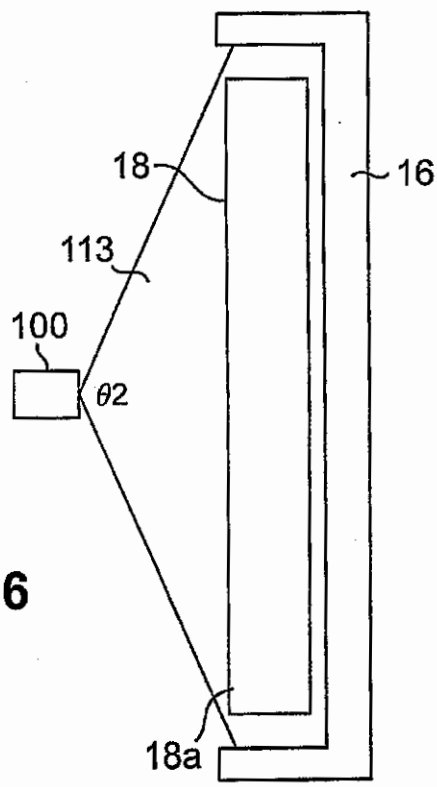


FIG. 6

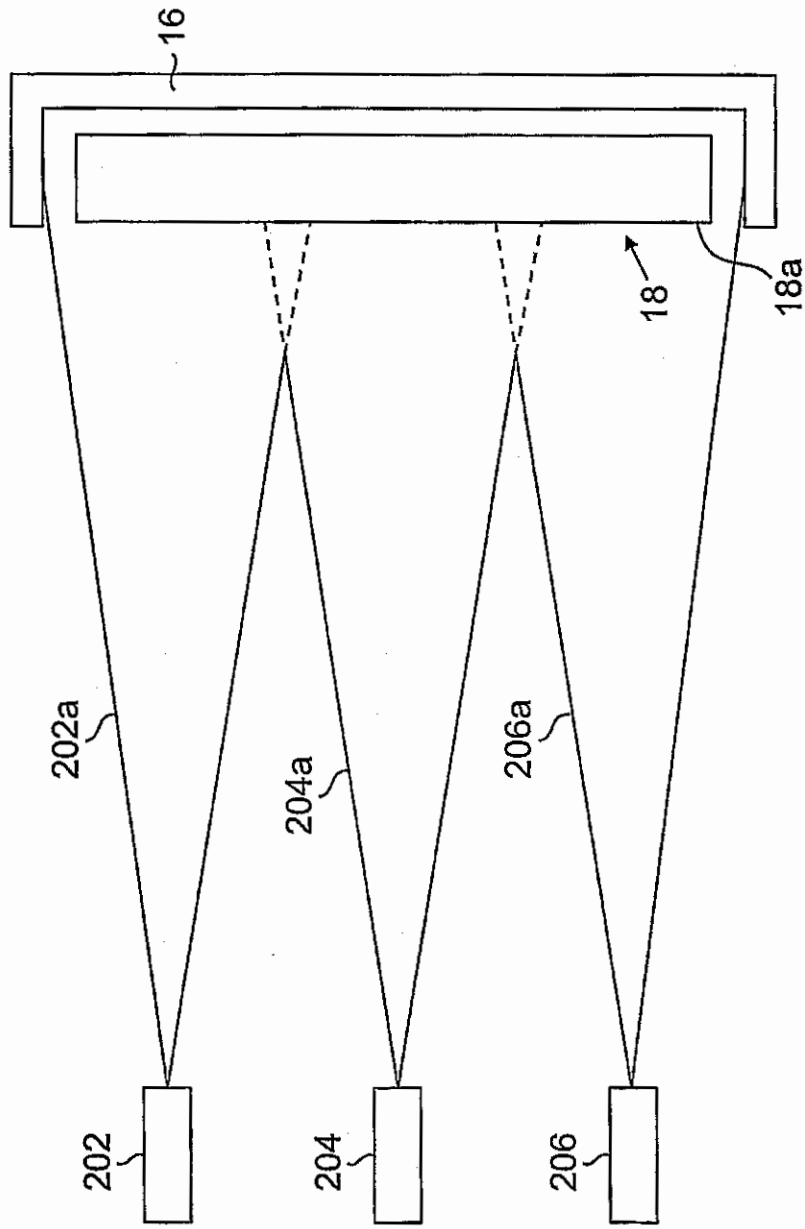


FIG. 7

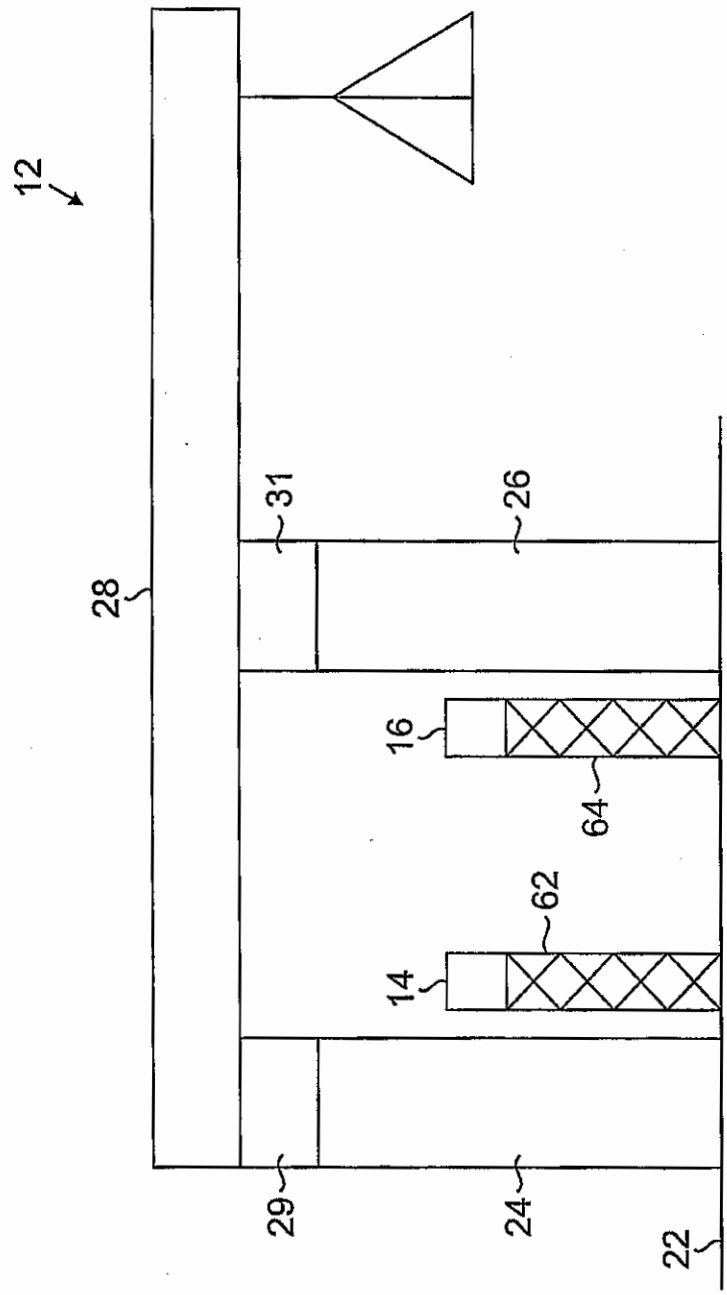


FIG. 8

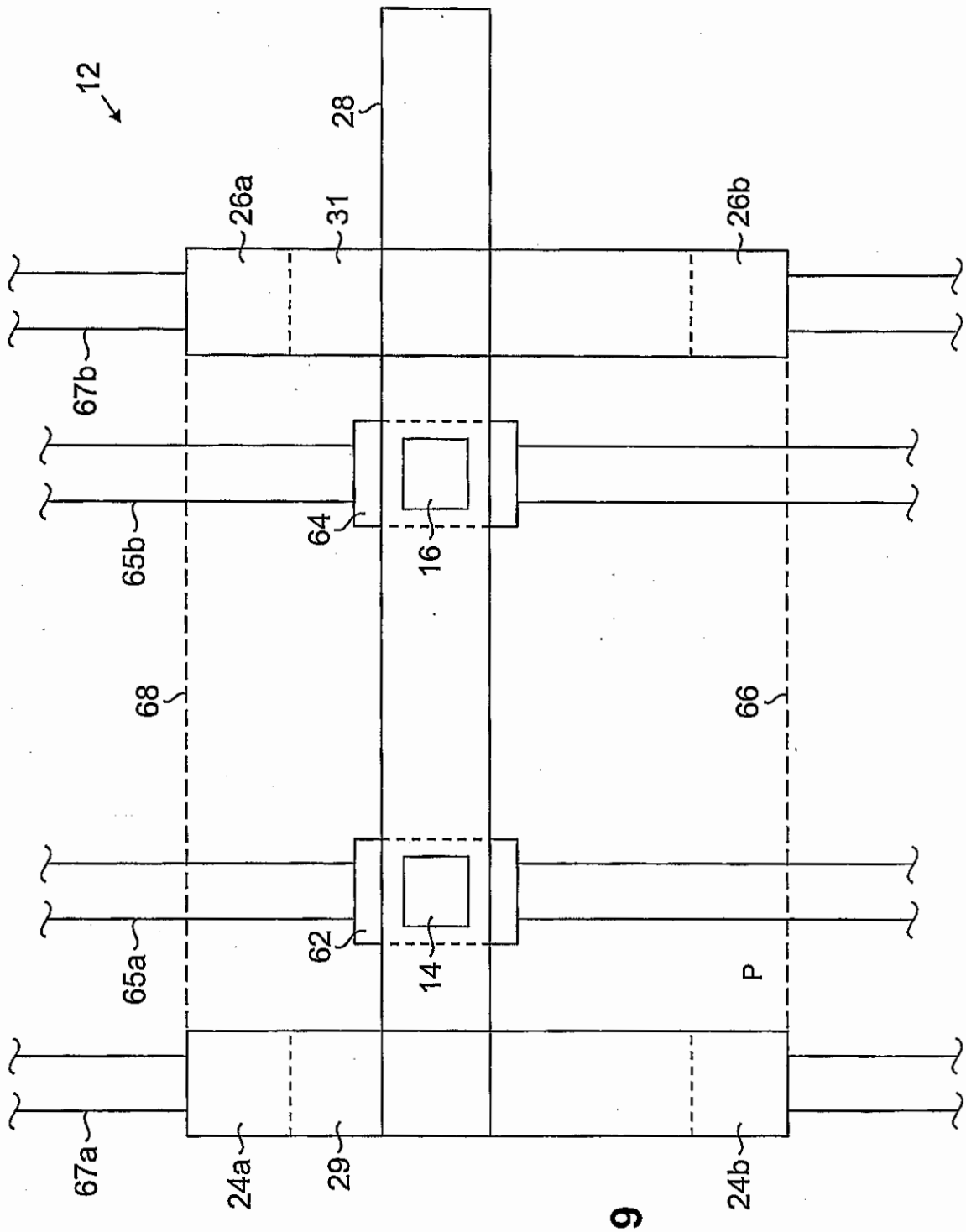


FIG. 9

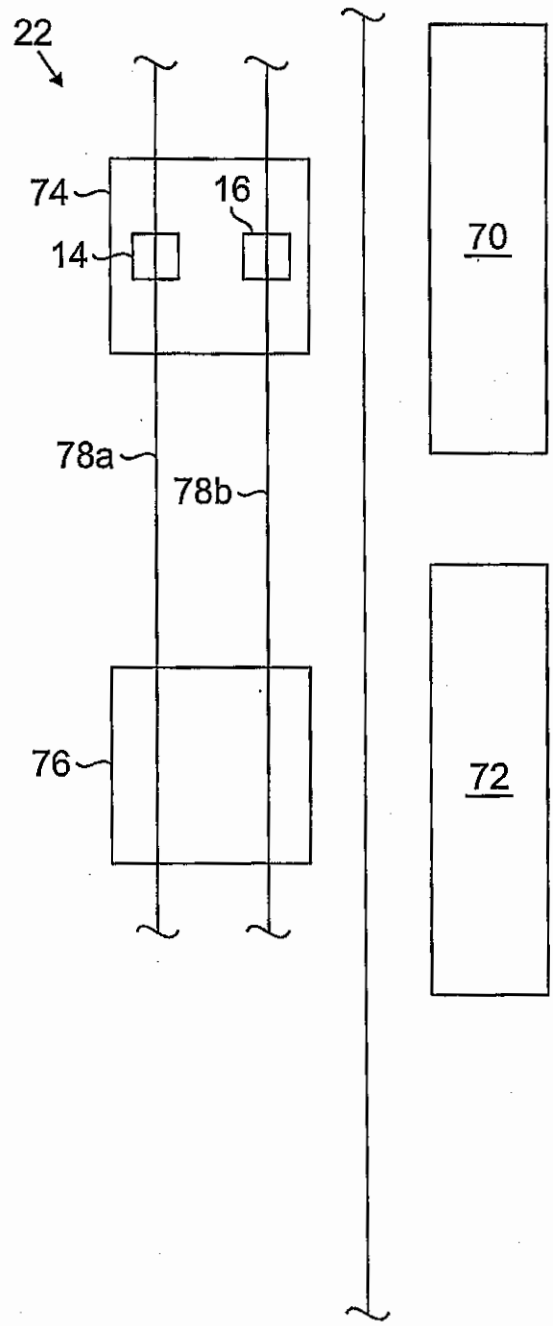


FIG. 10