

CLAIMS:

1. A multilayer structure comprising:

a single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate comprises two major, generally parallel surfaces, one of which is a front surface of the single crystal semiconductor handle substrate and the other of which is a back surface of the single crystal semiconductor handle substrate, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle substrate, a central plane between the front surface and the back surface of the single crystal semiconductor handle substrate, and a bulk region between the front and back surfaces of the single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate has a minimum bulk region resistivity of at least about 500 Ohm-cm, and further wherein the single crystal semiconductor handle substrate has a handle crystal orientation;

an epitaxial layer in direct contact with the front surface of the single crystal semiconductor handle substrate, wherein the epitaxial layer has a resistivity between about 100 Ohm-cm and about 5000 Ohm-cm and further wherein the epitaxial layer has a crystal orientation that is the same as the handle crystal orientation;

a charge trapping layer in direct contact with the epitaxial layer, the charge trapping layer comprising polycrystalline silicon and having a resistivity of at least about 3000 Ohm-cm;

a dielectric layer in direct contact with the charge trapping layer; and

a single crystal semiconductor device layer in direct contact with the dielectric layer.

2. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises single crystal silicon and the single crystal semiconductor device layer comprises single crystal silicon.

3. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 1000 Ohm-cm and about 100,000 Ohm-cm.

4. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 1000 Ohm-cm and about 6,000 Ohm-cm.

5. The multilayer structure of claim 1 wherein the epitaxial layer has a resistivity between about 200 Ohm-cm and about 2000 Ohm-cm.

6. The multilayer structure of claim 1 wherein the epitaxial layer has a resistivity between about 400 Ohm-cm and about 1000 Ohm-cm.

7. The multilayer structure of claim 1 wherein the charge trapping layer has a resistivity of at least about 7000 Ohm-cm.

8. The multilayer structure of claim 1 wherein the epitaxial layer comprises silicon.

9. The multilayer structure of claim 1 wherein the epitaxial layer comprises silicon doped with carbon at a carbon concentration between about 0.1 mole % and about 5 mole %.

10. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof.

11. The multilayer structure of claim 10 wherein the single crystal semiconductor handle substrate comprises an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof, wherein the single crystal semiconductor handle substrate comprises the electrically active p-type dopant at a concentration of less than about 2×10^{13} atoms/cm³.

12. The multilayer structure of claim 10 wherein the epitaxial layer comprises silicon and an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof.

13. The multilayer structure of claim 12 wherein the epitaxial layer comprises silicon and an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof, wherein the epitaxial layer comprises the electrically active n-type dopant at a concentration of less than about 1×10^{14} atoms/cm³.

14. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof, wherein the single crystal semiconductor handle substrate comprises the electrically active p-type dopant at a concentration of less than about 2×10^{13} atoms/cm³; and

the epitaxial layer comprises silicon and an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof, wherein the epitaxial layer comprises the electrically active n-type dopant at a concentration of less than about 1×10^{14} atoms/cm³.

15. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof.

16. The multilayer structure of claim 15 wherein the single crystal semiconductor handle substrate comprises an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof, wherein the single crystal semiconductor handle substrate comprises the electrically active n-type dopant at a concentration of less than about 2×10^{13} atoms/cm³.

17. The multilayer structure of claim 15 wherein the epitaxial layer comprises silicon and an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof.

18. The multilayer structure of claim 17 wherein the epitaxial layer comprises silicon and an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof, wherein the epitaxial layer comprises the electrically active p-type dopant at a concentration of less than about 1×10^{14} atoms/cm³.

19. The multilayer structure of claim 1 wherein the single crystal semiconductor handle substrate comprises an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof, wherein the single crystal semiconductor handle substrate comprises the electrically active n-type dopant at a concentration of less than about 2×10^{13} atoms/cm³; and

the epitaxial layer comprises silicon and an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof, wherein the epitaxial layer comprises the electrically active p-type dopant at a concentration of less than about 1×10^{14} atoms/cm³.