ABSTRACT

CMOS SRAM CELL CONFIGURED USING MULTIPLE-GATE TRANSISTORS

A complementary metal-oxide-semiconductor static random access memory cell that is formed by a pair of P-channel multiple-gate field-effect transistors (P-MGFETs), a pair of N-channel multiple-gate field-effect transistors (N-MGFETs), a second pair of N-MGFETs that has a drain respectively connected to a connection linking the respective drain of the N-MGFET of the first pair of N-MGFET to the drain of the P-MGFET of the pair of P-MGFETs; a pair of complementary bit lines, each respectively connected to the source of the N-MGFET of the second pair of N-MGFETS; and a word line connected to the gates of the N-MGFETs of the second pair of N-MGFETs.

(FIG. 1A)