CLAIMS

1. A data processing system to perform a hardware transactional memory (HTM) transaction, the data processing system comprising:
a byte-addressable nonvolatile memory for persistently storing data; and
a processor being to execute an atomic HTM write operation in connection with committing the HTM transaction by writing an indicator to the nonvolatile memory indicating a successful commit of the HTM transaction,
wherein the data processing system is further to flush the data written by the HTM operation from a cache memory to the nonvolatile memory after the successful commit of the HTM transaction.

2. A data processing system to perform a hardware transactional memory (HTM) transaction, the data processing system comprising:
a byte-addressable nonvolatile memory for persistently storing data; and
a processor being to execute an atomic HTM write operation in connection with committing the HTM transaction by writing an indicator to the nonvolatile memory indicating a successful commit of the HTM transaction,
wherein the data processing system is further to transparently flush the data written by the HTM operation from a cache memory to the nonvolatile memory without aborting a HTM transaction.

3. The data processing system of claim 1 or 2, wherein the processor is coupled to a cache memory by a plurality of cache lines and wherein the cache memory is to be used by the processor for caching data using a cache coherence protocol.

4. The data processing system of any one of claims 1 to 3, wherein the data processing system is further to set the HTM transaction to unlogged state, in particular unset the indicator after the successful commit of the HTM transaction.

5. The data processing system of any one of claims 1 to 4, wherein the indicator indicating the successful commit of the HTM transaction comprises a HTM transaction identifier., in particular a commit record.

6. A data processing method for performing a hardware transactional memory (HTM) transaction, the data processing method comprising:
the step of executing an atomic HTM write operation in connection with committing the HTM transaction by writing an indicator to a nonvolatile memory indicating a successful commit of the HTM transaction; and
the step of flushing the data written by the HTM operation from a cache memory to the nonvolatile memory after the successful commit of the HTM transaction.

7. A data processing method for performing a hardware transactional memory (HTM) transaction, the data processing method comprising:

the step of executing an atomic HTM write operation in connection with committing the HTM transaction by writing an indicator to a nonvolatile memory indicating a successful commit of the HTM transaction; and

the step of transparently flushing the data written by the HTM operation from a cache memory to the nonvolatile memory without aborting a HTM transaction.

8. The data processing method of claim 6 or 7, comprising the step of setting the HTM transaction to unlogged state, in particular unsetting the indicator after the successful commit of the HTM transaction.

9. A program which makes a computer to execute the data processing method of any one of claims 6 to 8.