



Description

The invention relates to a current-source arrangement comprising:

—means for generating a plurality of currents at outputs of the means, which currents are substantially in a given current ratio to one another

—means for detecting deviations in the values of at least some of the currents from those required to realize the given current ratio, and

—means for correcting said currents so as to reduce the detected deviations.

In various fields of electronics there is a need for circuits which are capable of supplying currents whose values bear a very accurate ratio to each other. Such circuits are required in, for example, measuring equipment, where various current ratios must be available for measuring-range selection, and digital-to-analogue converters which form an analogue signal by adding a plurality of currents to each other in accordance with a digital code.

It is known to generate binary weighted currents in a digital-to-analogue converter by applying a reference voltage across resistors of binary weighted resistance values or across a so-called resistive ladder network. The accuracy of this type of digital-analogue converter mainly depends on the accuracy of the resistance ratios. In order to obtain these accurate ratios the resistors are trimmed, for example by means of a laser. However, in practice resistor trimming is a time-consuming and expensive operation.

Another known method of generating currents with accurate current ratios employs the dynamic elements matching principle. This principle is known from United States Patent Specification 3,982,172 and United States Patent Specification 4,125,803. These employ a current-source arrangement which supplies a plurality of currents which have only substantially equal current values owing to the limited accuracy of the integration process. By means of a permutation circuit these currents are transferred to outputs of the permutation circuit in accordance with a cyclic permutation. The currents on the outputs each comprise a direct current of a value equal to the average value of the currents from the current-source arrangement and a ripple which is superimposed on the direct current, which ripple is formed by the differences between the currents from the current source arrangement. The ripple can be removed by arranging a filter capacitor on each output of the permutation circuit. However, because of their large values such filter capacitors cannot be integrated but must be added externally to the integrated circuit. This requires additional connection pins, which entails additional costs. For example, for 16-bit digital-analogue converter using such a current-source arrangement 16 additional connection pins are required.

This means that there is a need for methods which enable currents with accurate mutual current ratios to be generated in a simple manner.

A current-source arrangement of a type as set forth in the opening paragraph is known from the article "An Untrimmed D/A Converter with 14 Bit Resolution" IEEE Jnl. of Solid-State Circuits, Vol. SC-16, No. 6, December 1981, pages 616—620. This digital-to-analogue converter comprises a ladder network with untrimmed resistors. Deviations in the values of the currents are detected by comparing the output voltages of the digital-to-analogue converter which corresponds to said currents with a very accurate sawtooth voltage. The information about said deviations is stored in a memory. Subsequently the information is employed for driving a sub-digital-to-analogue converter by means of which the deviations in the currents of the digital-to-analogue converter are eliminated.

Such a circuit arrangement does not require resistor trimming, but it does require a sawtooth voltage of very high linearity over a wide range, which is difficult to achieve.

Therefore, it is the object of the invention to provide a current-source arrangement by means of which a plurality of currents having mutually accurate current ratios can be generated in a simple manner. A current source arrangement of the type set forth in the opening paragraph is characterized in that it comprises

—a precision current mirror circuit having an input and at least one output on which a current appears whose value is in an accurate ratio to a current on the input,

—a coupling network for coupling the input and the at least one output of the current mirror circuit to a corresponding number of outputs of the current-generating means in accordance with a cyclic pattern which is such that in each step of a cycle the input of said current-mirror circuit is coupled to a corrected current output of the current-generating means or when the cycle is started, to a non-corrected current output of the current-generating means, and the at least one output of the current-mirror circuit is coupled to an uncorrected-current output of the current-generating means, and

—a detection circuit on each output of the precision current-mirror circuit for detecting the difference between the current from the means for generating a plurality of currents coupled to said output and the current from the current-mirror circuit which appears on said output.

The invention is based on recognition of the fact that it is possible to detect deviations in the current ratios by coupling said currents to a current mirror which operates very accurately. The number of outputs of the current mirror is limited and is at least one. Each time some of the currents from the means for generating a plurality of currents are coupled to the current mirror by means of a coupling network, one current being coupled to the input and the other currents each being coupled to an output. The ratio of the currents coupled to the outputs to the current coupled to the input is only substantially equal to a given value. However, the reflected currents

also appear on the outputs of the current mirror, the ratio of these currents to the current on the input being equal to said given value with a very high accuracy. The difference between an inaccurate current from the means for generating a plurality of currents and a reflected accurate current on an output of the current mirror is detected by a detection circuit. This detection circuit controls a correction circuit which corrects the relevant current from the means for generating a plurality of currents, so that the ratio of this current to the current on the input is accurately equal to the current-mirror ratio for this output of the current mirror. After correction of the currents a subsequent number of currents is coupled to the outputs of the current mirror by means of the coupling network, one of the corrected currents of the preceding number being coupled to the input of the current mirror. In this way the current mirror circuit processes all or at least some of the currents from the means for generating a plurality of currents by means of the coupling network, after which the cycle is repeated. In this way it is possible to obtain a large number of currents with accurate mutual ratios by means of a current mirror having a small number of outputs.

An embodiment of the invention is characterized in that the precision current-mirror circuit comprises:

—a current distribution circuit provided with a plurality of transistors having parallel-connected main current paths and having commoned control electrodes which are driven by an amplifier whose input is coupled to the input of the current-mirror circuit, and

—permutation circuit for transferring the currents from the current distribution circuit to the input and the at least one output of the current-mirror circuit in accordance with a cycle permutation.

A precision current-mirror circuit can be arranged in an advantageous manner by the use of the dynamic element matching principle, which is known *per se* from the aforementioned United States Patent Specifications 3,982,172 and 4,125,803. The currents on the outputs of the current-mirror circuit then have very accurate direct current ratios.

The ripple superimposed on these direct currents can be filtered out by arranging filter capacitors on the input and the output(s) of the current-mirror circuit. Since the number of outputs of the current-mirror circuit is small, only a limited number of external connection pins for said filter capacitors are required on the integrated circuit. As a result of the small number of outputs the permutation circuit can also operate at a low frequency, which assists in obtaining a high accuracy.

The arrangement may be further characterized in that the or each detection circuit comprises a first current-voltage converter. Suitably such an arrangement is characterized in that each first current-voltage converter comprises an amplifier having a first input which is coupled to the

corresponding output of the current-mirror circuit, a second input which carries a reference voltage, and an output which is coupled to the first input of the amplifier *via* a feedback capacitor. The amplifier then functions as an integrator. The capacitor has a small value so that it can be integrated.

The arrangement may be further characterized in that the means for correcting the currents comprise a second current-voltage converter corresponding to each current to be corrected, which second current-voltage converter comprises an amplifier having an output which is coupled to a first input of the amplifier *via* a feedback capacitor, which first input can be coupled to the output of the first current-voltage converter by means of a switching capacitor. The switching capacitor transfers the charge on the capacitor of the first current-voltage converter to the capacitor of the second current-voltage converter. The capacitor of the second current-voltage converter, by means of which converter the relevant current is corrected, holds the correction voltage at least until the corresponding interval of the next cycle of the coupling network.

The output of the amplifier of the first current-voltage converter may be coupled to a first input of a comparator, which has a second input which carries a reference voltage. The comparator converts the output signal of the amplifier into a logic signal.

The means for correcting currents may comprise a counting circuit corresponding to each current to be corrected, which counting circuit can be coupled to the output of the first current-voltage converter by means of a switch and generates a plurality of logic signals in dependence upon the logic signal on the output of the comparator, which signals, by means of a digital-analogue converter, are converted into an analogue output signal with which the relevant current is corrected. The count of the counting circuit does not change until the corresponding interval of the next cycle of the coupling network, so that during this period the digital-to-analogue converter holds the correction signal.

The invention is particularly suitable for use in current source arrangements in which the means for generating a plurality of currents comprise means for generating at least a plurality of currents whose values vary in conformity with a binary weighted series, as required in digital-analogue converters. One precision current-mirror circuit can now correct the currents from one or more, for example 16-bit, digital-to-analogue converters. In addition the invention may be used in current-source arrangements in which the means for generating a plurality of currents comprise means for generating a plurality of currents of substantially equal current values, as is frequently required in modern integrated circuits. An embodiment in which the means for generating a plurality of currents are provided with a plurality of parallel branches which each comprise the main current path of a

respective first transistor, which main current path extends between respective first and second main terminals, each branch comprising a resistor which is coupled to the first main terminal of the relevant first transistor, may be characterized in that the at least one output and the input of the precision current-mirror circuit are coupled to the said second main terminals or to those ends of the resistors which are remote from the first transistors by means of the coupling networks. Herein, the first main terminal of a transistor is to be understood to mean the emitter or source electrode and the second main terminal of a transistor is to be understood to mean the collector or drain electrode of a bipolar and of a unipolar transistor respectively. Such an arrangement may be further characterized in that in at least some of the branches at those ends of the resistors which are remote from the first transistors the main current path of a field-effect transistor is arranged which path extends between respective first and second main terminals. The at least one output and the input of the precision current-mirror circuit may be coupled to the second main terminals of the field-effect transistors by means of the coupling network. The field-effect transistors have the advantage that undesired switching transients caused by switching of the coupling network have substantially no influence on the currents from the current-source arrangement. In this arrangement it is advantageous to couple the outputs of the correction means to the gate electrodes of the field-effect transistors. The correction means increase or decrease the voltage on the gate electrodes of the FETs and thus the voltage difference between these electrodes and the commoned control electrodes of the first transistors, so that the main currents of these transistors are corrected.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings in which

Figure 1 shows a first embodiment of the invention in the form of a digital-analogue converter,

Figure 2 shows a second embodiment of the invention in the form of a digital-analogue converter,

Figure 3 shows a third embodiment of the invention in the form of a digital-analogue converter,

Figure 4 shows a fourth embodiment of the invention in the form of a digital-analogue converter, and

Figure 5 shows a fifth embodiment of the invention used as a current-source arrangement.

Figure 1 schematically shows a first embodiment of the invention in the form of a digital-analogue converter. In general it comprises the actual digital-analogue converter 1 in which a plurality of binary weighted currents which should have accurate mutual current ratios are generated and a coupling network 15 with which a plurality of currents from the D/A converter 1

can be coupled to a precision current-mirror circuit 25 in accordance with a cyclic pattern, by means of which current-mirror circuit deviations in the ratios of the currents from the D/A converter 1 can be detected with detection means 80 which control correction means 18.2 to 18.16 by means of which the relevant currents from the D/A converter 1 can be corrected so as to reduce the deviations.

In the present embodiment the digital-analogue converter 1 is a 16-bit D/A converter comprising 16 transistors 2.1 to 2.16. For D/A converters having not more than approximately 10 bits it is possible to obtain equal current densities in the transistors by the binary scaling of all emitter areas. In the present 16-bit D/A converter equal current densities are obtained by arranging the transistors 2.1 to 2.16 in two identical sections of 8 transistors each, the emitter area of a transistor in each section being half the emitter area of the preceding transistor and the sections being adapted to each other by a voltage source, not shown, which is arranged in the base line between the sections. Untrimmed resistors 3.1 to 3.16 are arranged in the emitter lines of the transistors 2.1 to 2.16, the resistance value of each resistor being substantially twice as high as that of the preceding resistor. The transistors 2.1 to 2.16 have commoned bases which are coupled to the output of an operational amplifier 4 whose input is coupled to a current source 5 whose current has a value I_0 . The amplifier 4 drives these bases so that the collector current of transistor 2.1, which is employed as a reference current, is accurately equal to the current I_0 from the current source 5. For this collector current of the reference transistor 2.1 the collector current of each of the transistors 2.2 to 2.16 is substantially half the value of the collector current of the preceding transistor if inaccuracies in the resistors and transistors are ignored, because the emitter voltages of all the transistors are substantially equal. The currents from transistors 2.1 to 2.16 then have the values $I_0, I_0/2, I_0/4, \dots, I_0/2^{15}$. The collector currents of the transistors 2.1 to 2.16 can be fed to earth or to the input of an amplifier 7 by switches 6.1 to 6.16 which are controlled by the digital input code. The analogue output signal corresponding to the digital code appears on the output 9, which is coupled to the (inverting) input via a feedback resistor 8. The resistors 3.1 to 3.16 are connected to the source electrodes of n-channel field-effect transistors 12.1 to 12.16, whose channel length-width ratio, as the case may be per section, is scaled in conformity with the relevant current value in order to maintain equal current densities and thereby equal voltages between the gate and source electrodes of the transistors. In the normal condition the drain electrodes are coupled to a point of fixed voltage via switches 16.1 to 16.16 which form part of the coupling network 15, which point of fixed voltage is at 0 V in the present embodiment. The gate electrode 13.1 of transistor 12.1 is connected directly to a point of fixed voltage, in the present

example a voltage of zero, whilst the gate electrode 13.2 to 13.16 are connected to said point by means of correction circuits 18.2 to 18.16. For the sake of clarity only the correction circuits 18.2 and 18.3 are shown in detail, the other correction circuits being shown only schematically. The correction circuit 18.2 comprises an amplifier 19.2, whose output is coupled to the gate electrode 13.2 and via a capacitor 20.2 to the inverting input. The non-inverting input of the amplifier 19.2 is connected to earth. A capacitor 21.2 may be short-circuited to earth or may be connected between the inverting input of the amplifier 19.2 and input 24.2 by means of simultaneously controlled switches 22.2 and 23.2. The other correction circuits are constructed in the same way.

A control circuit 17 controls the switches 16.1 to 16.16 of the coupling network 15 in such a way that the collector-emitter currents of three consecutive ones of the transistors 2.1 to 2.16 are respectively coupled to the input 26 and the outputs 27 and 28 of the precision current-mirror circuit 25 in accordance with a cyclic pattern. The high output resistance of the drain electrode and the low input resistance of the source electrode of each of the field-effect transistors 12.1 to 12.16 ensure that during switching the collector-emitter currents of the transistors 2.1 to 2.16 are not influenced by undesired switching transients. The Figure shows the situation during the first interval of the cycle of the control circuit 17, in which the reference transistor 2.1 is coupled to the input 26 and the transistors 2.2 and 2.3 are coupled to the outputs 27 and 28 respectively of the current-mirror circuit 25. The current-mirror circuit 25 reflects the reference current on the input 26 to the outputs 27 and 28 in accurately defined ratios. Said circuit 25 comprises parallel connected transistors 30 to 36, whose emitters are connected to a common terminal 47 via equal resistors 40 to 46, which terminal 47 carries a fixed voltage and in the present case is the negative power-supply terminal. The commoned bases of the transistors 30 to 36 are driven by an amplifier 49 whose input is coupled to the input 26 of the current-mirror circuit 25. The amplifier 49 controls the voltage on the commoned bases in such a way that the sum of the currents on the outputs 61, 62, 63 and 64 of a permutation circuit 50 is equal to the collector-emitter current I_0 of the reference transistor 2.1. The collector currents of the transistors 30 to 36 are only substantially equal to each other as a result of the limited accuracy of the integration process and in the present case they are made substantially equal to $I_0/4$ by splitting the current I_0 from the reference transistor 2.1. These currents are fed to the inputs 51 to 57 of the permutation circuit 50. This permutation circuit 50 is controlled by a circuit 70, for example a shift register, which in its turn is controlled by a clock generator 71. The operation of the permutation circuit 50 is described comprehensively in the afore-mentioned United States Patent Specifications 3,982,172 and 4,125,803. In this respect it suffices to note that the permutation circuit 50

transfers each of the collector currents of the transistors 51 to 57 to each of the outputs 61 to 67 in accordance with a cyclic permutation. Thus, each of the collector currents of the transistors 30 to 36 will appear consecutively on each of the outputs 61 to 67. The direct current on each of the outputs 61 to 67 is equal to the average value $I_0/4$ of these collector currents. These output currents exhibit a ripple around said average value $I_0/4$, the ripple components being caused by the inequality of the collector currents. This ripple is filtered out by the filter capacitors 72, 73 and 74, which must be added externally to the circuit. Direct currents whose values relative to the direct current on the input 26 are accurately proportioned as 1:2:4 then appear on the outputs 27 and 28 of the precision-current mirror 25. For the value I_0 of the current from the reference transistor 2.1 on the input 26 currents whose direct current values are exactly equal to $I_0/2$ and $I_0/4$ will appear on the outputs 27 and 28 respectively. The currents from transistors 22 and 23 whose values are substantially equal to $I_0/2$ and $I_0/4$ respectively also appear on outputs 27 and 28. Any difference in value between the inaccurate applied and accurately reflected current on the output 27 is detected by a current-voltage converter 81 and any difference in value between the applied and the reflected currents on the output 28 is detected by the current-voltage converter 82. The current-voltage converters 81 and 82 together constitute the detection means 80. The output 27 is coupled to the inverting input of an operational amplifier 83, whose non-inverting input carries a fixed voltage, in the present case 0 V. The output of the amplifier 83 is connected to the inverting input via a feedback capacitor 84.

The output 85 of the amplifier 83 is coupled to the input 24.2 of the correction circuit 18.2 by means of a switching network, which is not shown for the sake of clarity. A difference between the values of the applied inaccurate current and the accurately reflected current $I_0/2$ on the output 27 charges the capacitor 84. The current-voltage converter 82 is constructed in the same way as the current-voltage converter 81 and comprises an amplifier 86 and a capacitor 87. The output 88 of the amplifier 86 is coupled to the input 24.3 of the correction circuit 18.3. A difference in value between the applied inaccurate current and the accurately reflected current charges the capacitor 87.

After the capacitor 84 has been charged the capacitor 21.2 is switched between the input 24.2 of the detection circuit 18.2 and the inverting input of the amplifier 19.2 by means of the switches 22.2 and 23.2. As a result of this, charge on capacitor 84 is transferred to capacitor 20.2, so that the latter is charged.

Similarly the capacitor 21.3 is arranged between the input 24.3 of the correction circuit 18.3 and the inverting input of the amplifier 19.3 by means of the switches 22.3 and 23.3, so that the charge on capacitor 87 is transferred to capacitor 20.3. After the capacitors 20.2 and 20.3

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have been charged the capacitors 21.2 and 21.3 are short-circuited to earth by means of the respective switches 22.2; 23.2 and 22.3; 23.3. Simultaneously, the reset switches 89 and 90 are closed, which switches short circuit the capacitors 84 and 87. Since the capacitors 20.2 and 20.3 are charged the voltages on the gate electrodes 13.2 and 13.3 increase or decrease, so that the voltage differences between the bases of transistors 2.2 and 2.3 and the respective gate electrodes 13.2 and 13.3 of the transistors 12.2 and 12.3, and consequently the emitter currents of the transistors 2.2 and 2.3, increase or decrease, in such a way that these currents more accurately become equal to $I_0/2$ and $I_0/4$ respectively. The capacitors 20.2 and 20.3 hold the correction voltages. In the corresponding interval of the next cycle of the control circuit 17 the emitter currents of the transistors 2.2 and 2.3 are again compared with the accurately reflected currents $I_0/2$ and $I_0/4$ by means of the current-mirror circuit 25. Differences are again detected by the detection circuits 81 and 82 and, by means of the capacitors 21.2 and 21.3, charge is transferred to the capacitors 20.2 and 20.3. Thus, the emitter currents of the transistors 2.2 and 2.3 become more accurately equal to $I_0/2$ and $I_0/4$. In this way the emitter currents of the transistors 2.2 and 2.3 are corrected in the consecutive cycles until they are equal to $I_0/2$ and $I_0/4$ with a high accuracy. The capacitors 20.2; 20.3 and the capacitors 21.2; 2.3 as well as the capacitors 84 and 87 have such small values that they can be integrated. In the second interval of the cycle of the control circuit 17 the switches 16.3, 16.4 and 16.5 couple the emitter currents of the transistors 2.3, 2.4 and 2.5 to the input 26 and the outputs 27 and 28, respectively, of the precision current-mirror circuit 25. The emitter current $I_0/4$ of transistor 2.3, which has been corrected in the preceding interval, now serves as the accurate input current for the current-mirror circuit 25. The reflected accurate currents $I_0/8$ and $I_0/16$ appear on outputs 27 and 28. The differences from the inaccurate emitter currents of the transistors 2.4 and 2.5 are again detected by the detection circuits 81 and 82. The outputs 85 and 88 of the amplifiers 83 and 86 are now coupled to the inputs 24.4 and 24.5 of the correction circuits 18.4 and 18.5 for the transistors 12.4 and 12.5, by means of which the emitter currents of the transistors 2.4 and 2.5 are corrected so that they become equal to $I_0/8$ and $I_0/16$ with a higher accuracy. In the next intervals the currents of the transistors 2.6 and 2.16 are corrected in a similar way, the smallest current of the three currents corrected in the preceding interval serving each time as the accurate input current to the current mirror circuit 25. After all currents have been corrected the entire cycle is repeated.

In the present embodiment the collector-emitter currents of all transistors 2.2 to 2.16 are corrected. In principle it is necessary to correct only those currents whose values exhibit an error which is greater than a predetermined fraction of the smallest current.

In the present embodiment the currents are corrected by controlling the voltages on the gate electrodes of the field-effect transistors. However, it is alternatively possible to correct the currents by controlling the voltages on the individual bases of the current-source transistors.

A second embodiment of the invention in the form of a digital-analogue converter will be described with reference to Figure 2; in which identical parts bear the same reference numerals as in Figure 1, whenever possible. The actual D/A converter 1 again comprises 16 transistors 2.1 to 2.16 with untrimmed resistors 3.1 to 3.16 having binary weighted resistance values. The reference current in the present embodiment is not equal to the largest current, i.e. to the current corresponding to the most significant bit, but to the smallest current, i.e. the current corresponding to the least significant bit. This reference current is generated by means of a transistor 2.17 having an emitter area equal to that of the transistor 2.16 in whose emitter line a resistor 3.17 is arranged whose value is equal to that of the resistor 3.16. The base of transistor 2.17 is driven by an operational amplifier 4, whose input is coupled to the output of a current source supplying a current of the value I_0 . The amplifier 4 drives the bases so that the collector current of the reference transistor 2.17 is accurately equal to the current I_0 . The collector currents of the transistors 2.16 to 2.1 are then I_0 , $2I_0$, $4I_0$, ..., $2^{15}I_0$. The switches 6.1 to 6.16, which are controlled by the digital input code, transfer the currents either to earth or to the input of the amplifier 7, on whose output the analogue output signal appears. The emitter resistors 3.1 to 3.17 are connected to switches 16.1 to 16.17 of the coupling network 15 via field-effect transistors 12.1 to 12.17. The gate electrode 13.17 is connected to earth, correction circuits being coupled to the gate electrodes 13.1 to 13.16. Each correction circuit 14 comprises a counting circuit 14.1 to 14.16 having inputs 14.41 to 14.56 and having outputs coupled to the inputs of digital-analogue converters 14.21 to 14.36, whose outputs are coupled to the gate electrodes 13.1 to 13.16. Depending on the required control range and the desired accuracy the counting circuits 14.1 to 14.16 comprise for example six-bit counters with one sign bit which defines the sign of the voltage on the outputs of the six-bit D/A converters 14.21 to 14.36. The D/A converters 14.21 to 14.36 do not supply an output voltage when the count is zero. The Figures show the situation during the first interval of the cycle of the control circuit 17 during which the reference transistor 2.17 is coupled to the input 26 and the transistors 2.16 and 2.15 are coupled to the outputs 27 and 28 of the precision current-mirror circuit 25. The control circuit 17 controls the switches 16.17 to 16.1 in such a way that two consecutive emitter currents are coupled to the outputs 27 and 28 of the current-mirror circuit 25 each time, the current on input 26 being equal to the sum of the emitter currents of the previously corrected transistors including the reference tran-

sistor. The current-mirror circuit in the present embodiment comprises parallel-connected transistors 100 to 103, whose emitters are connected to the common terminal 108 via equal resistors 104 to 107. The commoned bases are driven by an amplifier 49 whose input is coupled to the input 26 of the current mirror 25. The amplifier controls the bases so that the current on the output 115 of the permutation circuit 50 is equal to the current on the input 26. The collector currents of the transistors 100 to 103 applied to the inputs 110 to 113 are transferred to the outputs 115 to 118 by the permutation circuit 50 in accordance with a cyclic permutation. The currents from the outputs 117 and 118 are together applied to the output 28. The ratio of the current on the input 26 to the currents on the outputs 27 and 28 is then accurately equal to 1:1:2. The ripple on the input and outputs is filtered out by externally connected filter capacitors 72, 73 and 74. In the first interval of the cycle of the control circuit the current on input 26 is equal to I_0 . The reflected currents on the outputs 27 and 28 are then accurately equal to I_0 and $2 I_0$. The emitter currents of the transistors 2.16 and 2.15 are also coupled to the outputs 27 and 28, which emitter currents are substantially equal to I_0 and $2 I_0$. The differences between the accurately reflected currents and the inaccurate emitter currents on the outputs 27 and 28 are detected by the detection circuits 81 and 82. The construction of the detection circuit 81 is the same as in the first embodiment, except that the output of the amplifier 83 is coupled to the inverting input of a comparator 120, whose non-inverting input carries a fixed voltage, in the present case 0 V. Depending on whether the output voltage of the amplifier 83 is higher or lower than zero the voltage on the output of the comparator 120 is high or low, and is employed as a logic signal of the value "1" or "0". The output of the comparator 120 can be coupled to the input 14.56 of the counter 14.16 by means of a switch 91. Depending on the value of the logic signal on the output of the comparator 120 the counter 14.16 is incremented or decremented. This count is translated into six logic signals on the outputs of the counter 14.16, which signals are converted in the six-bit D/A converter 14.36 into an analogue output voltage which appears on the gate electrode 13.16. In a similar way it is possible to couple the output of the comparator 121 of the detection circuit 82 to the input 14.55 of the counting circuit 14.15 by means of a switch 92, so that an analogue output voltage appears on the gate electrode 13.15 of transistor 12.15. The positive or negative voltages on the gate electrodes 13.16 and 13.15 then reduce or increase the emitter currents of the transistors 2.16 and 2.15, so that these currents become more accurately equal to I_0 and $2 I_0$ respectively. The counts of the counters 14.16 and 14.15 and consequently the voltages on the gate electrodes 13.16 and 13.15 remain unchanged until the corresponding interval of the next cycle. In the consecutive cycles the emitter currents of the transistors 12.16 and 12.15

are thus corrected until they are equal to I_0 and $2 I_0$ respectively with a high degree of accuracy. In the second interval of the cycle the control circuit 17 controls the switches 16.1 to 16.17 in such a way that the emitter currents of the transistors 2.17, 2.16 and 2.15 are coupled to the input 26 and the emitter currents of the transistors 2.14 and 2.13 are coupled to the outputs 27 and 28 respectively of the precision current-mirror circuit 25. The sum of the emitter currents of transistors 2.17, 2.16 and 2.15 is accurately equal to $4 I_0$. Then the accurately reflected currents $4 I_0$ and $8 I_0$ appear to the outputs 27 and 28. These accurate currents are again compared with the inaccurate emitter currents $4 I_0$ and $8 I_0$ of the transistors 2.14 and 2.13. Differences in current value are again converted into logic signals by the detection circuits 81 and 82, which logic signals are applied to the inputs 14.54 and 14.53 of the counting circuits 14.14 and 14.13. The analogue output voltages of the D/A converters 14.34 and 14.33 are applied to the gate electrodes 13.14 and 13.13 of the transistors 12.14 and 12.13. In the same way the sum of the corrected currents constitutes the input current to the current mirror 25 in the next intervals. When all currents have been corrected the cycle recommences.

In the same way as in the first embodiment it is not necessary to correct all currents in the second embodiment. By means of the reference transistor it is possible to generate a current which is equal to a current which is larger than the current corresponding to the least significant bit. Only currents larger than and equal to this reference current are then corrected.

A third embodiment will be described with reference to Figure 3, in which identical parts bear the same reference numerals as in Figure 2. The D/A converter again comprises 16 transistors 2.1 to 2.16 with untrimmed binary weighted resistors 3.1 to 3.16 and a reference transistor 2.17 with a resistor 3.17. The commoned bases are driven by the amplifier 4 so that the collector current of transistor 2.17 is I_0 . The emitter resistors 3.1 to 3.17 are connected to earth by means of the field-effect transistors 12.1 to 12.17. Again correction circuits with inputs 14.41 to 14.56 are coupled to the gate electrodes 13.1 to 13.16. The switches 6.1 to 6.16 which are controlled by the digital input code, again feed the currents either to earth or to the input of the amplifier 7. However, the switches 6.1 to 6.17 may also be coupled to the input 26 and the outputs 27 and 28 of the precision current-mirror circuit 25 by the control circuit 17, which input and outputs in the present embodiment are not coupled to the emitter lines but to the collector lines of the transistors 2.1 to 2.17. When the precision current-source arrangement 25 is coupled to these lines the operation of the D/A converter 1 is interrupted. In the present embodiment the current-mirror circuit 25 comprises parallel-connected PNP-transistors 150 to 153 instead of NPN transistors as in Figure 2. Via equal resistors 155 to 158 the emitters are connected to a common terminal 160, which is the

positive power-supply terminal. The commoned bases of the transistors 150 to 153 are coupled to the output of the amplifier 49, whose input is coupled to the input 26 of the current-mirror circuit 25. The amplifier 49 controls the voltage on the commoned bases in such a way that the current on the output 115 is equal to the current on the input 26. The permutation circuit 50 transfers the currents on the inputs 110 to 113 to the outputs 115 to 118 in accordance with a cyclic permutation, so that the currents on the input 26 and the outputs 27 and 28 are accurately proportioned as 1:1:2. Again the ripple is filtered out by the capacitors 72, 73 and 74. In the first interval of the cycle of the control circuit 17, as shown, the current on input 26 is I_0 . The reflected currents on the outputs 27 and 28 are then accurately equal to I_0 and $2 I_0$. The differences between these accurately reflected currents and the inaccurate collector currents of the transistors 2.16 and 2.15 which are coupled to the outputs 27 and 28 are again detected by the detection circuits 81 and 82. The outputs of these circuits are coupled to the inputs 14.56 and 14.55 of the correction circuits, by means of which the collector currents of the transistors 2.16 and 2.15 are corrected. In the next interval of the cycle of the control circuit 18 the collector currents of the transistors 2.17, 2.16 and 2.15 are together coupled to the input 26 and the collector currents of the transistors 2.14 and 2.13 are coupled to the outputs 27 and 28 respectively, so that the collector currents of the transistors 2.14 and 2.13 are rendered accurately equal to $4 I_0$ and $8 I_0$. In the same way the sum of the corrected currents constitutes the input current for the current mirror 25 in the next intervals. After the collector currents of the transistors 2.1 to 2.16 have been corrected in a number of cycles the current-mirror circuit 25 may be coupled periodically to the D/A converter 1 in order to correct the collector currents again. The frequency with which this is effected *inter alia* depends on the variation of the collector currents as a function of time. In the same way as in the first and the second embodiment it is not necessary in the present embodiment to correct all the currents, but the reference current may be larger than the current corresponding to the least significant bit. In the third embodiment the resistors 3.1 to 3.17 may alternatively be connected directly to earth without the inclusion of the field-effect transistors 12.1 to 12.16. In that case the correction D/A converters 14.21 to 14.36 must be provided with a current output instead of a voltage output, which outputs must then be connected to the emitters of the transistors 2.1 to 2.16. By the addition of a correction current the voltage across the relevant resistor 3.1 to 3.16 is increased or reduced, which results in a decrease or increase of the collector current of the relevant transistor 2.1 to 2.16. If this third embodiment is equipped with hold capacitors, as in Figure 1, instead of correction D/A converters, the outputs of the correction circuits 18.2 to 18.16 may be connected directly to the resistors 3.1 to 3.16 without the inclusion of the field-effect transistors 12.1 to 12.17.

In the embodiments so far described the precision current-mirror circuit 25 always comprises one input and two outputs. This has the advantage that two currents are corrected per interval of the cycle of the control circuit so that all currents can be corrected in a comparatively short time. However, instead of two outputs the precision current-mirror may comprise only one output.

Moreover, in the embodiment so far described the number of outputs of the permutation circuit is always equal to the number of inputs of the permutation circuit. Moreover, the ratio between the currents on the outputs of the permutation circuit is always substantially equal to unity. Current-mirror ratios different from unity are obtained by combining currents on the outputs of the permutation circuit. In a precision current-mirror circuit in accordance with the invention the number of outputs of the permutation circuit may differ from the number of inputs, the number of currents transferred to an output in one period of the cycle time of the permutation circuit may be different from one, and the number of currents flowing to each output in one period of the cycle time may be different. Furthermore, the transistors of the current-mirror circuit may be selectively activated.

A fourth embodiment is described with reference to Figure 4, which schematically shows three 16-bit D/A converters 210, 220 and 230, which are for example identical to the D/A converter 1 shown in Figure 2. By means of a coupling network 240, which is controlled by a control circuit 250, the currents from the D/A converters 210, 220 and 230 can be corrected using only one precision current-mirror circuit 260, which is for example constituted by a 1:1:2 current-mirror circuit as shown in Figure 2, and detection circuits 270. The current-mirror circuit 260 can correct the D/A converters 210, 220 and 230 with a low frequency, because the variation of the currents from the D/A converters 210, 220 and 230 in one cycle time of the control circuit 260 is small.

So far the invention has been described for use in conjunction with D/A-converters. However, the invention is not limited to D/A-converters but may be used in any circuit arrangement in which a plurality of currents with an accurate mutual ratio are required. An embodiment for obtaining a large number of equal currents is described with reference to Figure 5 in which identical parts bear the same reference numerals as in Figure 1. The section 1 is constructed in the same way as in Figure 1, except that the emitter areas of the transistors 2.1 to 2.16 and the emitter resistors 3.1 to 3.16 are not binary scaled but are substantially equal to each other. Moreover, the collector lines are not coupled to the input of a summation amplifier but are coupled to further circuits, not shown, included in the integrated circuit. The emitter currents of the transistors 2.1 to 2.16 may be coupled to the input 26 and, in the present case, the one output 27 of the current-mirror circuit 25 by means of the coupling network 15. In the consecutive intervals the control circuit 17 controls the

switches 16.1 to 16.16 in such a way that one emitter current is compared each time with the reference emitter current of the transistor 2.1. The current-mirror circuit 25 comprises two transistors 300 and 301 with emitter resistors 302 and 303. Their commoned bases are again driven by an amplifier 49 whose input is connected to the input 26. The currents on the input 305 and 306 are transferred to the outputs 307 and 308 by the permutation circuit 50 in accordance with a cyclic permutation, so that accurately equal currents appear on the input 26 and the output 27. The difference between an accurately reflected current and the inaccurate emitter current of transistor 2.2 is detected by the detection circuit 81, by means of which the capacitor 20.2 is charged so that the emitter current is corrected. In the next intervals each of the currents from the transistors 2.3 to 2.16 is compared with the reference current from transistor 2.1 and is corrected.

It will be evident that a multitude of variants to the embodiments shown are possible within the scope of the invention. For example, it is obvious that in the embodiments shown P-MOS-transistors may be used instead of the P-channel junction field-effect transistors 12.1 to 12.17 and N-channel junction FETs and N-MOS-transistors may be used instead of the NPN-transistors 2.1 to 2.16. Moreover, it is obvious that complementary PNP-transistors, P-channel junction FETs and P-MOS transistors may be used for the transistors 2.1 to 2.16 and N-channel junction FETs and N-MOS transistors for the transistors 12.1 to 12.17. The same applies to the other transistors in the circuit. For example, in the embodiments it is possible to employ field-effect transistors as the current source transistors and to employ bipolar transistors to control the currents from the current-source transistors. Also a large number of modifications to the detection and correction circuits are conceivable to those skilled in the art.

Claims

1. A current-source arrangement comprising:
 - means (1) for generating a plurality of currents at outputs of the means, which currents are substantially in a given current ratio to one another
 - means for detecting deviations in the values of at least some of the currents from those required to realize the given current ratio, and
 - means for correcting said currents so as to reduce the detected deviations,
 characterized in that the means for detecting deviations in the values of the currents comprise:
 - a precision current mirror circuit (25) having an input (26) and at least one output (27, 28) on which a current appears whose value is in an accurate ratio to a current on the input (26),
 - coupling network (15) for coupling the input (26) and the at least one output (27, 28) of the current mirror circuit (25) to a corresponding number of outputs of the current-generating means (1) in accordance with a cyclic pattern

which is such that in each step of a cycle the input (26) of said current-mirror circuit (25) is coupled to a corrected current output of the current-generating means (1) or when the cycle is started to a non-corrected current output of the current-generating means (1) and the at least one output (27, 28) of the current-mirror circuit (25) is coupled to an uncorrected-current output of the current-generating means, and

—a detection circuit (81, 82) on each output (27, 28) of the precision current-mirror circuit (25) for detecting the difference between the current from the means (1) for generating a plurality of currents coupled to said output (27, 28) and the current from the current-mirror circuit (25) which appears on said output (27, 28) (Fig. 1).

2. A current-source arrangement as claimed in Claim 1, characterized in that the precision current-mirror circuit (25) comprises:

—a current distribution circuit provided with a plurality of transistors (30—36) having parallel-connected main current paths and having commoned control electrodes which are driven by an amplifier (49) whose input is coupled to the input (26) of the current-mirror circuit (25), and

—a permutation circuit (50) for transferring the currents from the current distribution circuit to the input (26) and the at least one output (27, 28) of the current-mirror circuit (25) in accordance with a cyclic permutation (Fig. 1).

3. A current-source arrangement as claimed in Claim 1 or 2, characterized in that each detection circuit (81, 82) comprises a first current-voltage converter (Fig. 1).

4. A current-source arrangement as claimed in Claim 3, characterized in that each first current-voltage converter (81, 82) comprises an amplifier (83, 86) having a first input which is coupled to the corresponding output (27, 28) of the current-mirror circuit (25), a second input which carries a reference voltage, and an output (85, 88) which is coupled to the first input of the amplifier via a feedback capacitor (84, 87) (Fig. 1).

5. A current-source arrangement as claimed in Claim 4, characterized in that the amplifier output is coupled to a first input of a comparator (120, 121) which has a second input which carries a reference voltage (Fig. 2).

6. A current-source arrangement as claimed in Claim 3 or 4, characterized in that the means for correcting the current (18.2, 18.3) comprise a second current-voltage converter corresponding to each current to be corrected, which second current-voltage converter comprises an amplifier (19.2, 19.3) having an output which is coupled to a first input of the amplifier via a feedback capacitor (20.2, 20.3), which first input can be coupled to the output of the first current-voltage converter (82, 83) by means of a switching capacitor (21.2, 21.3) (Fig. 1).

7. A current-source arrangement as claimed in Claim 5, characterized in that the means for correcting currents comprise a counting circuit (14.1—14.16) corresponding to each current to be corrected, which counting circuit can be coupled

switches 16.1 to 16.16 in such a way that one emitter current is compared each time with the reference emitter current of the transistor 2.1. The current-mirror circuit 25 comprises two transistors 300 and 301 with emitter resistors 302 and 303. Their commoned bases are again driven by an amplifier 49 whose input is connected to the input 26. The currents on the input 305 and 306 are transferred to the outputs 307 and 308 by the permutation circuit 50 in accordance with a cyclic permutation, so that accurately equal currents appear on the input 26 and the output 27. The difference between an accurately reflected current and the inaccurate emitter current of transistor 2.2 is detected by the detection circuit 81, by means of which the capacitor 20.2 is charged so that the emitter current is corrected. In the next intervals each of the currents from the transistors 2.3 to 2.16 is compared with the reference current from transistor 2.1 and is corrected.

It will be evident that a multitude of variants to the embodiments shown are possible within the scope of the invention. For example, it is obvious that in the embodiments shown P-MOS-transistors may be used instead of the P-channel junction field-effect transistors 12.1 to 12.17 and N-channel junction FETs and N-MOS-transistors may be used instead of the NPN-transistors 2.1 to 2.16. Moreover, it is obvious that complementary PNP-transistors, P-channel junction FETs and P-MOS transistors may be used for the transistors 2.1 to 2.16 and N-channel junction FETs and N-MOS transistors for the transistors 12.1 to 12.17. The same applies to the other transistors in the circuit. For example, in the embodiments it is possible to employ field-effect transistors as the current source transistors and to employ bipolar transistors to control the currents from the current-source transistors. Also a large number of modifications to the detection and correction circuits are conceivable to those skilled in the art.

Claims

1. A current-source arrangement comprising:
 - means (1) for generating a plurality of currents at outputs of the means, which currents are substantially in a given current ratio to one another
 - means for detecting deviations in the values of at least some of the currents from those required to realize the given current ratio, and
 - means for correcting said currents so as to reduce the detected deviations,
 characterized in that the means for detecting deviations in the values of the currents comprise:
 - a precision current mirror circuit (25) having an input (26) and at least one output (27, 28) on which a current appears whose value is in an accurate ratio to a current on the input (26),
 - coupling network (15) for coupling the input (26) and the at least one output (27, 28) of the current mirror circuit (25) to a corresponding number of outputs of the current-generating means (1) in accordance with a cyclic pattern

which is such that in each step of a cycle the input (26) of said current-mirror circuit (25) is coupled to a corrected current output of the current-generating means (1) or when the cycle is started to a non-corrected current output of the current-generating means (1) and the at least one output (27, 28) of the current-mirror circuit (25) is coupled to an uncorrected-current output of the current-generating means, and

—a detection circuit (81, 82) on each output (27, 28) of the precision current-mirror circuit (25) for detecting the difference between the current from the means (1) for generating a plurality of currents coupled to said output (27, 28) and the current from the current-mirror circuit (25) which appears on said output (27, 28) (Fig. 1).

2. A current-source arrangement as claimed in Claim 1, characterized in that the precision current-mirror circuit (25) comprises:

—a current distribution circuit provided with a plurality of transistors (30—36) having parallel-connected main current paths and having commoned control electrodes which are driven by an amplifier (49) whose input is coupled to the input (26) of the current-mirror circuit (25), and

—a permutation circuit (50) for transferring the currents from the current distribution circuit to the input (26) and the at least one output (27, 28) of the current-mirror circuit (25) in accordance with a cyclic permutation (Fig. 1).

3. A current-source arrangement as claimed in Claim 1 or 2, characterized in that each detection circuit (81, 82) comprises a first current-voltage converter (Fig. 1).

4. A current-source arrangement as claimed in Claim 3, characterized in that each first current-voltage converter (81, 82) comprises an amplifier (83, 86) having a first input which is coupled to the corresponding output (27, 28) of the current-mirror circuit (25), a second input which carries a reference voltage, and an output (85, 88) which is coupled to the first input of the amplifier *via* a feedback capacitor (84, 87) (Fig. 1).

5. A current-source arrangement as claimed in Claim 4, characterized in that the amplifier output is coupled to a first input of a comparator (120, 121) which has a second input which carries a reference voltage (Fig. 2).

6. A current-source arrangement as claimed in Claim 3 or 4, characterized in that the means for correcting the current (18.2, 18.3) comprise a second current-voltage converter corresponding to each current to be corrected, which second current-voltage converter comprises an amplifier (19.2, 19.3) having an output which is coupled to a first input of the amplifier *via* a feedback capacitor (20.2, 20.3), which first input can be coupled to the output of the first current-voltage converter (82, 83) by means of a switching capacitor (21.2, 21.3) (Fig. 1).

7. A current-source arrangement as claimed in Claim 5, characterized in that the means for correcting currents comprise a counting circuit (14.1—14.16) corresponding to each current to be corrected, which counting circuit can be coupled



to the output of the current-voltage converter (81, 82) by means of a switch (91, 92) and generates a plurality of logic signals in dependence upon the logic signal on the output of the comparator (120, 121), which signals, by means of a digital-analogue converter (14.21—14.36), are converted to an analogue output signal with which the relevant current is corrected (Fig 2).

8. A current source arrangement as claimed in any of the preceding Claims, characterized in that the means (1) for generating a plurality of currents comprise means for generating at least one plurality of currents whose values vary in accordance with a binary weighted series (Fig 1).

9. A current source arrangement as claimed in any of the preceding Claims 1 to 7, characterized in that the means (1) for generating a plurality of currents comprise means for generating a plurality of currents of substantially equal values (Fig 5).

10. A current source arrangement as claimed in Claims 8 or 9, the means for generating a plurality of currents comprising a plurality of parallel branches which each comprise the main current path of a respective first transistor (2.1—2.16), which main current path extends between respective first and second main terminals, each branch comprising a resistor (3.1—3.16) which is coupled to the first main terminal of the relevant first transistor, characterized in that the at least one output (27, 28) and the input (26) of the precision current-mirror circuit (25) are coupled to the said second main terminals or to those ends of the resistors which are remote from the first transistors by means of the coupling network (15) (Figs 1, 2).

11. A current source arrangement as claimed in Claim 10, characterized in that in at least some of the branches at those ends of the resistors (3.1—3.16) which are remote from the first transistors (2.1—2.16) the main current path of a field-effect transistor (13.1—13.16) is arranged which path extends between respective first and second main terminals (Fig 1).

12. A current source arrangement as claimed in Claim 11, characterized in that the at least one output (27, 28) and the input (26) of the precision current-mirror circuit (25) are coupled to the second main terminals of the field-effect transistors (13.1—13.16) by means of the coupling network (15) (Figs 1, 2).

13. A current source arrangement as claimed in Claim 11 or 12, characterized in that the outputs of the correction means (18.2, 18.3) are coupled to the gate electrodes of the field-effect transistors (13.1—13.16) (Fig 1).

Patentansprüche

1. Stromquellenschaltung mit

—Mitteln (1) zum Erzeugen einer Anzahl von Strömen an Ausgängen der Mittel, wobei diese Ströme im wesentlichen in einem gegebenen Stromverhältnis zueinander stehen;

—Mitteln zum Detektieren von Abweichungen

in den Werten wenigstens einiger der Ströme von denen der zur Verwirklichung des gegebenen Stromverhältnisses erforderlichen Strömen, und;

—Mitteln zum Korrigieren dieser Ströme zur Verringerung der detektierten Abweichungen, dadurch gekennzeichnet, dass die Mittel zum Detektieren von Abweichungen in den Stromwerten folgende Schaltungselemente enthalten:

—eine Präzisionsstromspiegelschaltung (25) mit einem Eingang (26) und wenigstens einem Ausgang (27, 28), an dem ein Strom erscheint, dessen Wert in einem genauen Verhältnis zu einem Strom am Eingang (26) steht;

—ein Kopplungsnetzwerk (15) zum Verbinden des Eingangs (26) und des wenigstens einen Ausgangs (27, 28) der Stromspiegelschaltung (25) mit einer entsprechenden Anzahl von Ausgängen der Stromzeugungsmittel (1) in Übereinstimmung mit einem derartigen zyklischen Muster, das in jedem Schritt eines Zyklus der Eingang (26) der Stromspiegelschaltung (25) an einen korrigierten Stromausgang der Stromerzeugungsmittel (1), oder, wenn der Zyklus gestartet wird, an einen nicht korrigierten Stromausgang der Stromerzeugungsmittel (1) und der wenigstens einen Ausgang (27, 28) der Stromspiegelschaltung (25) an einen Ausgang der Stromerzeugungsmittel mit unkorrigiertem Strom angeschlossen ist, und;

eine Detektorschaltung (81, 82) an jedem Ausgang (27, 28) der Präzisionsstromspiegelschaltung (25) zum Detektieren des Unterschieds zwischen dem Strom aus den mit dem Ausgang (27, 28) verbundenen Mitteln (1) zum Erzeugen einer Anzahl von Strömen und dem Strom aus der Stromspiegelschaltung (25), der am Ausgang (27, 28) erscheint (Figur 1).

2. Stromquellenanordnung nach Anspruch 1, dadurch gekennzeichnet, dass die Präzisionsstromspiegelschaltung (25) folgende Schaltungselemente enthält:

—eine Stromverteilerschaltung mit einer Anzahl von Transistoren (30, . . . , 36) mit parallel geschalteten Hauptstromwegen und gemeinsamen Steuerelektroden, die von einem Verstärker (49) gesteuert werden, dessen Eingang an den Eingang (26) der Stromspiegelschaltung (25) angeschlossen ist, und;

—eine Permutationsschaltung (50) zum Übertragen der Ströme aus der Stromverteilerschaltung auf den Eingang (26) und den wenigstens einen Ausgang (27, 28) der Stromspiegelschaltung (25) entsprechend einer zyklischen Permutation (Figur 1).

3. Stromquellenanordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass jede Detektorschaltung (81, 82) einen ersten Stromspannungswandler enthält (Figur 1).

4. Stromquellenanordnung nach Anspruch 3, dadurch gekennzeichnet, dass jeder erste Stromspannungswandler (81, 82) einen Verstärker (83, 86) mit einem ersten Eingang, der mit dem entsprechenden Ausgang (27, 28) der Stromspiegelschaltung (25) verbunden ist, mit einem zweiten Eingang, der eine Bezugsspannung führt, und mit einem Ausgang (85, 88) enthält, der an den ersten



Eingang des Verstärkers über einen Rückkopplungskondensator (84, 87) angeschlossen ist (Figur 1).

5. Stromquellenanordnung nach Anspruch 4, dadurch gekennzeichnet, dass der Verstärkersausgang an einen ersten Eingang eines Komparators (120, 121) angeschlossen ist, dessen zweiter Eingang eine Bezugsspannung führt (Figur 2).

6. Stromquellenanordnung nach Anspruch 3 oder 4, dadurch gekennzeichnet, dass die Mittel zum Korrigieren der Ströme (182, 183) einen zweiten Stromspannungswandler in Übereinstimmung mit jedem zu korrigierenden Strom enthält, der einen Verstärker (192, 193) mit einem Ausgang enthält, der an einen ersten Eingang des Verstärkers über einen Rückkopplungskondensator (202, 203) angeschlossen ist, und dieser erste Eingang mit Hilfe eines Schaltkondensators (212, 213) an den Ausgang des ersten Stromspannungswandlers (82, 83) angeschlossen werden kann (Figur 1).

7. Stromquellenanordnung nach Anspruch 5, dadurch gekennzeichnet, dass die Mittel zum Korrigieren von Strömen ein Zähschaltung (14.1, ..., 14.16) in Übereinstimmung mit jedem zu korrigierenden Strom enthält, die mit dem Ausgang des Stromspannungswandlers (81, 92) über einen Schalter (91, 92) verbunden werden kann und eine Anzahl logischer Signale in Abhängigkeit vom logischen Signal am Ausgang des Komparators (120, 121) erzeugt, und diese Signale mittels eines Digital/Analog-Wandlers (14.21, ..., 14.36) in ein analoges Ausgangssignal umgewandelt wird, mit dem der betreffende Strom korrigiert wird (Figur 2).

8. Stromquellenanordnung nach einem vorangehenden Ansprüche, dadurch gekennzeichnet, dass die Mittel (1) zum Erzeugen einer Anzahl von Strömen Mittel zum Erzeugen wenigstens einer Anzahl von Strömen enthält, deren Werte in Übereinstimmung mit einer binär gewogenen Reihe variieren (Figur 1).

9. Stromquellenanordnung nach einem der vorangehenden Ansprüche 1 bis 7, dadurch gekennzeichnet, dass die Mittel (1) zum Erzeugen einer Anzahl von Strömen Mittel zum Erzeugen einer Anzahl von Strömen mit im wesentlichen gleichen Werten enthält (Figur 5).

10. Stromquellenanordnung nach Anspruch 8 oder 9, wobei die Mittel zum Erzeugen einer Anzahl von Strömen eine Anzahl von parallelen Abzweigungen enthält, die je den Hauptstromweg eines betreffenden ersten Transistors (2.1, ..., 2.16) enthalten, wobei der Hauptstromweg sich zwischen entsprechenden ersten und zweiten Hauptanschlüssen erstreckt, und jede Abzweigung einen Widerstand (3.1, ..., 3.16) enthält, der mit dem ersten Hauptanschluss des betreffenden ersten Transistors verbunden ist, dadurch gekennzeichnet, dass der wenigstens eine Ausgang (27, 28) und der Eingang (26) der Präzisionsstromspiegelschaltung (25) an die zweiten Hauptanschlüsse oder an jene Ausläufer der Widerstände angeschlossen sind, die von den ersten Transistoren mittels des Verbindungsnetzwerks (15) abgewandt sind (Figur 11, 3).

11. Stromquellenanordnung nach Anspruch 10, dadurch gekennzeichnet, dass in wenigstens einigen der Abzweigungen an den von den ersten Transistoren (2.1, ..., 2.16) abgewandten Ausläufern der Widerstände (3.1, ..., 3.16) abgewandten Ausläufern der Widerstände (3.1, ..., 3.16) der Hauptstromweg eines Feldeffekttransistors (13.1—13.6) angeordnet ist, und dieser Weg sich zwischen entsprechenden ersten und zweiten Hauptanschlüssen erstreckt (Figur 1).

12. Stromquellenanordnung nach Anspruch 11, dadurch gekennzeichnet, dass der wenigstens eine Ausgang (27, 28) und der Eingang (26) der Präzisionsstromspiegelschaltung (25) mit den zweiten Hauptanschlüssen der Feldeffekttransistoren (13.1, ..., 13.16) mittels des Verbindungsnetzwerks (15) verbunden sind (Figur 1, 2).

13. Stromquellenanordnung nach Anspruch 11 oder 12, dadurch gekennzeichnet, dass die Ausgänge der Korrekturmittel (18.2, 18.13) mit den Gateelektroden der Feldeffekttransistoren (13.1, ..., 13.16) verbunden sind (Figur 1).

Revendications

1. Configuration de source de courant comportant:

—des moyens pour engendrer une pluralité de courants aux sorties des moyens, courants qui sont dans un rapport de courant donné les uns par rapport aux autres

—des moyens pour détecter des écarts dans les valeurs d'au moins certains des courants par rapport à celles requises pour réaliser le rapport de courant donné et

—des moyens pour corriger lesdits courants afin de réduire les écarts détectés, caractérisé en ce qu'il comprend

—un circuit de miroir de courant de précision (25) présentant une entrée (26) et au moins une sortie (27, 28) à laquelle apparaît un courant dont la valeur présente un rapport très précis par rapport à un courant présent à l'entrée (26),

—un réseau de couplage (15) servant à coupler l'entrée (26) et au moins une sortie (27, 28) du circuit de miroir de courant (25) à un nombre correspondant de sorties des moyens de source de courant (1) selon une configuration cyclique qui est tel qu'à chaque pas d'un cycle, l'entrée (26) dudit circuit de miroir de courant (25) est couplée à une sortie de courant corrigée du moyen de source de courant (1) ou, lorsque le cycle est démarré, à une sortie de courant non corrigée du moyen de source de courant (1) et au moins ladite sortie (27, 28) du circuit de miroir de courant (25) est couplée à une sortie de courant non corrigée du moyen de source de courant et,

—un circuit de détection (81, 82) à chaque sortie (27, 28) du circuit de miroir de courant de précision (25) pour la détection de la différence entre le courant provenant du moyen (1) pour la formation d'une pluralité de courants couplés à ladite sortie (27, 28) et le courant provenant du circuit de miroir de courant (25) et apparaissant à ladite sortie (27, 28) (Fig. 1).



2. Configuration de source de courant selon la revendication 1, caractérisé en ce que le circuit de miroir de courant de précision (25) comporte

—un circuit de répartition de courant muni de plusieurs transistors (30—36) présentant des trajets de courant principal montés parallèlement et des électrodes de commande communes, qui sont commandés par un amplificateur (47) dont l'entrée est couplée à l'entrée (26) du circuit de miroir de courant (25), et

—un circuit de permutation (50) pour la transmission des courants provenant du circuit de répartition de courant à l'entrée (26) et à au moins une sortie (27, 28) du circuit de miroir de courant (25), conformément à une permutation circulaire (Fig. 1).

3. Configuration de source de courant selon la revendication 1 ou 2, caractérisé en ce que chaque circuit de détection (81, 82) comporte un premier convertisseur de courant-tension (Figure 1).

4. Configuration de source de courant selon la revendication 3, caractérisé en ce que chaque premier convertisseur courant tension (81, 82) est muni d'un amplificateur (83, 86) ayant une première entrée, qui est couplée à la sortie correspondante (27, 28) du circuit de miroir de courant (25), d'une deuxième entrée, qui présente une tension de référence, et d'une sortie (85, 88) qui est couplée à la première entrée de l'amplificateur par l'intermédiaire d'un condensateur de rétroaction (84, 87) (Fig. 1).

5. Configuration de source de courant selon la revendication 4, caractérisé en ce que la sortie de l'amplificateur est couplée à une première entrée d'un comparateur (120, 121), qui présente une deuxième entrée présentant une tension de référence (Figure 2).

6. Configuration de source de courant selon la revendication 3 ou 4, caractérisé en ce que le moyen pour la correction des courants (182, 183) comporte un deuxième convertisseur courant-tension correspondant à chaque courant à corriger, deuxième convertisseur de courant tension qui est muni d'un amplificateur (192, 193) présentant une sortie qui est couplée à une première entrée de l'amplificateur par l'intermédiaire d'un condensateur de rétroaction (202, 203), cette première entrée pouvant être couplée à la sortie du premier convertisseur de courant de tension (82, 83) à l'aide d'un condensateur de commutation (212, 213) (Fig. 1).

7. Configuration de source de courant selon la revendication 5, caractérisé en ce que les moyens pour la correction de courant sont constitués par un circuit de comptage (14.1—14.16) correspondant à chaque courant à corriger, circuit de comptage qui peut être couplé à la sortie du premier convertisseur de courant de tension (81,

82) à l'aide d'un commutateur (91, 92) et qui engendre plusieurs signaux logiques suivant le signal logique présent à la sortie du comparateur (120, 121), signaux qui sont convertis, à l'aide d'un convertisseur numérique-analogique (14.21—14.36), en un signal de sortie analogique permettant de corriger le courant en question.

8. Configuration de source de courant selon l'une des revendications précédentes, caractérisé en ce que les moyens (1) pour engendrer plusieurs courants comportent des moyens pour engendrer au moins une pluralité de courants, dont les valeurs varient conformément à une série pondérée de façon binaire (Fig. 1).

9. Configuration de source de courant selon l'une des revendications précédentes 1 à 7, caractérisé en ce que les moyens (1) pour engendrer plusieurs courants sont constitués par des moyens pour engendrer plusieurs courants de valeurs pratiquement égales (Fig. 5).

10. Configuration de source de courant selon la revendication 8 ou 9, dont les moyens pour engendrer plusieurs courants sont munis d'une pluralité de branches parallèles, comportant chacune le trajet de courant principal d'un premier transistor respectif (2.1—2.16), ce trajet de courant principal s'étendant entre les première et deuxième bornes principales respectives, chaque branche comportant une résistance (3.1—3.16) qui est couplée à la première borne principale du premier transistor correspondant, caractérisé en ce qu'au moins une sortie (27, 28) et l'entrée (26) du circuit de miroir de courant de précision (25) sont couplées auxdites deuxième bornes principales ou aux extrémités des résistances opposées des premiers transistors à l'aide du réseau de couplage (15) (Fig. 1, 3).

11. Configuration de source de courant selon la revendication 10, caractérisé en ce que dans au moins certaines des branches aux extrémités des résistances (3.1—3.16) opposées des premiers transistors (2.1—2.16), est disposé le trajet de courant principal d'un transistor à effet de champ (13.1—13.16), trajet qui s'étend entre les première et deuxième bornes principales respectives (Fig. 1).

12. Configuration de source de courant selon la revendication 11, caractérisé en ce qu'au moins une sortie (27, 28) et l'entrée (26) du circuit de miroir de courant de précision (25) sont couplées aux deuxième bornes principales des transistors à effet de champ (13.1—13.16) à l'aide du réseau de couplage (15) (Fig. 1, 2).

13. Configuration de source de courant selon la revendication 1 ou 12, caractérisé en ce que les sorties des moyens de correction (18.2, 18.3) sont couplées aux électrodes de porte des transistors à effet de champ (13.1—13.16) (Fig. 1).

