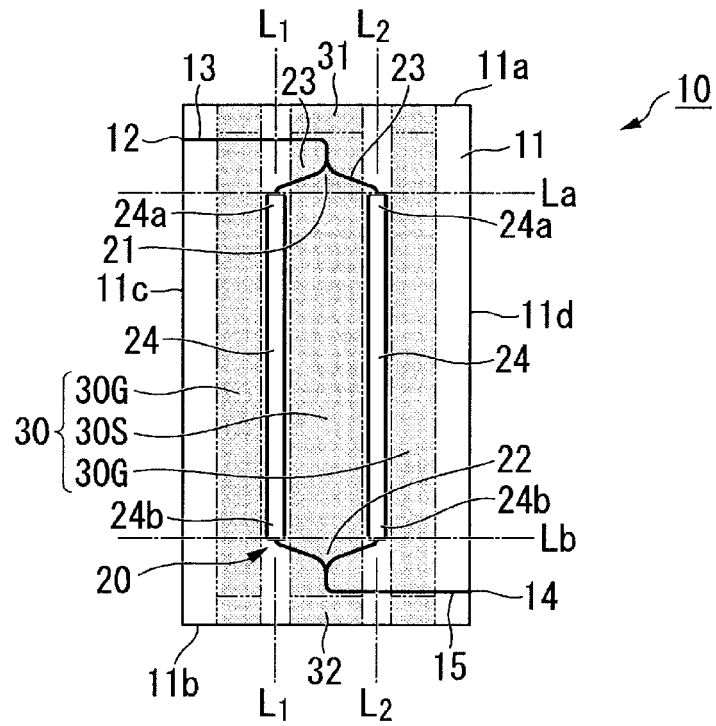
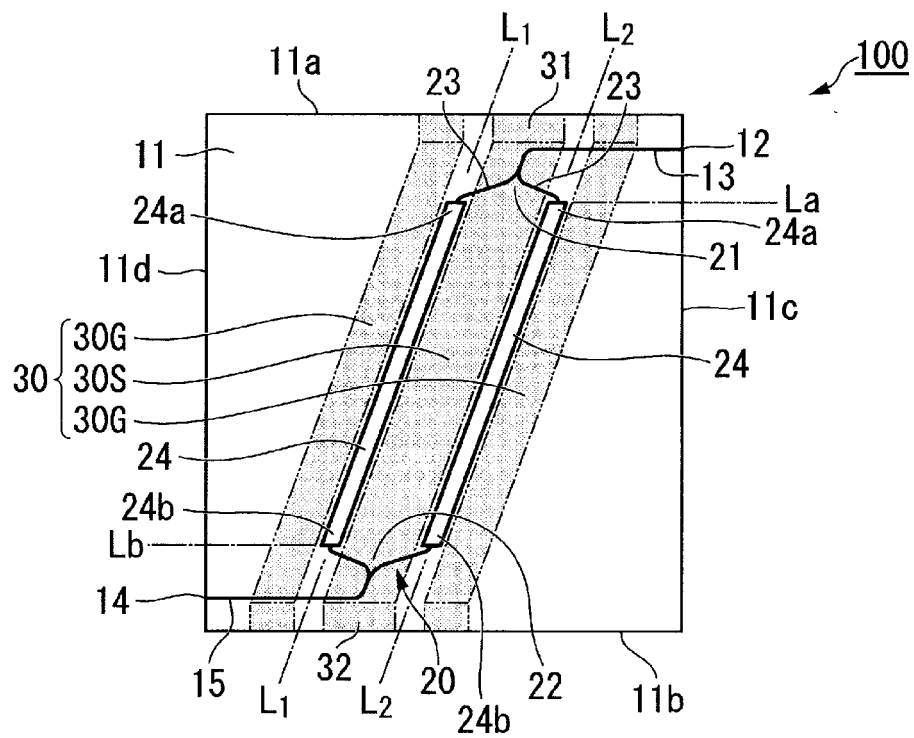


[図1A]



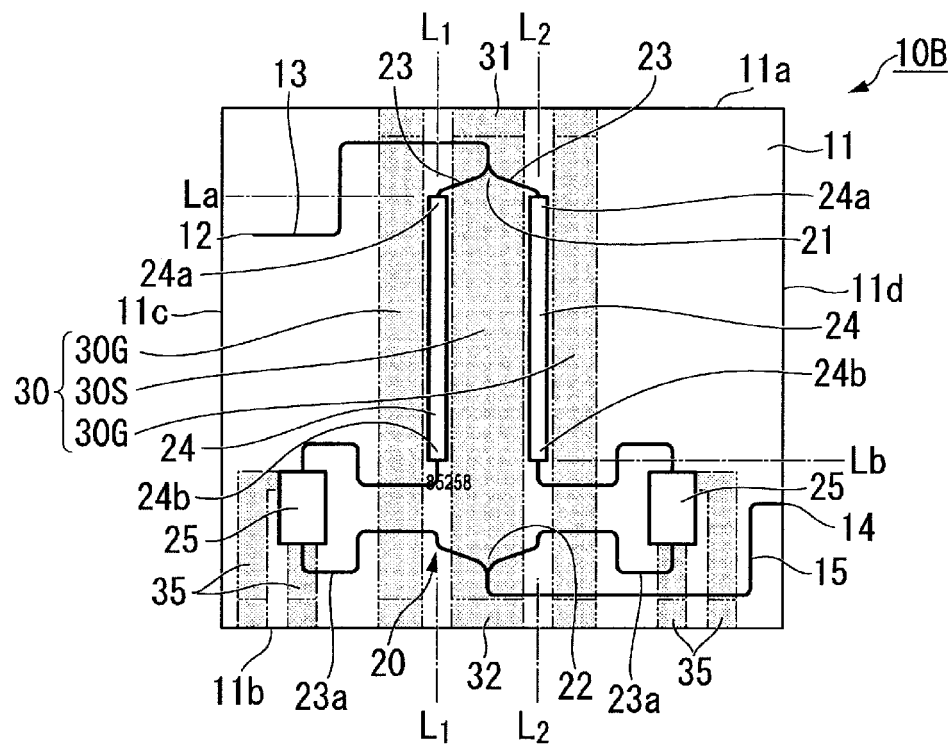
[図1B]



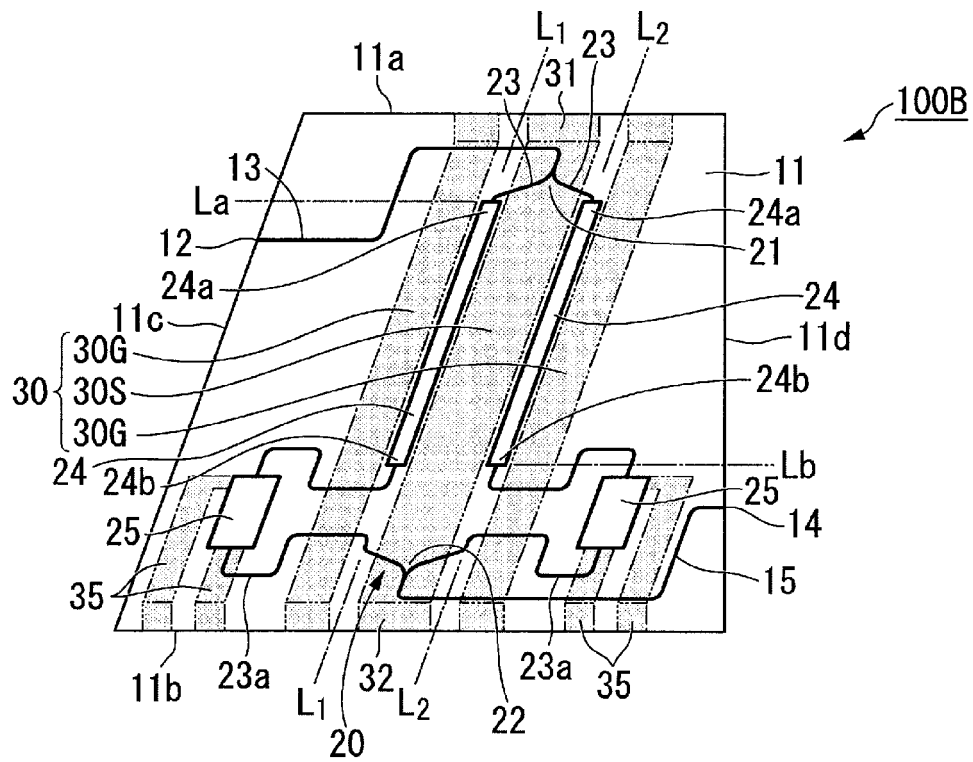
A cross-sectional view of a semiconductor device. A central gate structure 120 is formed on a substrate 110. The gate structure 120 includes a gate dielectric layer 124 and a gate electrode 130G. The gate electrode 130G is divided into a top portion 130S and a bottom portion 130B. The gate structure 120 is surrounded by a gate sidewall 113. The gate sidewall 113 is formed on a gate spacer 112. The gate spacer 112 is formed on a gate pad 114. The gate pad 114 is formed on a gate contact 115. The gate contact 115 is formed on a gate electrode 130G. The gate electrode 130G is divided into a top portion 130S and a bottom portion 130B. The gate structure 120 is surrounded by a gate sidewall 113. The gate sidewall 113 is formed on a gate spacer 112. The gate spacer 112 is formed on a gate pad 114. The gate pad 114 is formed on a gate contact 115. The gate contact 115 is formed on a gate electrode 130G. The gate electrode 130G is divided into a top portion 130S and a bottom portion 130B.

[illegible]

[図4A]

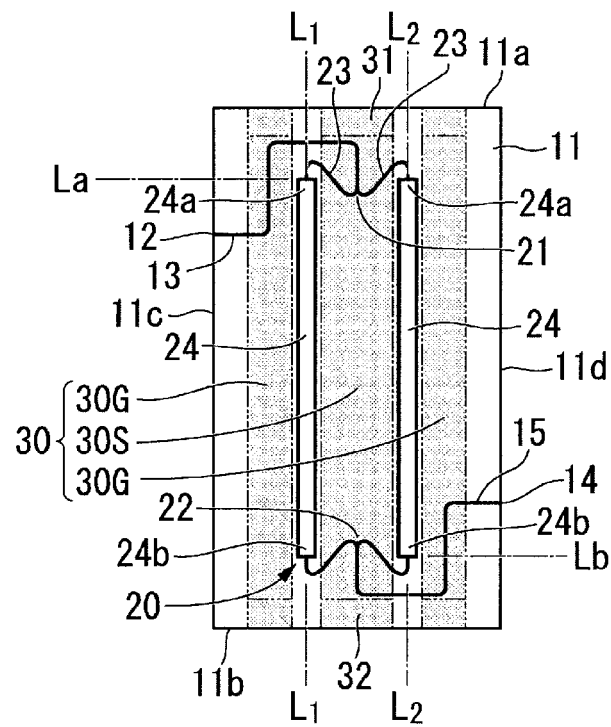


[図4B]

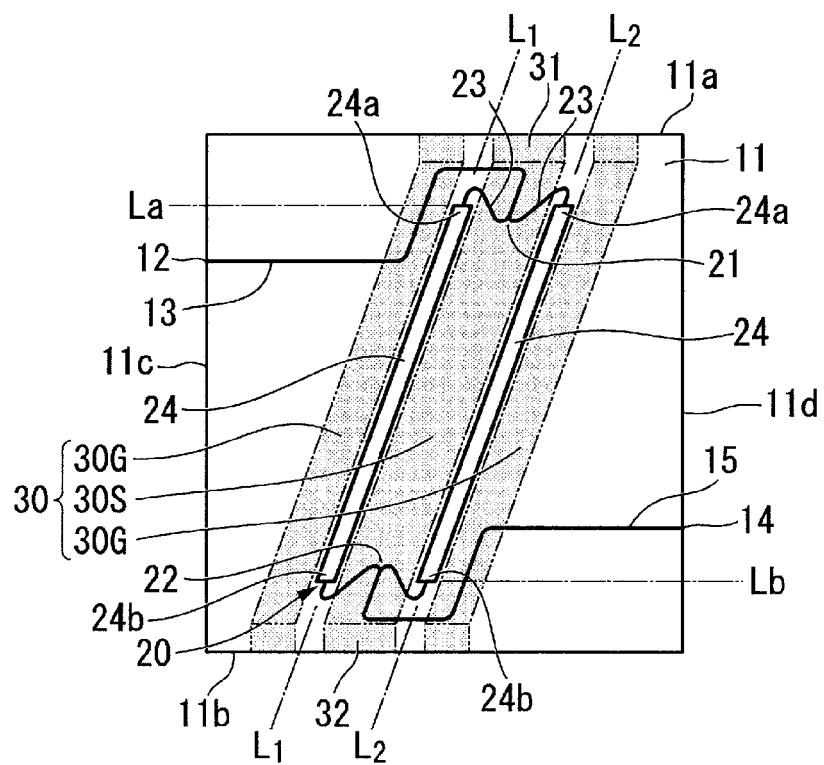


[illegible]

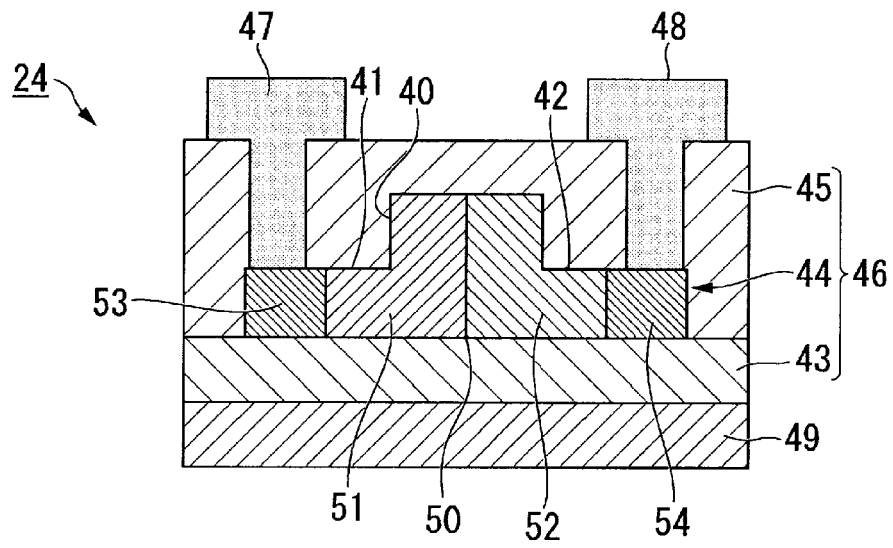
10D



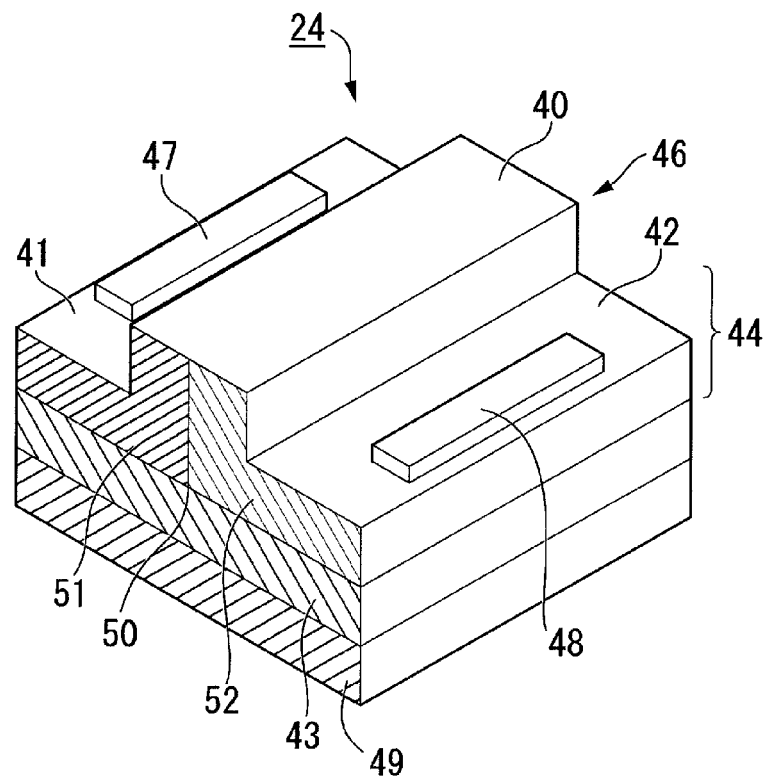
100D



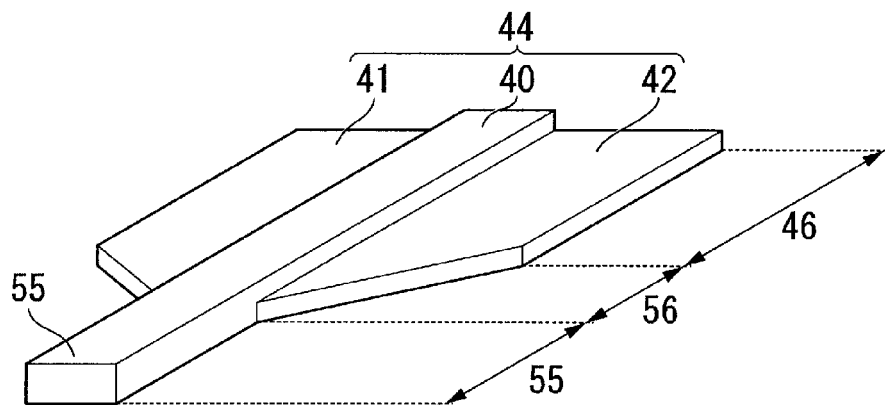
[図7]



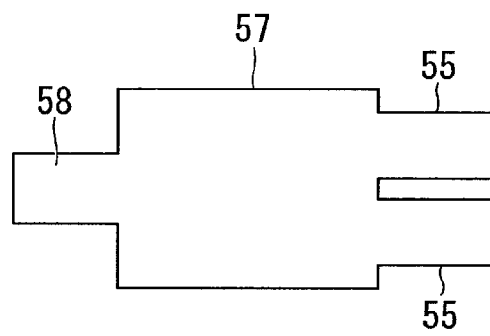
[図8]



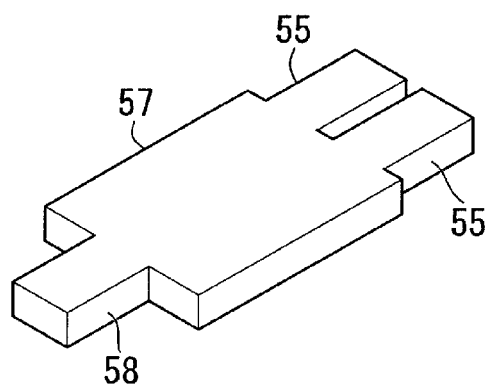
[図9]



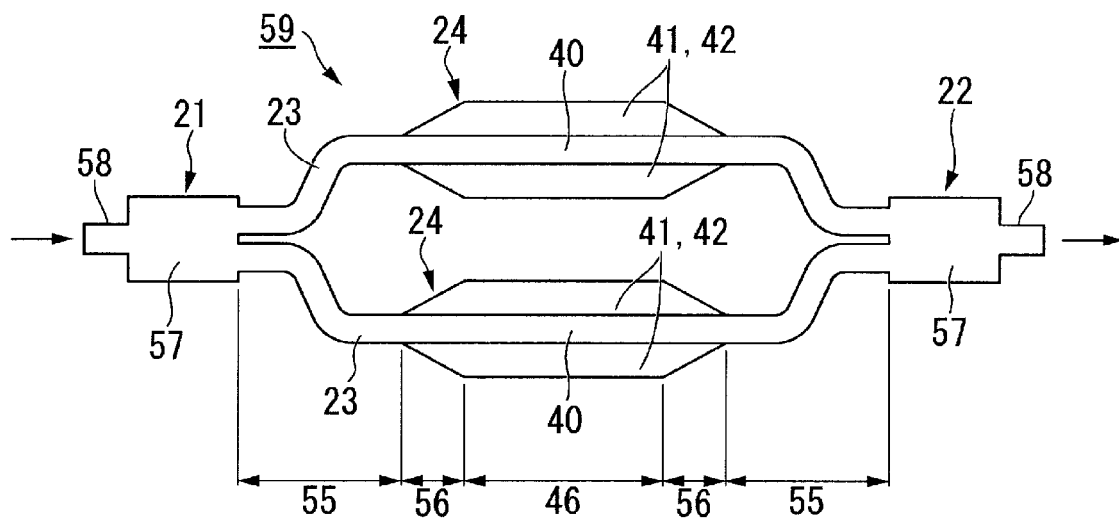
[図10A]



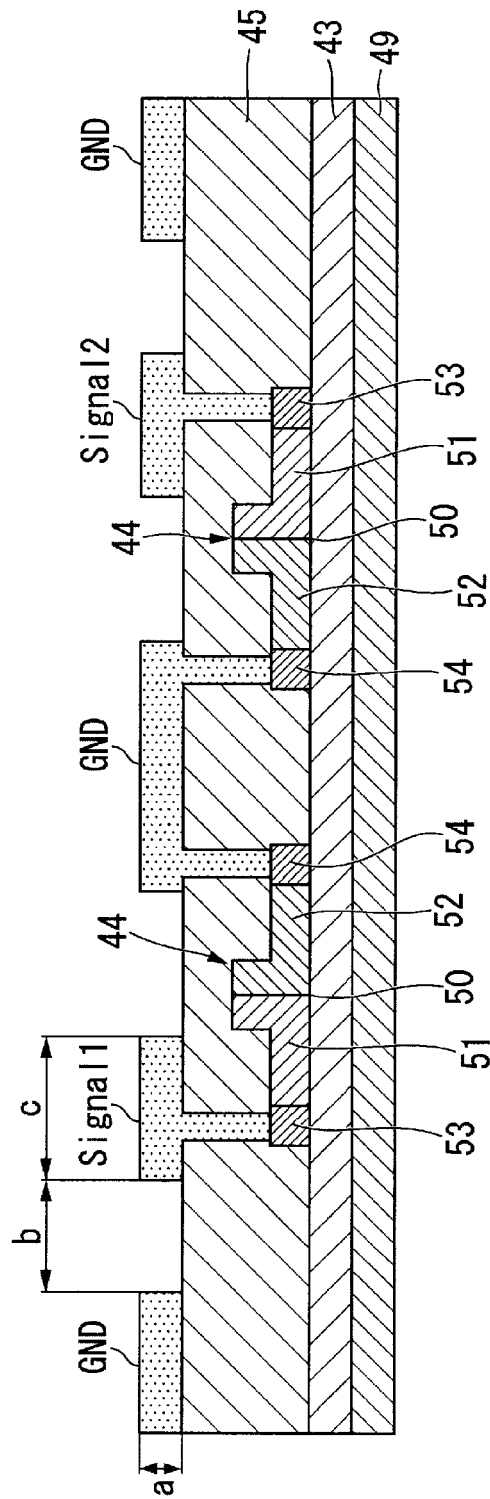
[図10B]



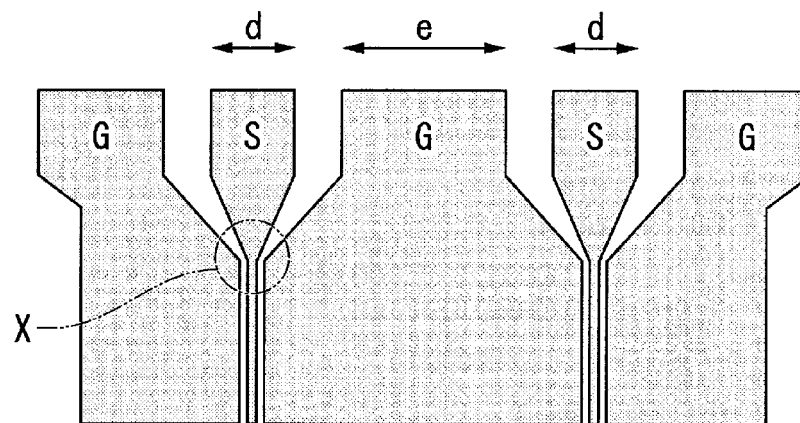
[図11]



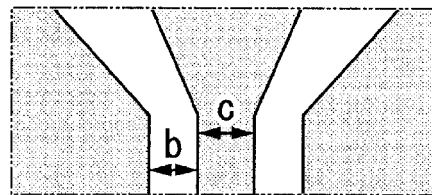
[図12]



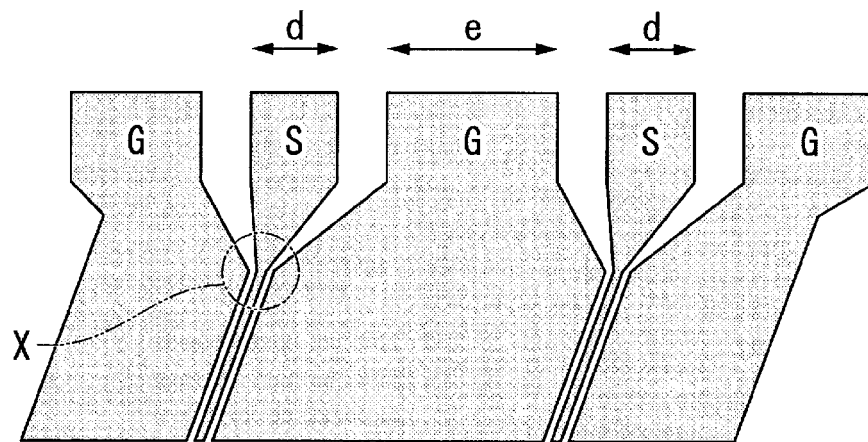
[図13A]



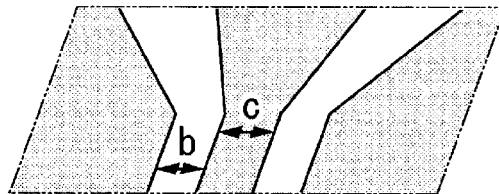
[図13B]



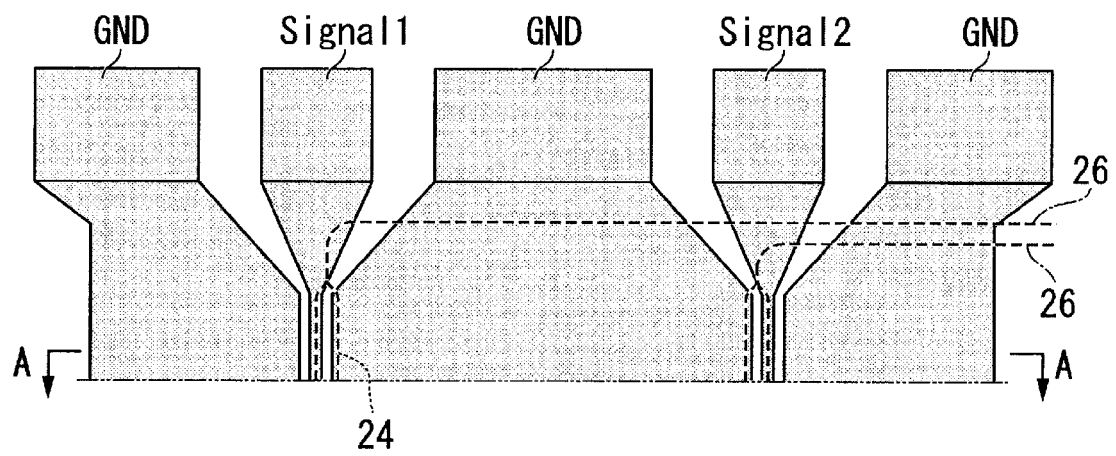
[図13C]



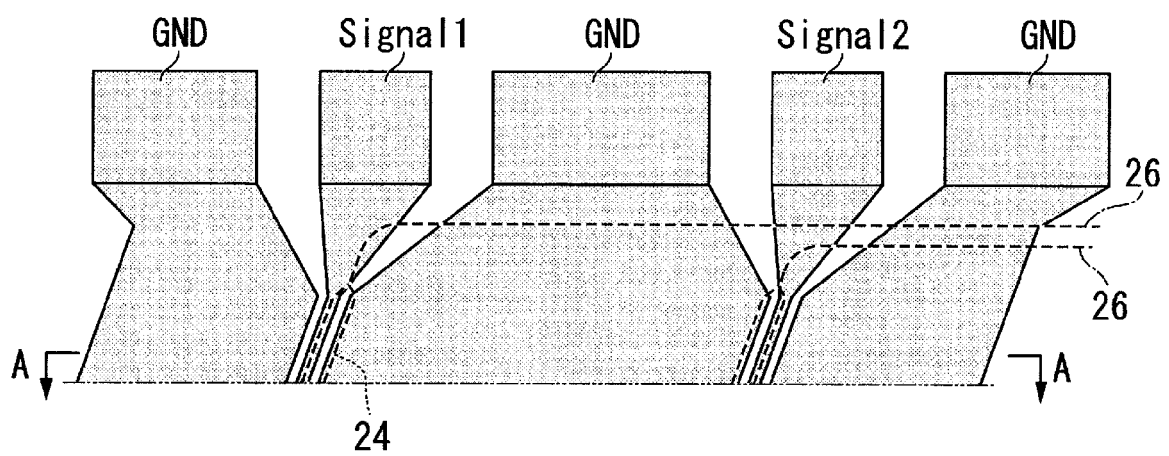
[図13D]



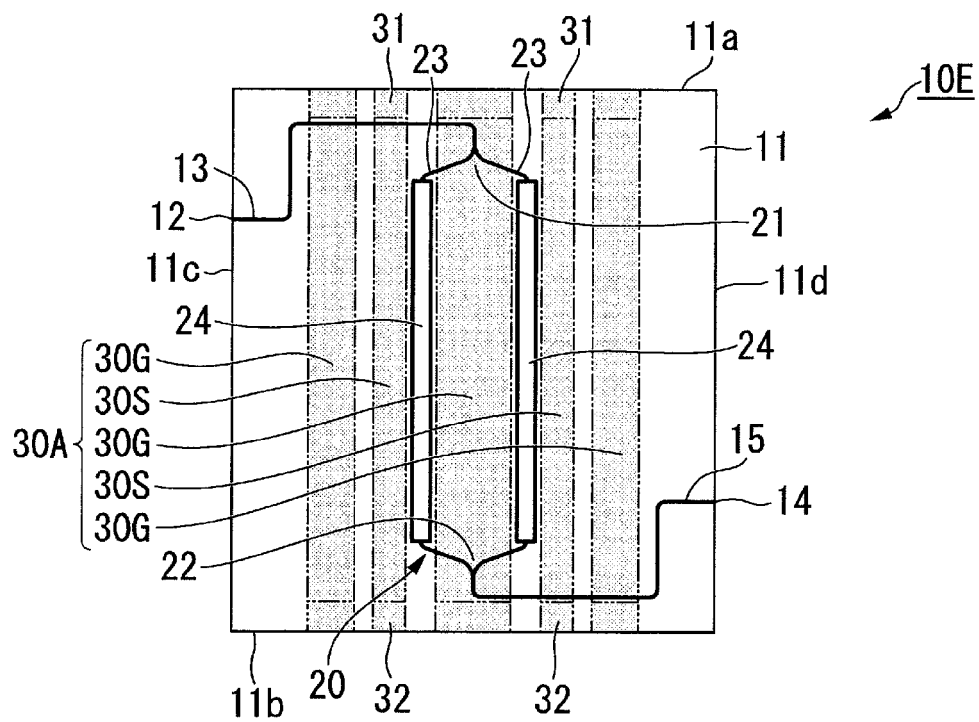
[図14A]



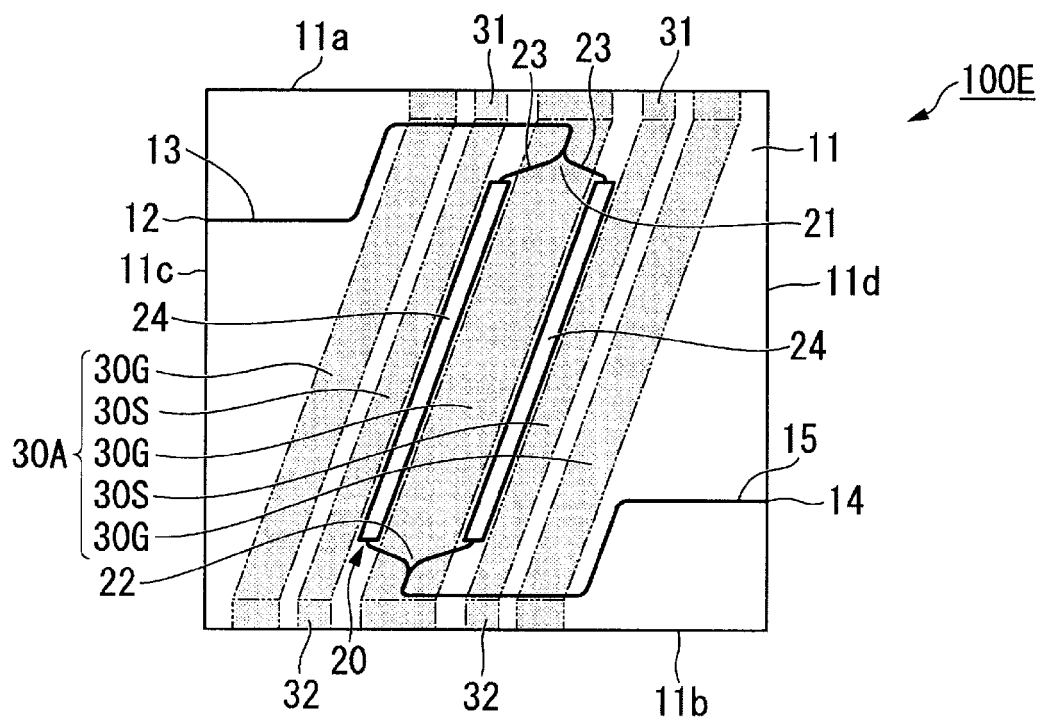
[図14B]



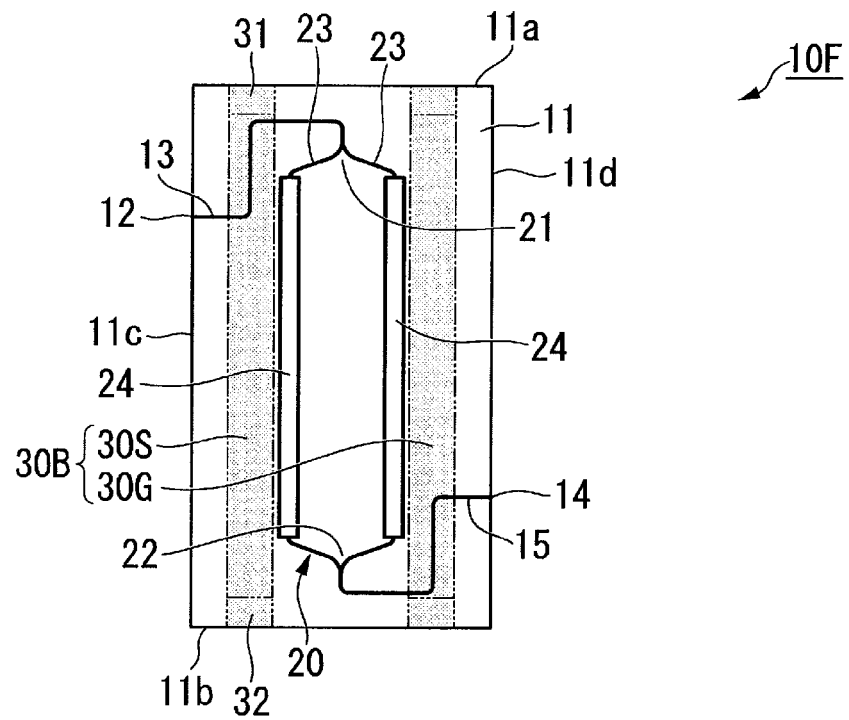
[図15A]



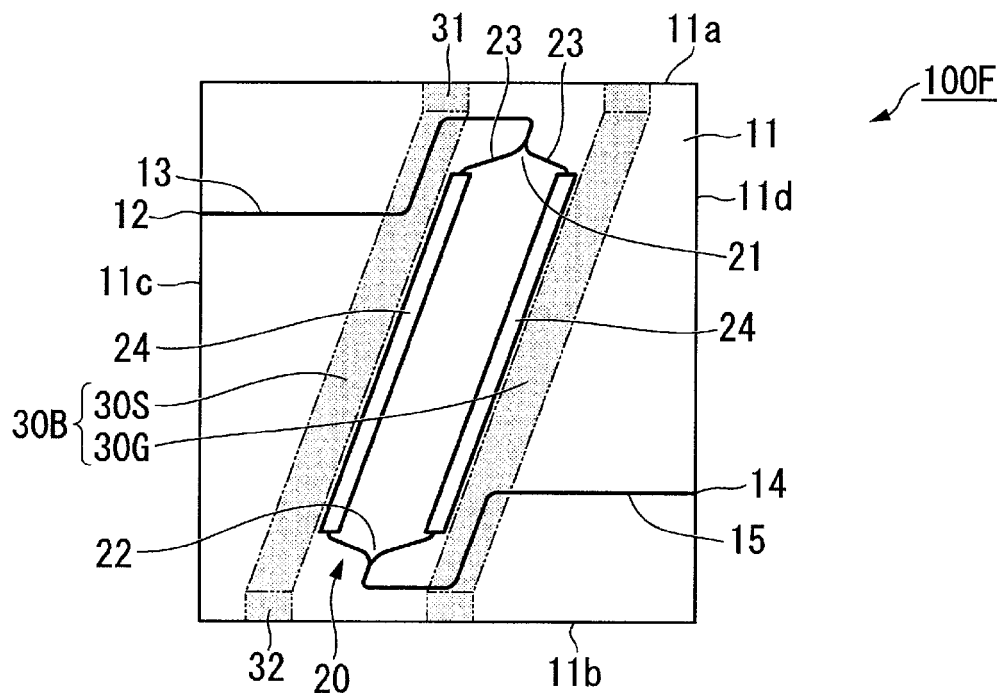
[図15B]



[図16A]

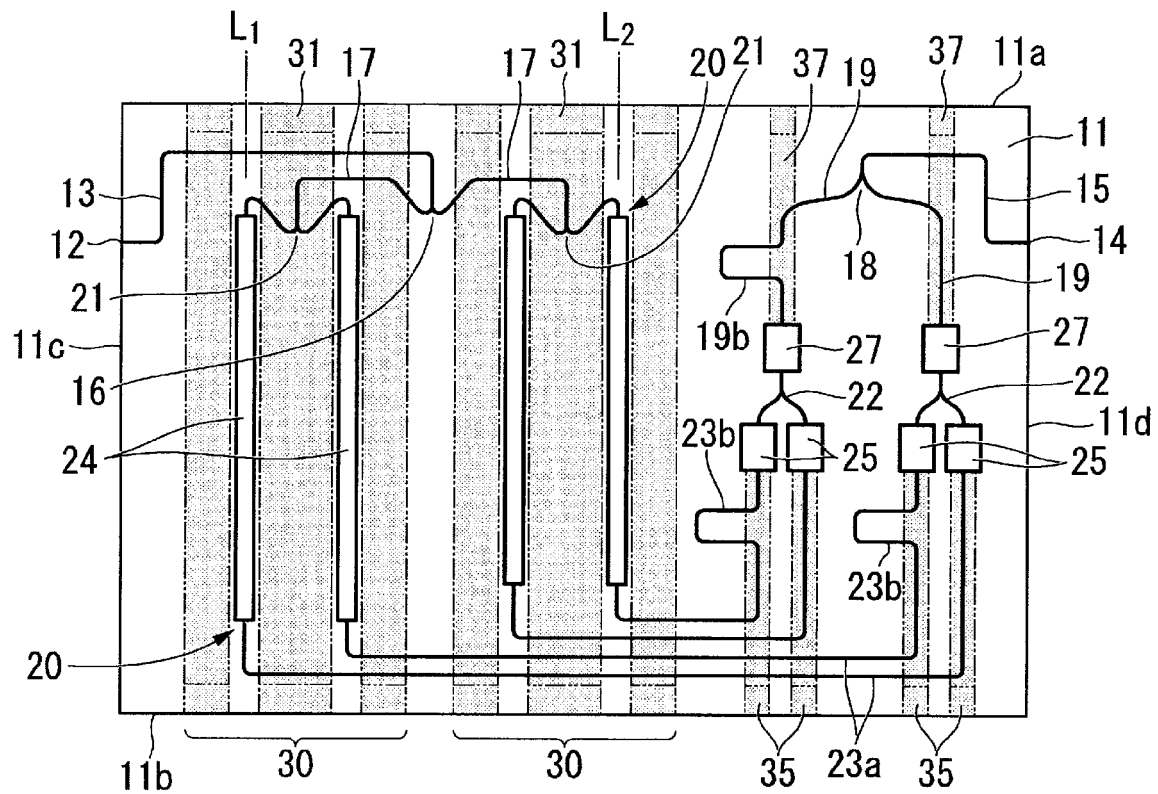


[図16B]

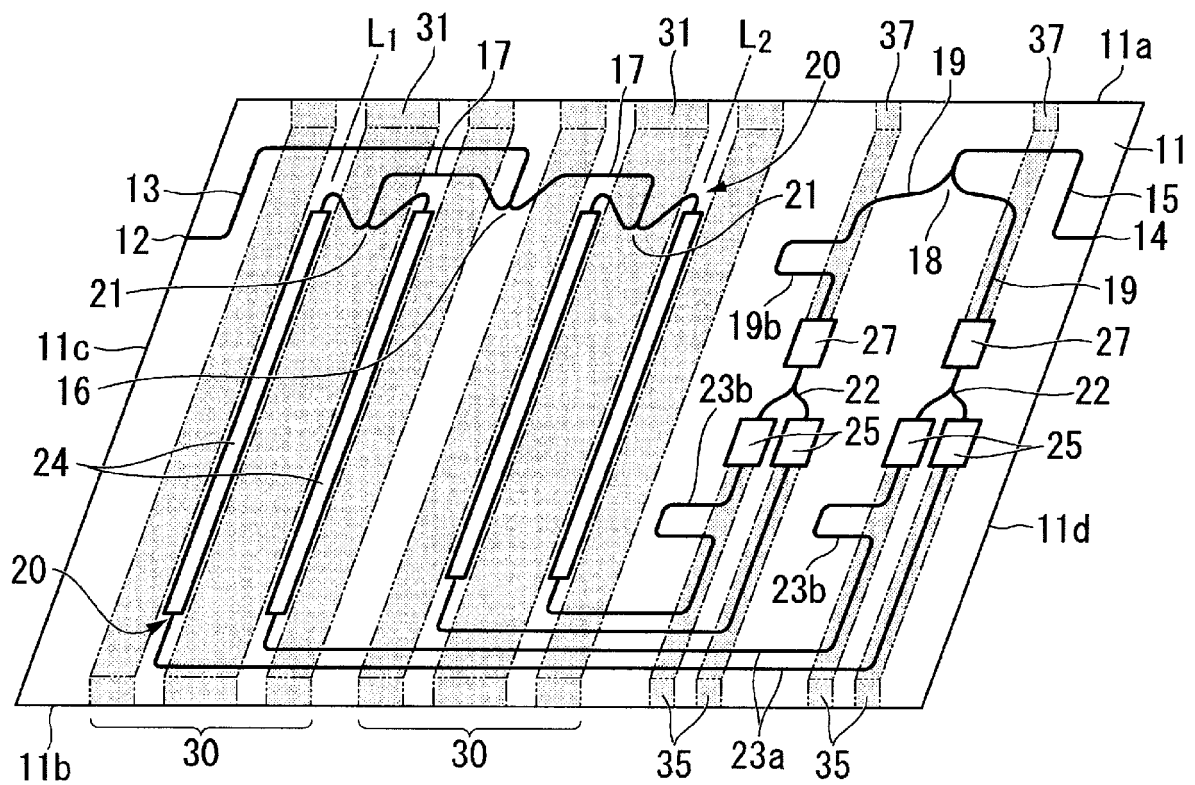


This plan view shows a semiconductor device with two pairs of vertical electrodes, labeled 11b and 11c. Each pair is connected to a common horizontal line 12. The electrodes are connected to a central circuit block 19 via lines 20 and 21. The circuit block 19 includes components 14, 15, 18, 19a, 19b, 19c, and 27. The device is divided into regions 11a, 11b, 11c, and 11d. The electrodes are labeled L1, L2, and 31. The central circuit block is labeled 19. The device is divided into regions 11a, 11b, 11c, and 11d. The electrodes are labeled L1, L2, and 31. The central circuit block is labeled 19. The device is divided into regions 11a, 11b, 11c, and 11d. The electrodes are labeled L1, L2, and 31. The central circuit block is labeled 19.

[図18A]



[図18B]

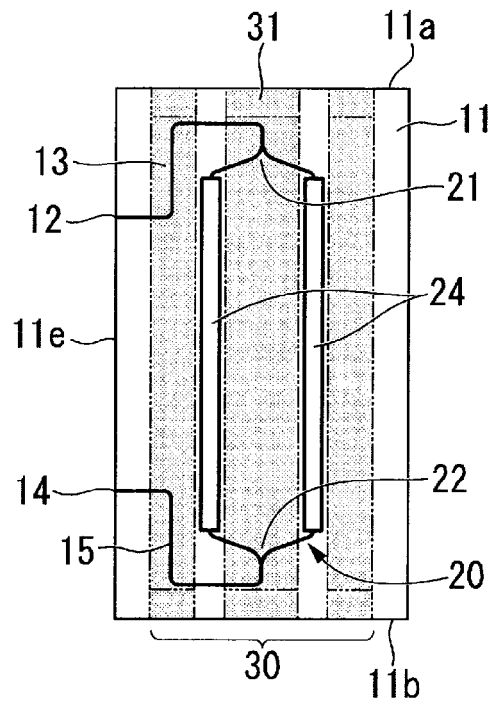


The diagram shows a perspective view of a semiconductor device 10. It includes a substrate 11 with a top surface 11a and a bottom surface 11b. Four parallel strips of conductive material 16 are disposed on the top surface. Each strip has a central raised portion 17A and side portions 17. These strips are connected to a common bus 18 through contact pads 19a, 19b, and 19c. The bus 18 is connected to a series of resistors 20 and capacitors 21. A passivation layer 13 covers the top surface. Other features include vias 22, 23a, and 23b, and various interconnects labeled L1, L2, and L3.

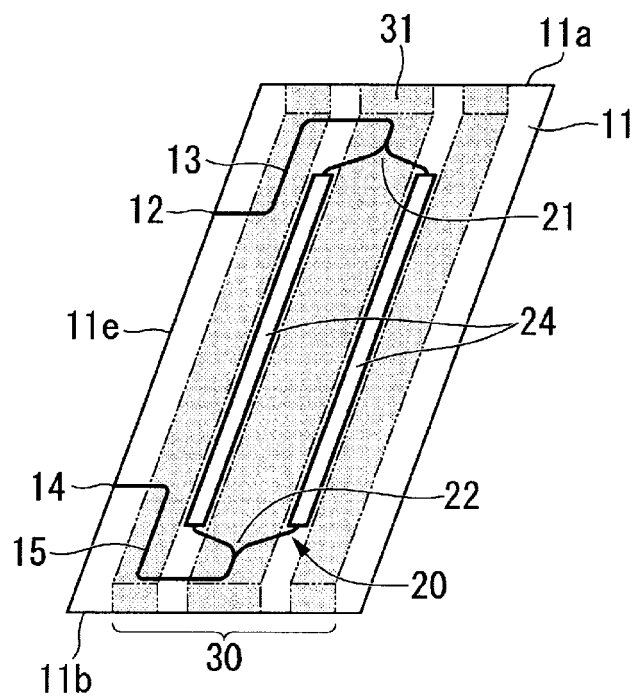




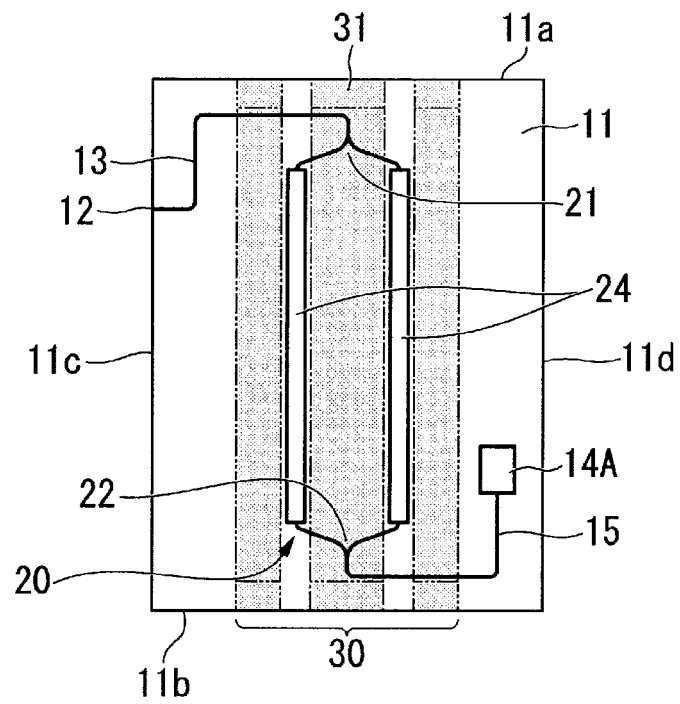
[図22A]



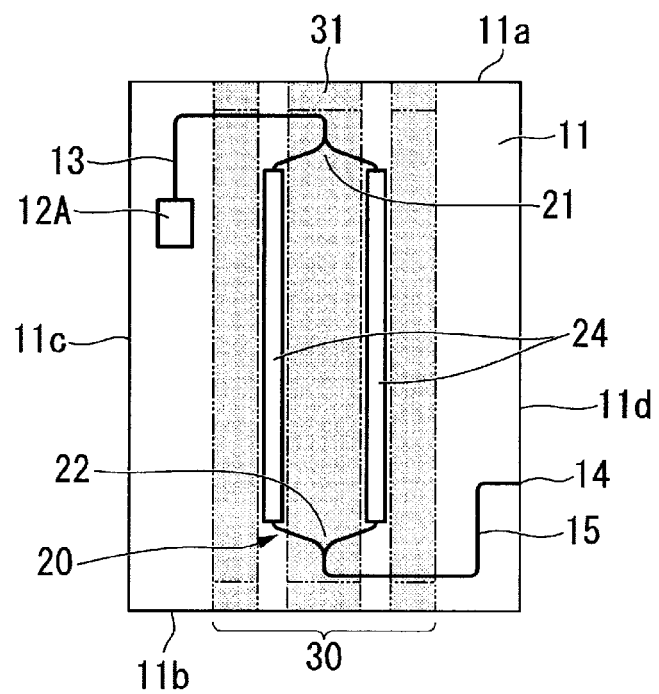
[図22B]



[図23A]



[図23B]

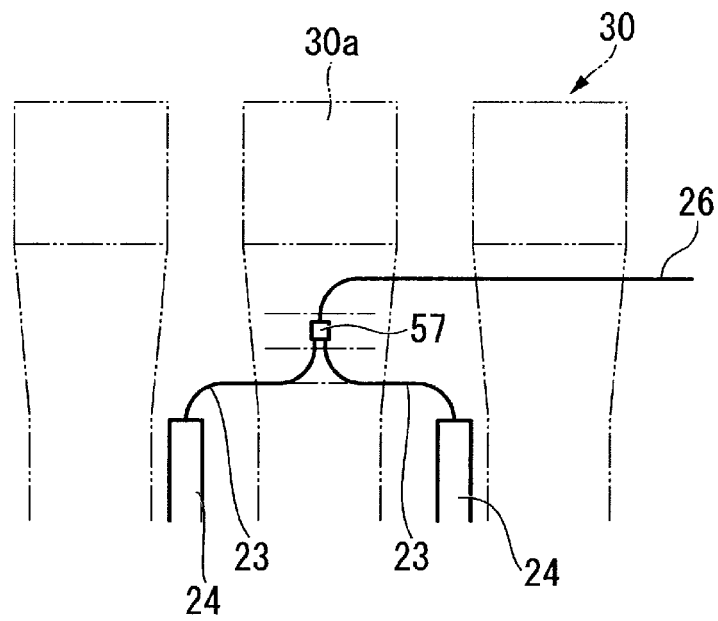




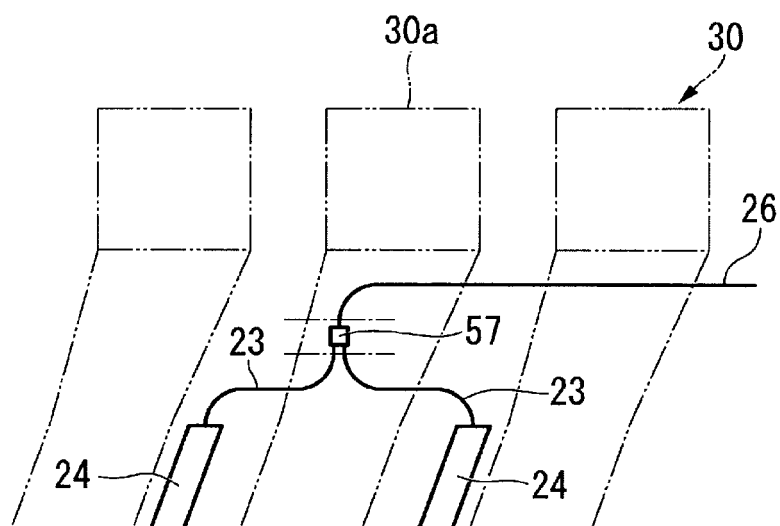




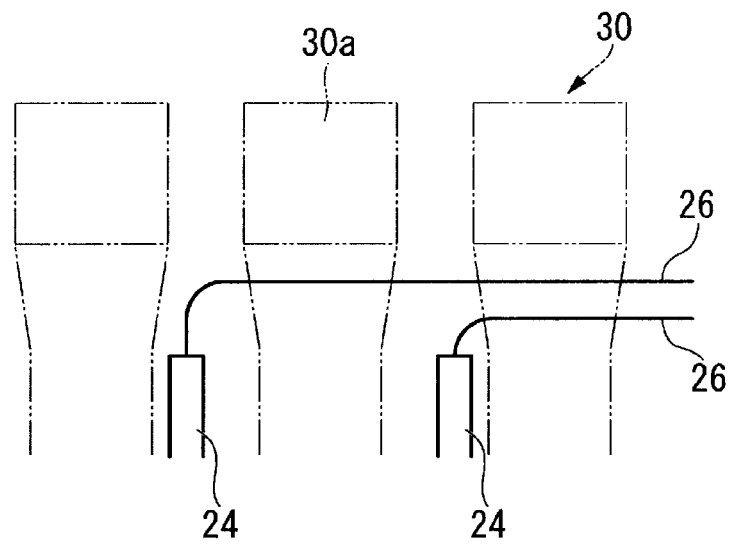
[図25A]



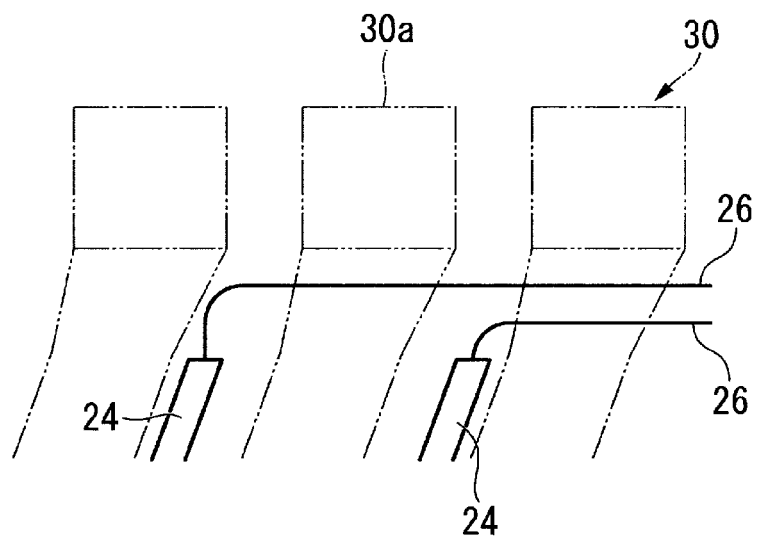
[図25B]



[図26A]

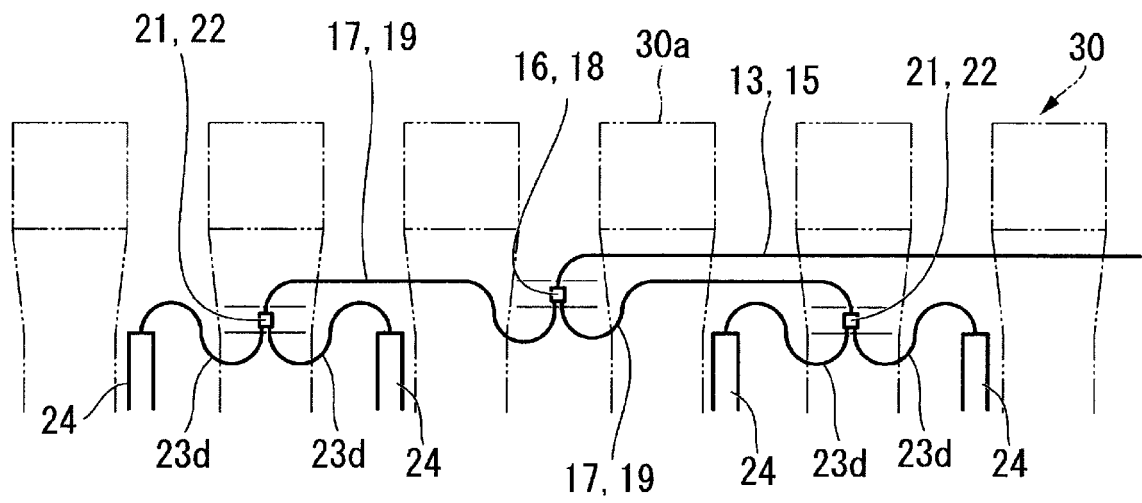


[図26B]

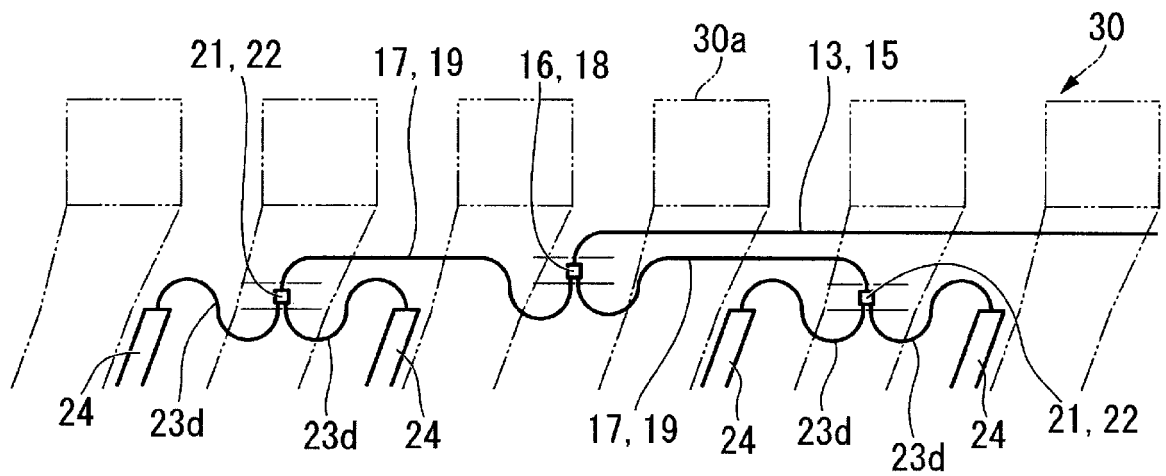




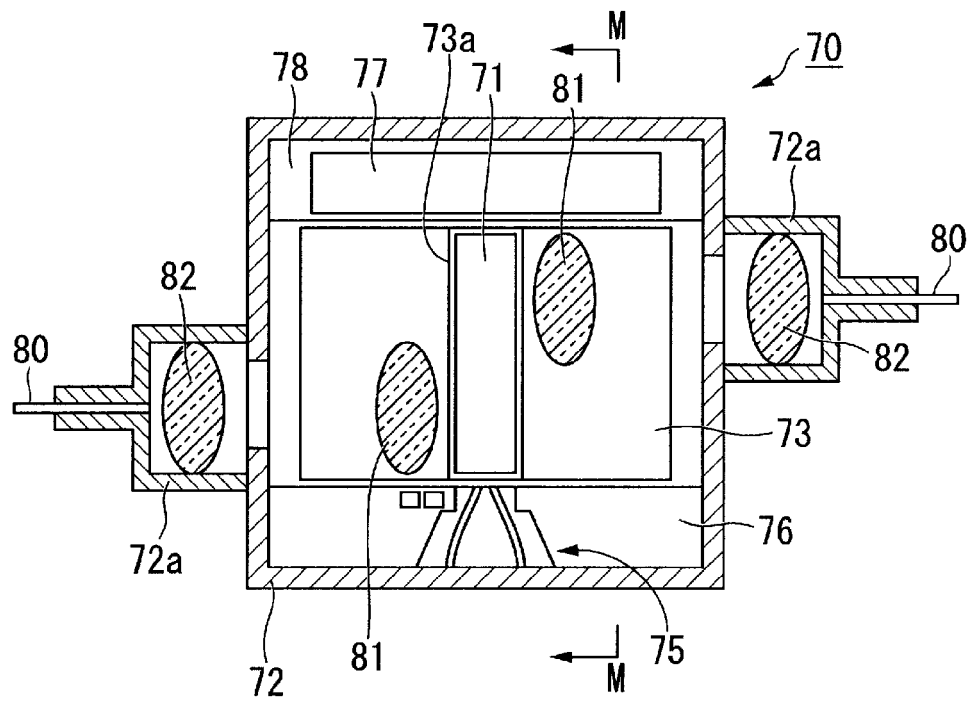
[図28A]



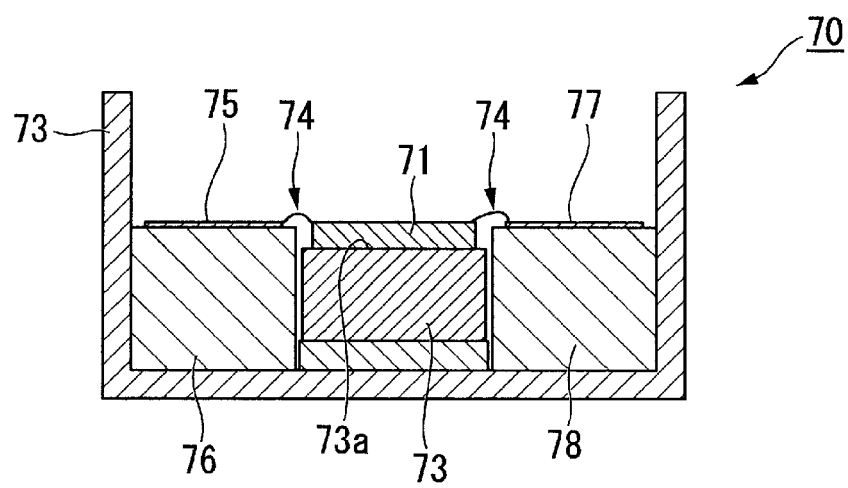
[図28B]



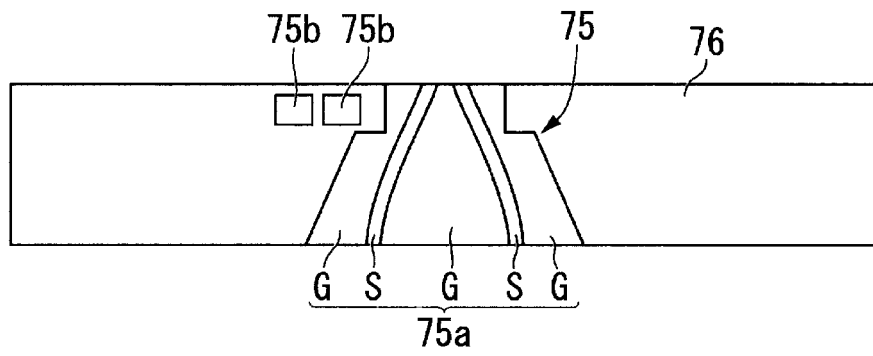
[図29]



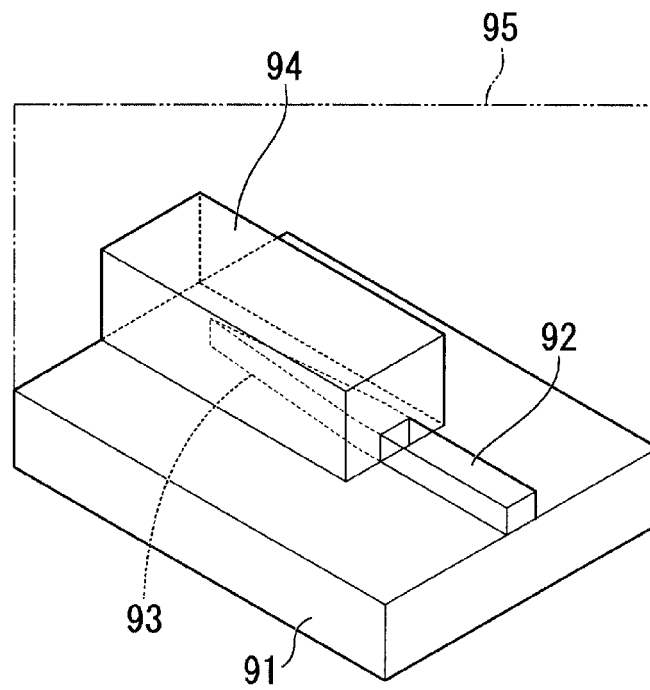
[図30]



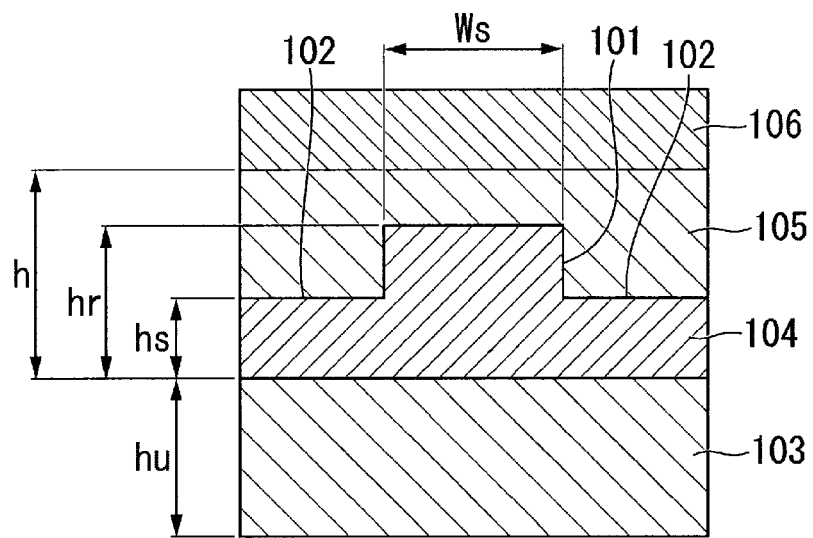
[図31]



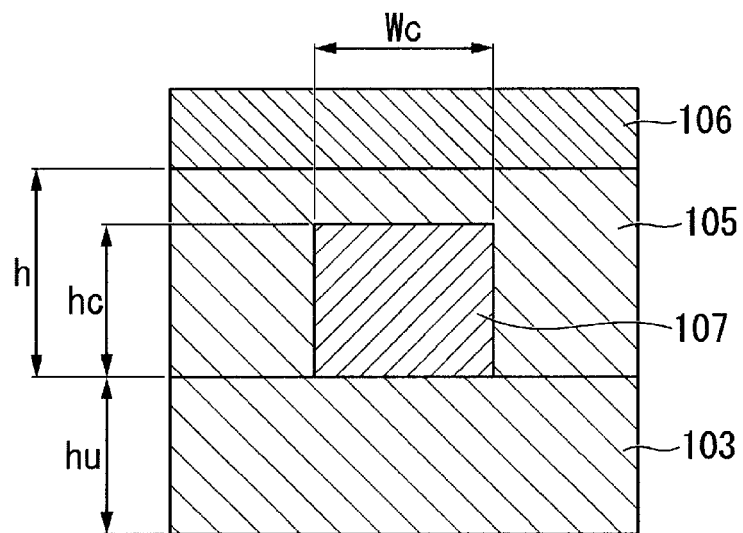
[図32]



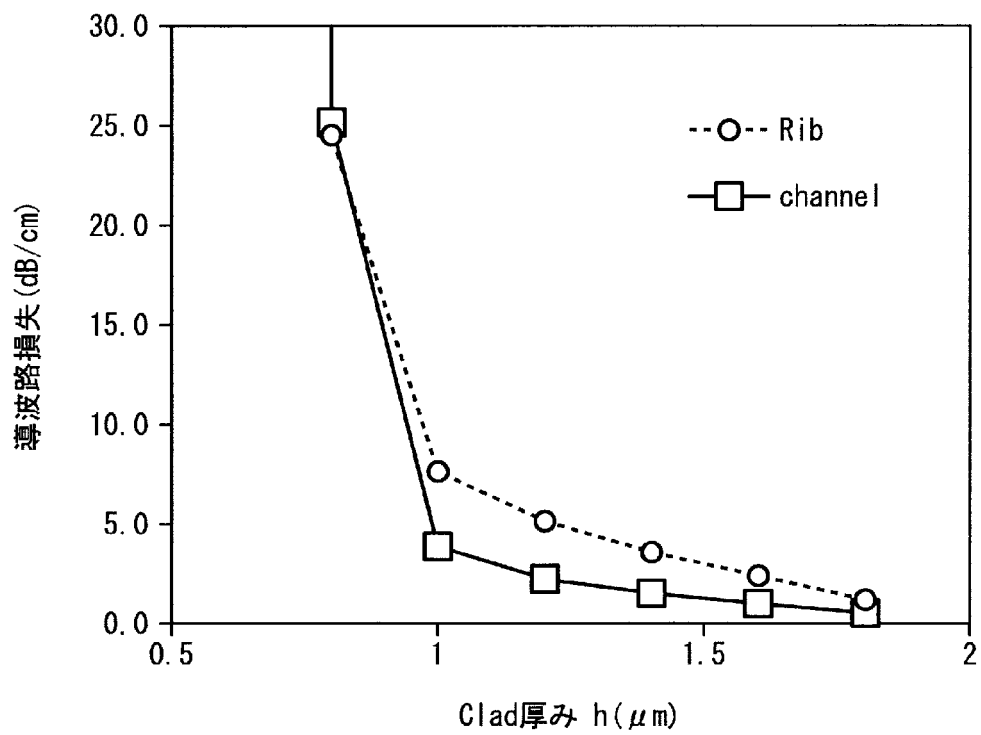
[図33A]



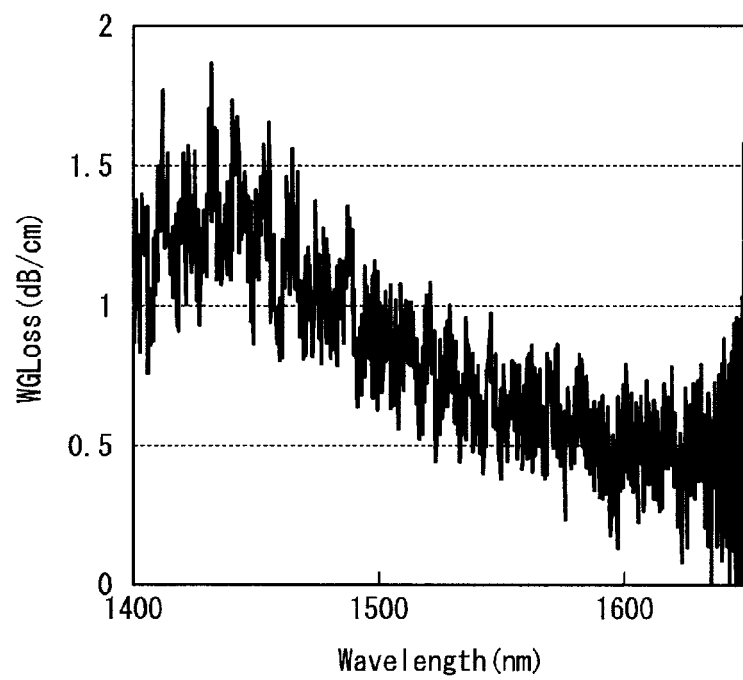
[図33B]



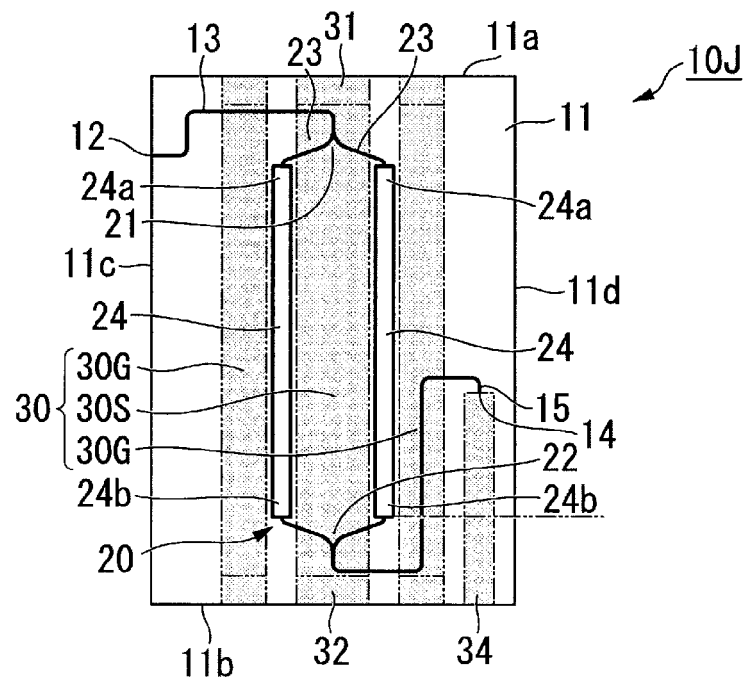
[図34]



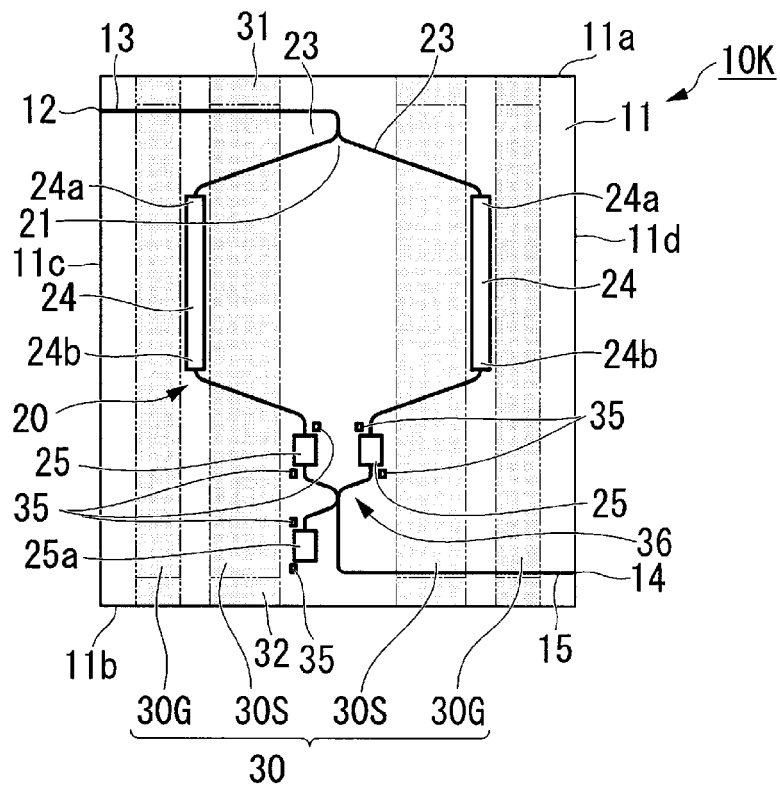
[図35]



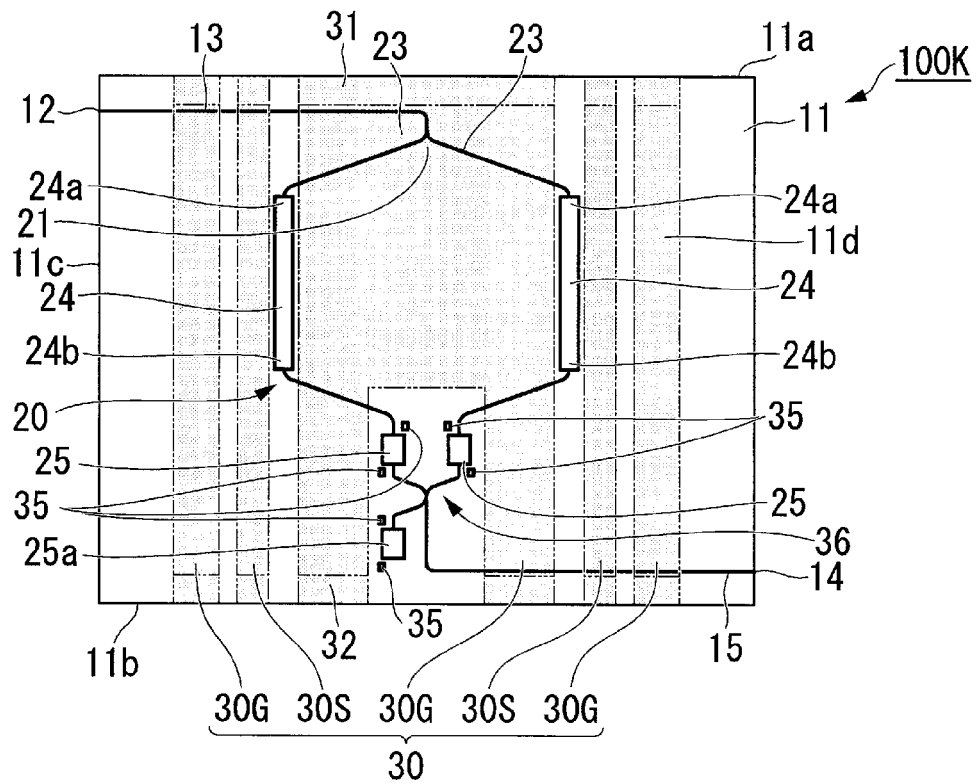
[illegible][illegible]



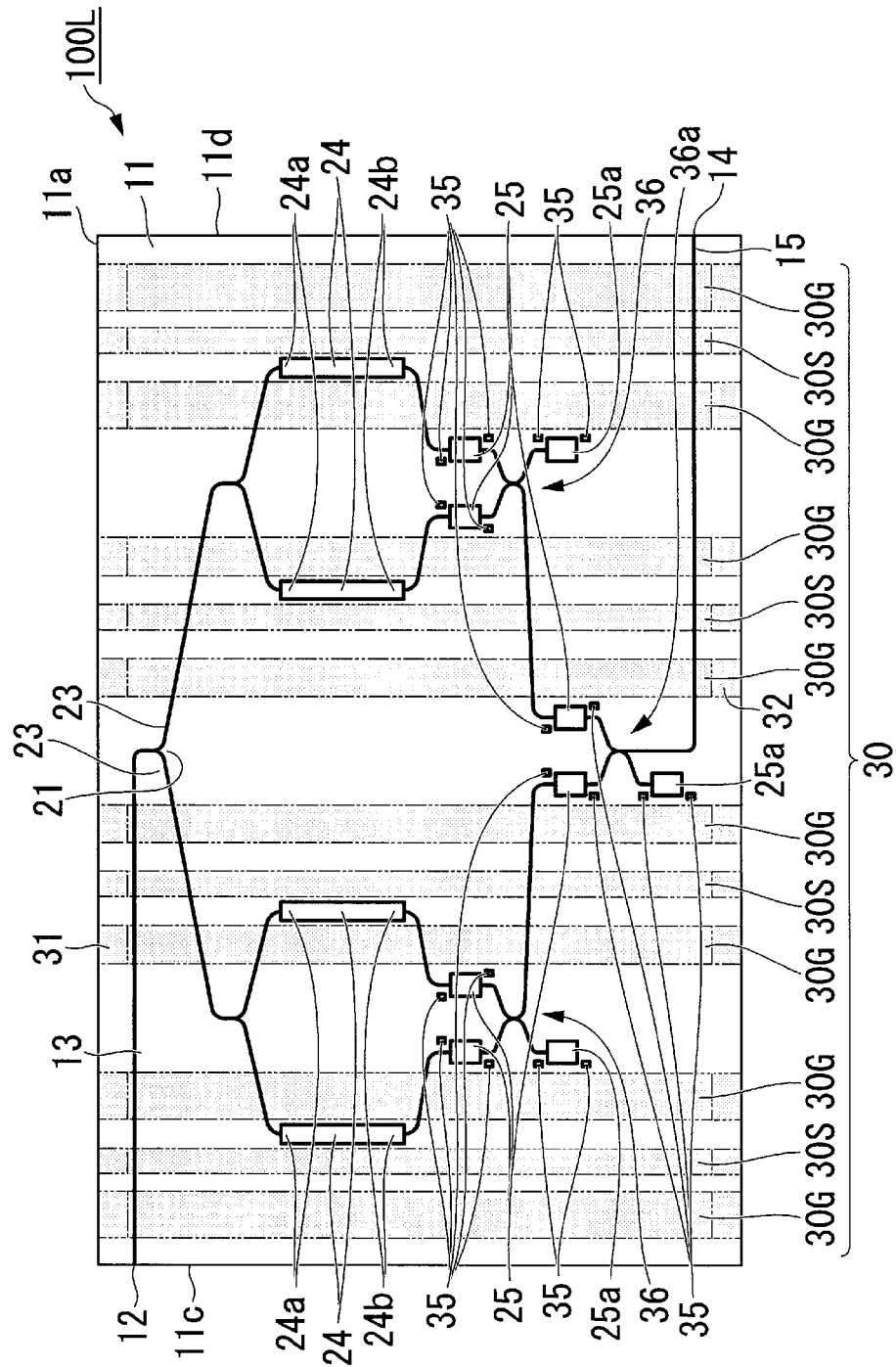
[図40A]



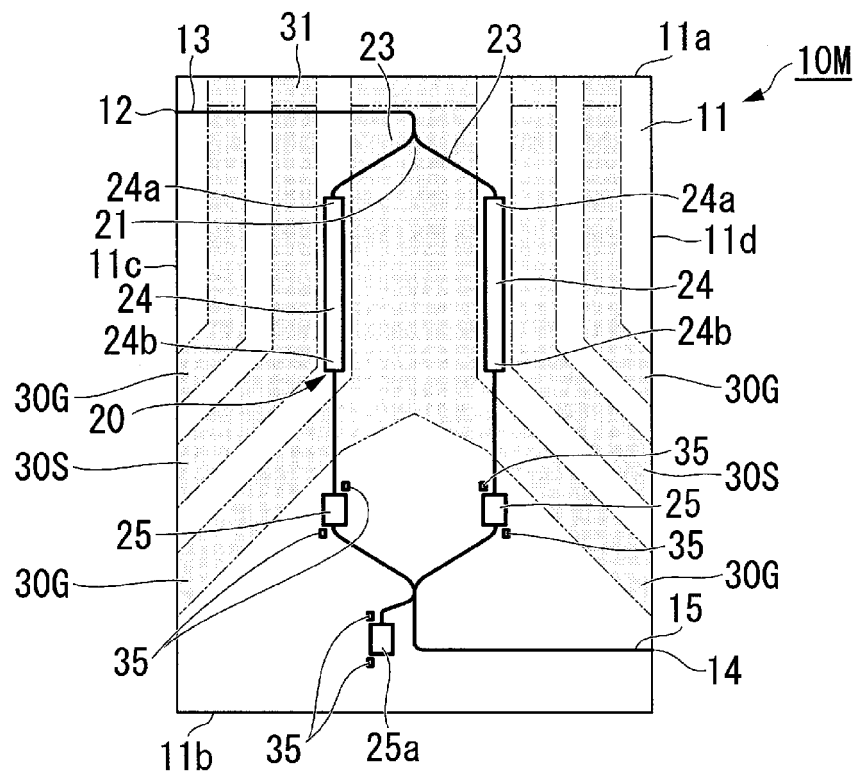
[図40B]



[図41]



[図42A]



[図42B]

