

ABSTRACT

CELL BOTTOM NODE RESET IN A MEMORY ARRAY

Methods, systems, and devices for cell bottom node reset in a memory array are described. The memory array may include a plurality of ferroelectric memory cells having a cell bottom node and a cell plate opposite the cell bottom node. A zero voltage may be applied to a plurality of digit lines in the memory array. A plurality of word lines may be activated to electrically coupled the plurality of digit lines to cell bottom node of each of the ferroelectric memory cells. Accordingly, the cell bottom node of each of the ferroelectric memory cells may be reset to the zero voltage.

Figure 4