CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate comprising a memory cell region and a connection region;

a plurality of gate lines vertically overlapping each other in the memory cell region, each gate line comprising a first metal;

a stepped connection unit in the connection region comprising a plurality of conductive pad regions, each conductive pad region integrally connected to a respective gate line of the plurality of gate lines and comprising the first metal;

a plurality of contact structures vertically overlapping the stepped connection unit, each contact structure connected to a respectively corresponding conductive pad region of the plurality of conductive pad regions and comprising a second metal; and

at least one metal silicide layer between each of the plurality of contact structures and the respectively corresponding conductive pad regions,

wherein an uppermost surface of each of the metal silicide layers is equal to or lower than an uppermost surface of the respectively corresponding conductive pad region and a bottom surface of each of the metal silicide layers is above a lower surface of the respectively corresponding conductive pad region.

2. The semiconductor device of claim 1, wherein the first metal comprises tungsten (W), and wherein the at least one metal silicide layer comprises WSi, WSiN, WSiO, or a combination thereof.

3. The semiconductor device of claim 1 or claim 2, wherein the at least one metal silicide layer comprises a first metal silicide layer that contacts a first conductive pad region of the plurality of conductive pad regions, and wherein a lowermost surface of the first metal silicide layer is spaced apart from a lower surface of the first conductive pad region.

4. The semiconductor device of claim 1 or claim 2, wherein the at least one metal silicide layer comprises a first metal silicide layer that contacts a first conductive pad region of the plurality of conductive pad regions, and wherein the first metal silicide layer contacts an upper surface of the first conductive pad region.

5. The semiconductor device of claim 1 or claim 2, wherein the at least one metal silicide layer comprises a first metal silicide layer that contacts a lower surface of a first contact structure of the plurality of contact structures and a first conductive pad region of the plurality of conductive pad regions, and wherein a width of the first metal silicide layer is less than a width of the first contact structure in a horizontal direction, and a height of the first metal silicide layer is less than a height of the first conductive pad region in a vertical direction.

6. The semiconductor device of claim 1 or claim 2, wherein the at least one metal silicide layer comprises a first metal silicide layer that contacts a lower surface of a first contact structure of the plurality of contact structures and a first conductive pad region of the plurality of conductive pad regions, and wherein the first metal silicide layer is spaced apart from an upper surface and a lower surface of the first conductive pad region.

7. The semiconductor device of any one of claims 1 to 6, wherein the at least one metal silicide layer comprises a plurality of metal silicide layers between each conductive pad region of the plurality of conductive pad regions and a respectively corresponding contact structure of the plurality of contact structures.

8. The semiconductor device of any one of claims 1 to 6, wherein at least one conductive pad region of the plurality of conductive pad regions, is directly connected to a respectively corresponding contact structure without a metal silicide layer therebetween.

9. A semiconductor device comprising:

a substrate comprising a memory cell region and a connection region;

a gate stack comprising a first gate line integrally connected with a first conductive pad region and a second gate line integrally connected with a second conductive pad region, wherein the first gate line and the second gate line extend in a horizontal direction parallel with a main surface of the substrate in the memory cell region and the first conductive pad region and the second conductive pad region extend in the horizontal direction in the connection region, and wherein the first gate line, the first conductive pad region, the second gate line, and the second conductive pad region each comprise a first metal;

first and second contact structures extending in the connection region in a vertical direction, the first and second contact structures comprising a second metal; and

a first metal silicide layer between the first conductive pad region and the first contact structure and a second metal silicide layer between the second conductive pad region and the second contact structure, the first metal silicide layer contacting the first conductive pad region and the first contact structure and the second metal silicide layer contacting the second conductive pad region and the second contact structure,

wherein the first metal silicide layer has an uppermost surface equal to or lower than a vertical level of an uppermost surface of the first conductive pad region and a bottom surface that is above a lower surface of the first conductive pad region, and

wherein the second metal silicide layer has an uppermost surface equal to or lower than a vertical level of an uppermost surface of the second conductive pad region and a bottom surface that is above a lower surface of the second conductive pad region.

10. The semiconductor device of claim 9, wherein the first metal is the same as the second metal.

11. The semiconductor device of claim 9, wherein the first metal and the second metal are different from each other.

12. The semiconductor device of any one of claims 9 to 11, wherein the first metal silicide layer comprises at least one of nitrogen (N) and oxygen (O).

13. The semiconductor device of any one of claims 9 to 12, wherein a lowermost surface of the first metal silicide layer is spaced apart from a lower surface of the first conductive pad region.

14. The semiconductor device of any one of claims 9 to 13, wherein the gate stack comprises a plurality of gate lines in the memory cell region that overlap each other in the vertical direction, and a plurality of conductive pad regions in the connection region each integrally connected to a respective gate line of the plurality of gate lines, the plurality of conductive pad regions overlapping each other in the vertical direction,

wherein the first conductive pad region is one of the plurality of conductive pad regions, and

wherein a vertical distance from the first conductive pad region to the substrate is less than a vertical distance from an uppermost conductive pad region of the plurality of conductive pad regions to the substrate.

15. The semiconductor device of any one of claims 9 to 14, further comprising:

a periphery circuit region that faces the gate stack with the substrate therebetween and comprising a periphery circuit wiring layer comprising a third metal,

a periphery contact structure that penetrates the substrate to extend vertically to the periphery circuit wiring layer, and comprises a fourth metal, and

a periphery metal silicide layer between the periphery circuit wiring layer and the periphery contact structure that contacts the periphery circuit wiring layer and the periphery contact structure.

16. An electronic system comprising:

a main substrate;

a semiconductor device on the main substrate; and

a controller electrically connected to the semiconductor device on the main substrate,

wherein the semiconductor device comprises:

a substrate comprising a memory cell region and a connection region;

a plurality of gate lines vertically overlapping each other in the memory cell region, each gate line comprising a first metal;

a stepped connection unit in the connection region comprising a plurality of conductive pad regions, each conductive pad region integrally connected to a respective gate line of the plurality of gate lines and comprising the first metal;

a plurality of contact structures vertically overlapping the stepped connection unit, each contact structure connected to a respectively corresponding conductive pad region of the plurality of conductive pad regions and comprising a second metal; and

at least one metal silicide layer between each of the plurality of contact structures and the respectively corresponding conductive pad regions,

wherein an uppermost surface of each of the metal silicide layers is equal to or lower than an uppermost surface of the respectively corresponding conductive pad region and a bottom surface of each of the metal silicide layers is above a lower surface of the respectively corresponding conductive pad region.