A METHOD FOR MAKING HIGH-GAIN VERTICAL BIPOLAR JUNCTION TRANSISTOR STRUCTURES COMPATIBLE WITH CMOS PROCESS

ABSTRACT

An improved NPN bipolar transistor integratable with CMOS FET processing is achieved. The transistor is formed on a substrate using a CMOS process and one additional masking and implant step. The CMOS N wells are used to form the collector contacts (reachthrough) and the P wells are used to form the base. N doped third wells are formed under the N wells, P wells, and shallow trench isolation regions to provide subcollectors. Since the P wells are not implanted through the STI, basewidths are reduced and current gain is increased. Gate electrode masking elements, formed over the base, separate the emitter and base contact regions, improving the emitter-to-base breakdown voltage. The CMOS source/drain N type implants then form emitters in the emitter regions and ohmic contacts in the collector contacts. The source/drain P type implants form the ohmic base contacts to complete the bipolar transistor.

(Figure 7)