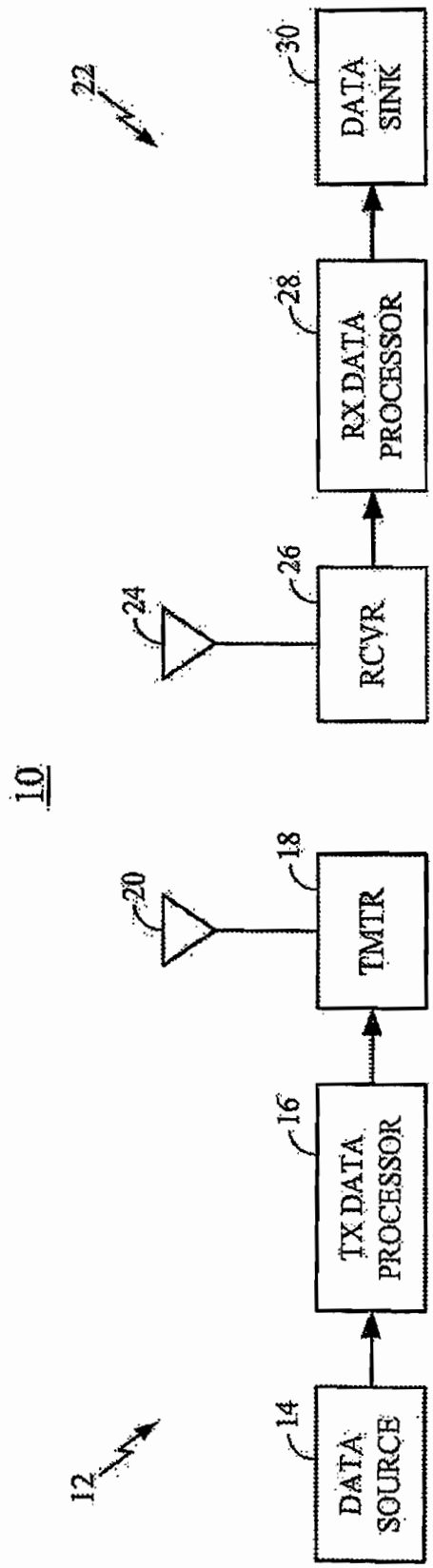

10
12
DATA SOURCE
14
TX DATA PROCESSOR
16
TMTR
18
20
22
RCVR
24
26
RX DATA PROCESSOR
28
DATA SINK
30

FIG. 1

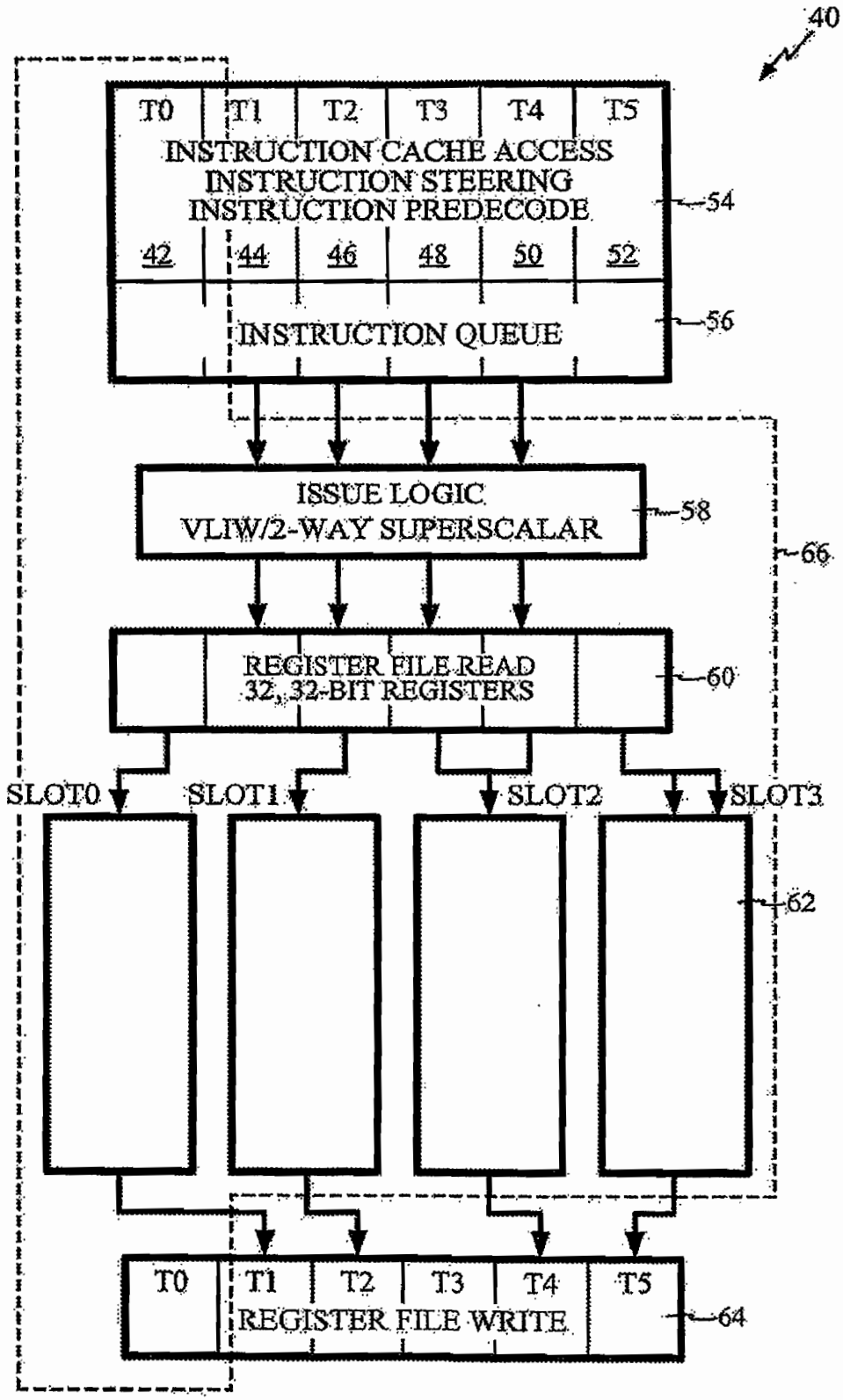

40
T0
T1
T2
T3
T4
T5
INSTRUCTION CACHE ACCESS
INSTRUCTION STEERING
INSTRUCTION PREDECODE
54
42
44
46
48
50
52
INSTRUCTION QUEUE
56
ISSUE LOGIC
VLIW/2-WAY SUPERSCALAR
58
66
REGISTER FILE READ
32, 32-BIT REGISTERS
60
SLOT0
SLOT1
SLOT2
SLOT3
62
T0
T1
T2
T3
T4
T5
REGISTER FILE WRITE
64

FIG. 2

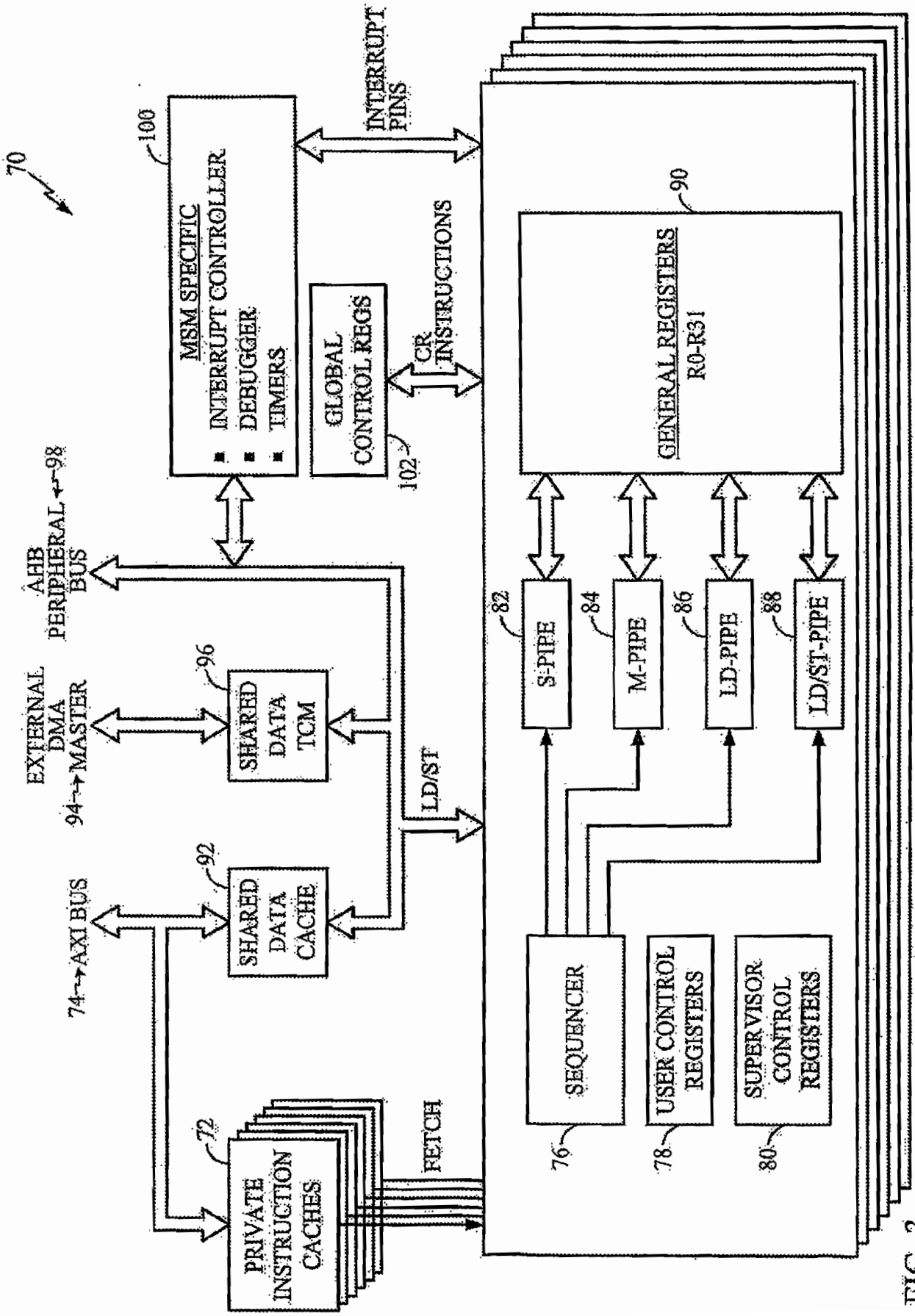

70
100
MSM SPECIFIC
INTERRUPT CONTROLLER
DEBUGGER
TIMERS
INTERRUPT PINS
GLOBAL CONTROL REGS
102
CR INSTRUCTIONS
90
GENERAL REGISTERS
R0-R31
AHB PERIPHERAL BUS
98
EXTERNAL DMA MASTER
94
96
SHARED DATA TCM
LD/ST
82
S-PIPE
84
M-PIPE
86
LD-PIPE
88
LD/ST-PIPE
74
AXI BUS
92
SHARED DATA CACHE
72
PRIVATE INSTRUCTION CACHES
FETCH
76
SEQUENCER
78
USER CONTROL REGISTERS
80
SUPERVISOR CONTROL REGISTERS

FIG. 3

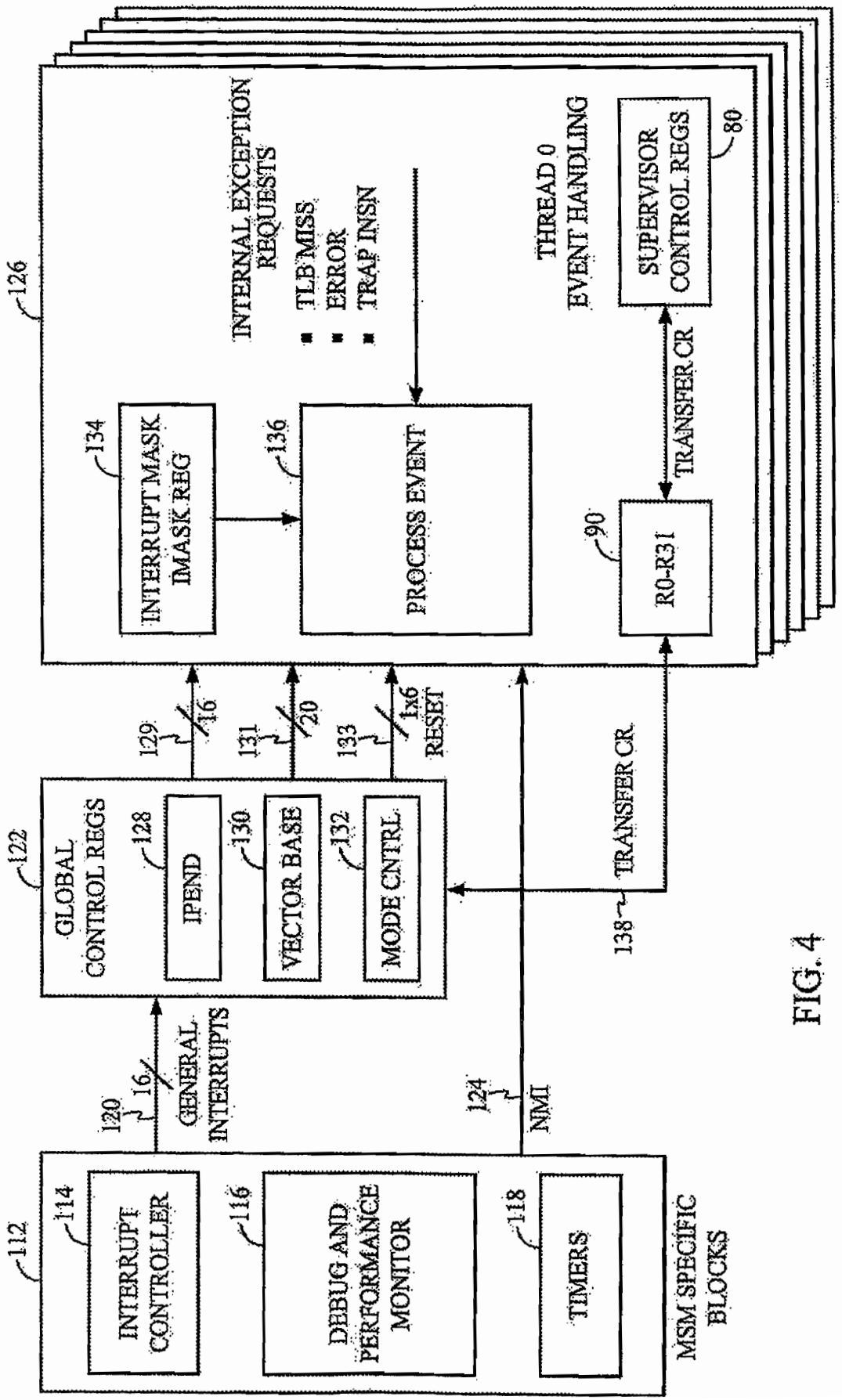

112
MSM SPECIFIC BLOCKS
114
INTERRUPT CONTROLLER
116
DEBUG AND PERFORMANCE MONITOR
118
TIMERS
120
16
GENERAL INTERRUPTS
124
NMI
122
GLOBAL CONTROL REGS
128
IPEND
130
VECTOR BASE
132
MODE CNTRL
129
16
131
20
133
1x6
RESET
TRANSFER CR
138
126
134
INTERRUPT MASK IMASK REG
136
PROCESS EVENT
INTERNAL EXCEPTION REQUESTS
TLB MISS
ERROR
TRAP INSN
THREAD 0 EVENT HANDLING
90
R0-R31
TRANSFER CR
SUPERVISOR CONTROL REGS
80

FIG. 4

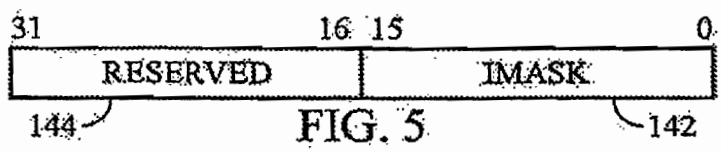


FIG. 5

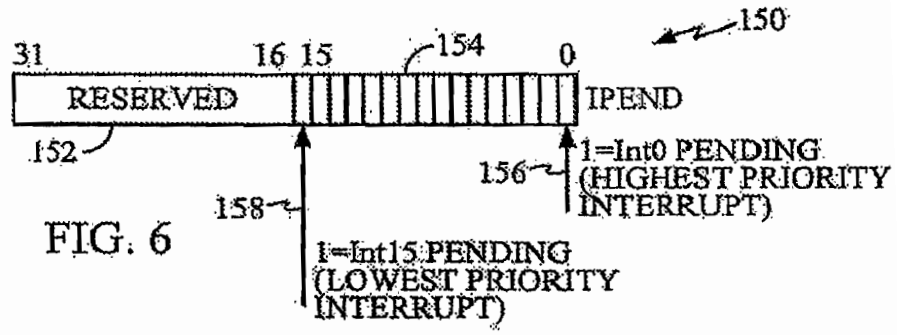


FIG. 6

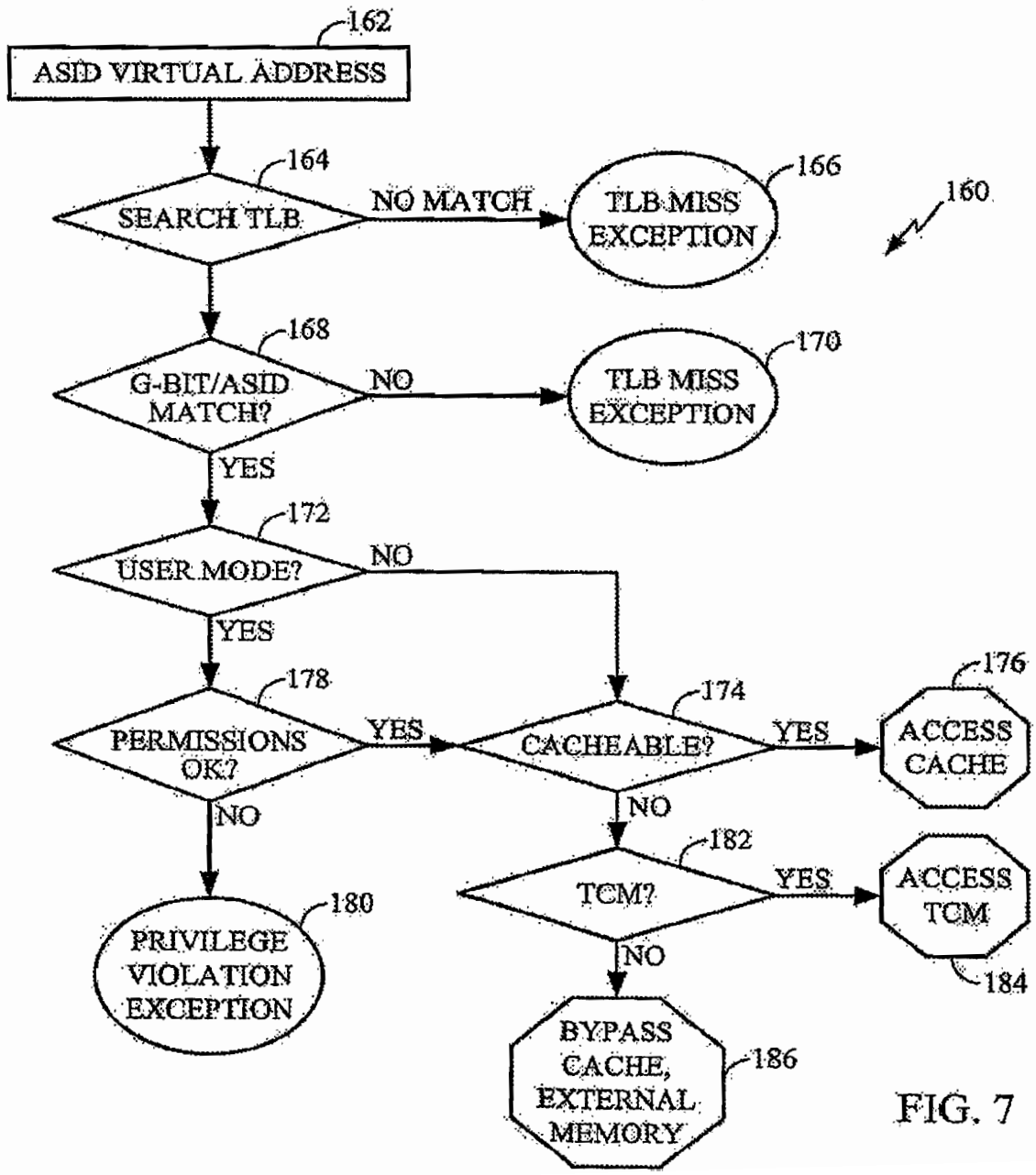


FIG. 7

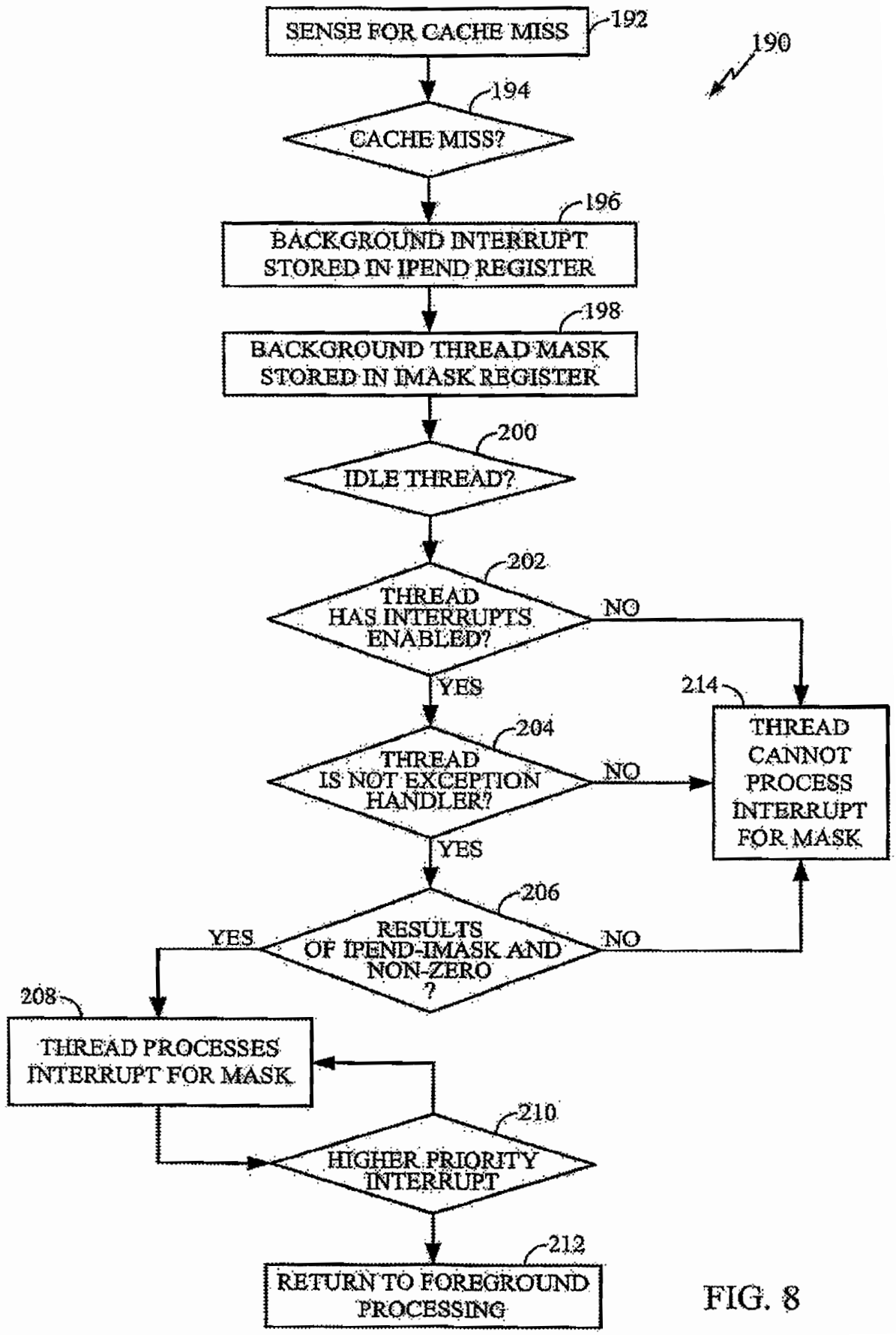

SENSE FOR CACHE MISS
192
190
194
CACHE MISS?
196
BACKGROUND INTERRUPT STORED IN IPEND REGISTER
198
BACKGROUND THREAD MASK STORED IN IMASK REGISTER
200
IDLE THREAD?
202
THREAD HAS INTERRUPTS ENABLED?
NO
YES
214
THREAD CANNOT PROCESS INTERRUPT FOR MASK
204
THREAD IS NOT EXCEPTION HANDLER?
NO
YES
206
RESULTS OF IPEND-IMASK AND NON-ZERO ?
YES
NO
208
THREAD PROCESSES INTERRUPT FOR MASK
210
HIGHER PRIORITY INTERRUPT
212
RETURN TO FOREGROUND PROCESSING

FIG. 8