

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) MIXER CIRCUIT

(71) We, RCA CORPORATION, formerly Radio Corporation of America, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to mixer circuits and more particularly to transistor mixer circuits for heterodyne receiver systems.

In the past, because of the parasitic feedback capacity between the output electrode and the input electrode of transistor mixer circuits, it has been necessary to provide a neutralization capacitor. Typically, the neutralization capacitor is connected between an inductor in the mixer tank circuit and the transistor input electrode. This feedback neutralizes the parasitic feedback of intermediate frequency (IF) signal components from the transistor output circuit back to the transistor input circuit. Because of the expense of the neutralization capacitor and the additional factory operation of adjusting the neutralization capacitor, it is desirable that transistor mixers operate in a satisfactory manner without the necessity of neutralization.

Another major problem of tuner fabrication has been the interaction of the tuner stage of a receiver with the IF signal processing circuitry of the receiver. Because of the interaction, alignment of the receiver must be accomplished with the tuner connected. Consequently, should the tuner be removed for servicing, realignment of the receiver is required. Moreover, the interaction of the tuner and the IF signal processing circuitry prevents a modular approach to receiver fabrication. This is, an approach wherein modules, such as a tuner, are separately fabricated and suitable for use with any other modular component.

A mixer circuit embodying the present invention is adapted for utilization in a hetero-

dyne receiver system in which radio frequency (RF) signals are converted to IF signals by mixing the RF signals and a locally generated signal. It comprises the combination of a module containing a first transistor connected in common emitter configuration followed by a module containing a second transistor in common base configuration, an interconnecting cable of characteristic impedance, so the output of the common emitter configuration provides the input signal to the common base configuration. The RF signals and locally generated signal are applied as contemporaneous inputs to the common emitter configuration and a tuned circuit is provided for deriving resultant IF signals from the output of the common base configuration.

The invention, both as to the organization of mixer circuits embodying it and as to their manner of operation, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

Figure 1 is a schematic circuit diagram of a transistor mixer circuit suitable for embodying the invention;

Figure 2 is a schematic circuit diagram of the transistor mixer shown in Figure 1 with a feedback capacitor utilized to minimize spurious responses and also suitable for embodying the invention;

Figure 3 is a graph illustrating certain features of the spurious response attenuation characteristics of the transistor mixer circuit of Figure 1;

Figure 4 is a schematic circuit diagram of a transistor mixer which permits separate alignment of a radio receiver tuner and the succeeding IF signal processing circuitry in accordance with the invention; and

Figures 5 and 6 are schematic circuit diagrams illustrating modifications of the transistor mixer circuit of the invention shown in Figure 4 to permit coupling between the transistors of the mixer with an arbitrary length of cable.

Referring now to the drawings, wherein like

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reference numerals designate similar elements in the various figures, and more particularly to Figure 1, a radio receiver tuner 12 includes a local oscillator stage 14, an RF amplifier stage 16 and a mixer stage 18. RF signals are coupled from the amplifier stage 16 via a capacitor 20 to the mixer stage 18, and locally generated signals from the oscillator stage 14 are coupled to the mixer stage 18 via a capacitor 22. The RF signal and the oscillator signal are heterodyned in the mixer stage 18 to produce an IF signal which may be processed by IF signal processing circuits of a radio receiver, not shown.

15 The mixer 18 includes

The mixer stage 18 includes two transistors 24 and 26. The transistor 24 is interconnected by circuit components in a common emitter configuration, and the transistor 26 is interconnected by the circuit components in the common base configuration. Specifically, the emitter electrode of the transistor 24 is connected to ground by a resistor 28 and a feedthrough capacitor 30, the feedthrough capacitor providing signal frequency ground for the emitter electrode. The base of the transistor 26 is connected to ground for signal frequencies by the feedthrough capacitor 32. The base electrode of the transistor 26 is also connected to the junction of the bias resistors 34 and 36 which are serially connected with a resistor 38 between a source of operating potential applied at terminal 40 and the ground. A feedthrough capacitor 39 prevents any RF or IF signal from affecting the source of operating potential. The serially connected resistors provide the necessary bias potential for the transistors, and thus, the base electrode of the transistor 24 is connected to the junction of the resistors 34 and 38. To complete the bias for the mixer stage 18, a choke 42 and a serially connected variable inductor 44 interconnect the source of operating potential at the terminal 40 and the collector electrode of the transistor 26.

Input signals to the mixer 18, the RF signal and the local oscillator signal are applied at the junction of the base electrode of the transistor 24 and the impedance matching feed-through capacitor 46, where they are heterodyned in the transistor to produce an IF signal. The IF signal appears at the collector electrode of the transistor 24 which is directly connected to the emitter electrode of the transistor 26, a low impedance point. This insures that there will be a minimum of effect of the feedback capacitance between the collector electrode of the transistor 24 and its input circuit.

60 As capacitance feedback is proportional to the rate of change in voltage between two points with respect to time, that is, $\frac{dv}{dt}$, and moreover, since the collector electrode of the

transistor 24 is connected to a low impedance point where only a small signal voltage can be

developed, the time variation ($\frac{dv}{dt}$) of the volt-

age at the collector electrode for a given frequency with respect to the base electrode is correspondingly small, hence, only a small parasitic feedback voltage exists between the collector and base electrodes of the transistor 24. Consequently, no neutralization capacitor is needed to counter the effects of the parasitic feedback capacitance. Should it be desired, the connection between the collector electrode of the transistor 24 and the emitter electrode of the transistor 26 can be supported by a stand-off terminal, not shown. This terminal provides mechanical support with a very small capacitance and can be used as an alignment point for a radio receiver.

The IF signals appearing at the collector electrode of the transistor 24 are amplified by the transistor 26 to provide an IF signal across a resonant circuit connected to its collector electrode. The resonant circuit includes the variable inductor 44 and capacitors 48 and 50, the components being proportioned for resonance at the frequency of the IF signal. IF signals may sometimes result from heterodyne processing by the radio receiver.

Distortion of reproduced video and sound signals may sometimes result from heterodyning of harmonics and various combinations of the sound and picture carriers with the locally generated signal. For instance with the current U.S. Federal Communications Commission's assignment of television frequencies for the various channels, such distortion often occurs in FCC channel 6 reception. At this channel there are two particularly difficult spurious responses formed as follows: (1) channel 6 picture carrier (83.25 MHz) + channel 6 sound carrier (87.75 MHz) — local oscillator frequency for channel 6 (129 MHz) = 42 MHz; (2) 2 × sound carrier for channel 6 (87.75 MHz) — local oscillator for channel 6 (129 MHz) = 46.5 MHz. As the IF bandpass for television receivers ranges from 41 to 47 MHz, the channel 6 spurious responses of 42 MHz, which is within 170 KHz of the color subcarrier, and 46.5 MHz are particularly troublesome.

An improvement in the beat rejection of the mixer circuit can be achieved by the employment of a small feedback capacitor. This may be particularly desirable for improved beat rejection of spurious responses such as those at FCC channel 6. Thus in Figure 2, a small fixed value feedback capacitor 54 is coupled between the collector electrode of the transistor 26 and the base electrode of the transistor 24. The capacitor 54 may improve the beat rejection because of secondary mixing occurring in the transistor 26 as the result of the basic carrier and oscillator signals which

are amplified in the transistor 24, or may aid in the cancellation or reduction of higher order nonlinearities in the mixer circuit.

It has been found that the spurious response rejection capability of the mixer circuit can be optimized by careful selection of the bias resistors. Figure 3 illustrates the attenuation of the 42 and 46.5 MHz beats as a function of the resistance of bias resistor 34 for the component values shown in the various figures. The particular value of resistance for optimum performance depends, in part, upon the mixer circuit transistor parameters.

Reference is now made to Figure 4 which is a schematic circuit diagram of a transistor mixer having the advantage given by the invention of permitting separate alignment of a radio receiver tuner and the succeeding IF signal processing circuitry. Because the emitter electrode of the transistor 26 is a low impedance point, there is little interaction between the local oscillator stage 14, and the RF amplifier stage 16, and the transistor 24 with its associated circuitry as one unit and the transistor 26 with its associated circuitry and the succeeding IF signal processing circuitry, not shown, as the second unit. Consequently, it is feasible to break the direct connection, shown in Figure 1, between the collector electrode of the transistor 24 and the emitter electrode of the transistor 26. This gives important advantages.

The mixer circuit may therefore be divided into two parts in separate modules; the common emitter section remaining on the tuner chassis and the common base section being put with the IF signal processing circuitry. The interconnection between these two halves may be facilitated by means of an appropriate connector such as a plug 56 and jack 58. In a like manner, the break in the mixer bias circuitry which is required may be facilitated by means of another plug 60 and jack 62.

The breaking of the mixer circuit 18 into two parts allows a separate and independent alignment of the tuner at RF frequencies and the succeeding IF signal processing circuitry at IF frequencies. Because there is a minimal interaction between the two parts, servicing and factory replacement is facilitated due to the interchangeability of parts without realignment of the entire receiver.

To further implement the modular approach to television receiver fabrication, the split mixer stage 18 can be modified to permit coupling between the two units by means of an arbitrary length of coaxial cable. Referring now to Figure 5, the mixer circuit 18 is broken into two units 64 and 66. The units are interconnected by a coaxial cable 68.

To provide proper impedance matching between the collector electrode of the transistor 24 and the coaxial cable 68, a load resistor 70, which approximates the characteristic impedance of the cable, is connected in series with

a DC blocking capacitor 72 between the collector electrode of the transistor 24 and the ground. The collector electrode of the transistor 24 may be coupled to the coaxial cable 68 by a jack 74 and a plug 76. In a like manner, to complete the mixer bias circuitry, the resistor 34 may be coupled to the base electrode of the transistor 26 by a jack 78 and plug 80. It should be noted that the coaxial cable 68 is not terminated with its characteristic impedance at the emitter electrode of the transistor 26. This is because the emitter electrode of the transistor 26 is a low impedance point and the mismatch is needed, for reasons previously described, to insure that the parasitic feedback capacitance is small.

The split mixer circuit can also be arranged for a parallel bias of the two units 64 and 66 as shown in Figure 6. Again, to provide proper impedance matching between the collector electrode of the transistor 24 and the coaxial cable 68, a load resistor 70, which approximates the characteristic impedance of the cable, is connected between the collector electrode of the transistor 24 and a source of operating potential applied at the terminal 82. The collector electrode of the transistor 24 is coupled to a jack 84 by a DC blocking capacitor 86. The capacitor 86 prevents DC interaction between the units 64 and 66.

The DC bias for the mixer circuit is a parallel connection. This is, the transistor 24 is biased from a source of operating potential applied to the terminal 82 and coupled to the collector electrode by the resistor 70 and to the base electrode by the serially connected resistors 88 and 90. The DC bias for the transistor 26 is obtained from the source of operating potential applied to the terminal 40. This potential is applied to the collector electrode of the transistor by the serially connected choke 42 and variable inductor 44 and to the base electrode of the transistor by the serially connected resistors 92 and 94. The resistor 96 coupled between the emitter electrode of the transistor 26 and the ground provides the necessary DC emitter return for the grounded base portion and can also be used for loading, if desired.

The feedback capacitor 54 of Fig. 2 will, if used, require a separate lead between the modules of Figs. 4, 5 and 6.

WHAT WE CLAIM IS:—

1. A mixer circuit for a heterodyne radio receiver, comprising the combination of a first transistor connected in common emitter configuration having its output electrode interconnected with the input electrode of a second transistor in common base configuration, a tuned circuit for deriving intermediate frequency signals from the output electrode of the common base configuration when radio signals and a locally generated signal are applied as contemporaneously to the input electrode of the



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are amplified in the transistor 24, or may aid in the cancellation or reduction of higher order nonlinearities in the mixer circuit.

It has been found that the spurious response rejection capability of the mixer circuit can be optimized by careful selection of the bias resistors. Figure 3 illustrates the attenuation of the 42 and 46.5 MHz beats as a function of the resistance of bias resistor 34 for the component values shown in the various figures. The particular value of resistance for optimum performance depends, in part, upon the mixer circuit transistor parameters.

Reference is now made to Figure 4 which is a schematic circuit diagram of a transistor mixer having the advantage given by the invention of permitting separate alignment of a radio receiver tuner and the succeeding IF signal processing circuitry. Because the emitter electrode of the transistor 26 is a low impedance point, there is little interaction between the local oscillator stage 14, and the RF amplifier stage 16, and the transistor 24 with its associated circuitry as one unit and the transistor 26 with its associated circuitry and the succeeding IF signal processing circuitry, not shown, as the second unit. Consequently, it is feasible to break the direct connection, shown in Figure 1, between the collector electrode of the transistor 24 and the emitter electrode of the transistor 26. This gives important advantages.

The mixer circuit may therefore be divided into two parts in separate modules; the common emitter section remaining on the tuner chassis and the common base section being put with the IF signal processing circuitry. The interconnection between these two halves may be facilitated by means of an appropriate connector such as a plug 56 and jack 58. In a like manner, the break in the mixer bias circuitry which is required may be facilitated by means of another plug 60 and jack 62.

The breaking of the mixer circuit 18 into two parts allows a separate and independent alignment of the tuner at RF frequencies and the succeeding IF signal processing circuitry at IF frequencies. Because there is a minimal interaction between the two parts, servicing and factory replacement is facilitated due to the interchangeability of parts without realignment of the entire receiver.

To further implement the modular approach to television receiver fabrication, the split mixer stage 18 can be modified to permit coupling between the two units by means of an arbitrary length of coaxial cable. Referring now to Figure 5, the mixer circuit 18 is broken into two units 64 and 66. The units are interconnected by a coaxial cable 68.

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a DC blocking capacitor 72 between the collector electrode of the transistor 24 and the ground. The collector electrode of the transistor 24 may be coupled to the coaxial cable 68 by a jack 74 and a plug 76. In a like manner, to complete the mixer bias circuitry, the resistor 34 may be coupled to the base electrode of the transistor 26 by a jack 78 and plug 80. It should be noted that the coaxial cable 68 is not terminated with its characteristic impedance at the emitter electrode of the transistor 26. This is because the emitter electrode of the transistor 26 is a low impedance point and the mismatch is needed, for reasons previously described, to insure that the parasitic feedback capacitance is small.

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The DC bias for the mixer circuit is a parallel connection. This is, the transistor 24 is biased from a source of operating potential applied to the terminal 82 and coupled to the collector electrode by the resistor 70 and to the base electrode by the serially connected resistors 88 and 90. The DC bias for the transistor 26 is obtained from the source of operating potential applied to the terminal 40. This potential is applied to the collector electrode of the transistor by the serially connected choke 42 and variable inductor 44 and to the base electrode of the transistor by the serially connected resistors 92 and 94. The resistor 96 coupled between the emitter electrode of the transistor 26 and the ground provides the necessary DC emitter return for the grounded base portion and can also be used for loading, if desired.

The feedback capacitor 54 of Fig. 2 will, if used, require a separate lead between the modules of Figs. 4, 5 and 6.

WHAT WE CLAIM IS:—

1. A mixer circuit for a heterodyne radio receiver, comprising the combination of a first transistor connected in common emitter configuration having its output electrode interconnected with the input electrode of a second transistor in common base configuration, a tuned circuit for deriving intermediate frequency signals from the output electrode of the common base configuration when radio signals and a locally generated signal are applied as contemporaneously to the input electrode of the

- common emitter configuration, wherein the two configurations are included in separate modules and are interconnected by a signal conducting cable having a characteristic impedance and extending between said modules.
- 5 2. A mixer circuit as claimed in Claim 1 wherein said cable includes a coaxial cable length.
 - 10 3. A mixer circuit as claimed in Claim 2 wherein the module including the first transistor includes means terminating the coaxial cable length at said module with an impedance approximating its characteristic impedance.
 - 15 4. A mixer circuit as claimed in Claim 1, Claim 2 or Claim 3 wherein said cable includes a separable coupling.
 - 20 5. A mixer circuit as claimed in Claim 4 wherein said modules are also interconnected by a connection means including a further separable coupling for the interconnection of biasing circuitry provided in the two modules for said transistors therein.
 6. A mixer circuit as claimed in any one of Claims 1 to 5 wherein the module includ-

ing the first transistor includes also a radio frequency amplifier and a local oscillator both having their outputs coupled to the input electrode of the common base configuration.

7. A mixer circuit as claimed in any one of Claims 1 to 6 wherein the module including the second transistor includes also intermediate frequency processing circuitry.

8. A mixer circuit as claimed in any preceding claim having a feedback capacitor connected between the output of the common base configuration and the input to the common emitter configuration for improved beat rejection.

9. A mixer circuit substantially as hereinbefore described with reference to any one of Figures 5 and 6 of the accompanying drawings.

10. A heterodyne receiver having a mixer circuit as claimed in any preceding claim.

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