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SYNCHRONIZING/DRIVING CIRCUIT FOR A
FORWARD SYNCHRONOUS RECTIFIER

BACKGROUND OF THE INVENTION

1. Field of the Invention

10 The present invention relates to a
synchronizing and driving circuit for a forward converter
employing a synchronous rectifier.

2. Related Art

15 In known forward switching power supply
circuits employing synchronous rectifiers, the secondary
side diodes are replaced by transistors to obtain a lower
on-state voltage drop. The transistors must be biased to
conduct from source to drain (for an N-channel power
20 MOSFET) when a diode would have been conducting from
anode to cathode, and conversely, must be gated to block
voltage from drain to source when a diode would have been
blocking from cathode to anode.

 In these known synchronous rectifier circuits,
the gate signals to the transistors must be synchronized
25 as close as possible to the inflection points of the
output inductor current, which inflection points
correspond to the zero crossings of the squarewave output

inductor voltage. The gate signals can be "self-driven" (i.e., the gate signal is tied directly to the circuit) or "controlled synchronized" (i.e., a synchronizing signal is derived from some point in the circuit and fed to a MOSFET gate driver).

Examples of prior art synchronous rectifiers may be found in U.S. Patent Nos. 4,903,189 to Ngo, et al.; 5,430,640 to Lee; and 5,457,624 to Hastings; and in the following articles: "Synchronous Rectifiers Improve Efficiency in Low Output Voltage Forward Converters" by Clemente, et al. (pp. 347-350) and "The Impact of Low Output Voltage Requirements on Power Converters" by Jitaru, HFPC, May 1995 Proceedings (pp. 1-10).

Some synchronous rectifier circuits of the prior art monitor the primary side control signals and transfer such signals to the secondary side of the power converter (i.e., across the isolation boundary) in order to synchronize the gating of the synchronous transistors. Unfortunately, costly, non-optimal and complex circuitry is required to maintain isolation between primary and secondary portions of the circuit. For example, when opto-isolators are used to maintain isolation, undesirable delays and unpredictable gain variations introduce errors in the system.

Other synchronous rectifier circuits of the prior art use additional transformer windings to transfer synchronizing information to the secondary circuit transistors and still maintain isolation. However, such transformers are more costly and complex and a transformer reset problem also arises.

Accordingly, there is a need in the art for a new synchronous rectifier circuit which does not require opto-couplers or additional transformer windings to

transfer synchronizing information across the isolation boundary between primary and secondary circuits in a forward power converter.

SUMMARY OF THE INVENTION

5 In order to overcome the disadvantages of the prior art synchronous rectifier circuits, the present invention provides "self-driven" gate signals produced by monitoring the voltage across the output inductor of the converter and alternately gating the transistors in
10 response to transitions of the inductor voltage such that one transistor is always on when the other is off, and vice versa.

 Other features and advantages of the present invention will become apparent from the following
15 description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

 For the purpose of illustrating the invention, there is shown in the drawings forms which are presently
20 preferred, it being understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown.

 Figure 1 is a circuit diagram partially in block form of a synchronous rectifier in accordance with
25 the invention.

 Figure 2 is an equivalent circuit of a secondary circuit of Figure 1 during a first mode of operation.

 Figure 3 is an equivalent circuit of the
30 secondary circuit of Figure 1 in a second mode of operation.



Figure 4 illustrates waveforms at various points during operation of in the circuit of Figure 1.

Figure 5 shows the circuit of Figure 1 with a comparator shown in the block diagram in Figure 1 shown in detail in Figure 5.

Figure 6 shows an alternative embodiment of the comparator of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings wherein like numerals indicate like elements, there is shown in Fig. 1 a synchronous rectifier 10 in accordance with the invention which includes a primary circuit 20 and a secondary circuit 30. The primary circuit 20 includes a voltage source V_m , a primary winding 11 of a transformer 12, a switch S_p , a reset winding 13 for resetting the core of the transformer 12 and a reset diode D_r . The switch S_p , for simplicity, is shown as a single pole, single-throw switch; in actuality, however, the switch may be a conventional MOS-gated semiconductor switch, such as power MOSFET or insulated gate bipolar transistor (IGBT).

The secondary circuit 30 includes a secondary winding 14, an output inductor L , and output capacitor C , a first power transistor S_1 , and a second power transistor S_2 . Each power transistor S_1 , S_2 includes an anti-parallel diode thereacross.

A comparator 40 is connected across the output conductor L for sensing the voltage thereacross, V_L , that is, for sensing the difference in potential between the voltages V_A and V_{out} . The comparator 40 has an output connected to the gate of the transistor S_1 and an

inverted output connected to the gate of the transistor S_2 .

When the voltage V_L across the inductor L is positive, the transistor S_1 is biased on and the transistor S_2 is biased off. Conversely, when the voltage V_L is negative, the transistor S_2 is biased on and the transistor S_1 is biased off.

Thus, the rectifier 10 has two modes of operation. In the first mode, Mode 1, the transistor S_1 is on and conducting current and the transistor S_2 is off and blocking current. In the second mode, Mode 2, the transistor S_1 is off and blocking current and the transistor S_2 is on and conducting current.

A better understanding of Mode 1 may be had by referring to the equivalent circuit of Figure 2 in which V_s represents the voltage across the secondary winding 14, transistor S_1 is represented by an ideal diode S_1 , and the output voltage is represented by an output voltage source V_o . The relationship between the various voltages is as follows: $V_s = V_L + V_o$, and $V_L = V_s - V_o$. Since V_s is greater than V_o , V_L is thus positive.

Also, I_L in Mode 1 is ramping up or increasing.

Accordingly, $\frac{di}{dt}$ is positive. Since $V_L = L \frac{di}{dt}$, this analysis also shows that V_L is positive in Mode 1.

Mode 2, in which the transistor S_1 is blocking current and the transistor S_2 is conducting current, may be represented by the equivalent circuit shown in Figure 3, where the transistor S_2 is represented by the ideal diode S_2 . As in the equivalent circuit for Mode 1, $V_s = V_L + V_{out}$ and, therefore, $V_L = V_s - V_{out}$. Here, V_A is zero volts which is less than V_{out} and, therefore, V_L is

negative. Also, in Mode 2, I_L is decreasing or ramping down. Accordingly, $\frac{di}{dt}$ is negative. Since

$V_L = L \frac{di}{dt}$, this analysis also indicates that V_L is negative in Mode 2.

5 Waveforms occurring at different points in the circuit of Figure 1 during operation are shown in Figure 4.

Turning now to Figure 5, there is shown a detailed implementation of the comparator 40 of Figure 1 which includes a non-inverting transistor comparator Q_1 and associated (push-pull) driver transistors Q_3 and Q_4 , and an inverting transistor comparator Q_2 and associated (push-pull) driver transistors Q_5 and Q_6 . The transistors Q_1 and Q_2 respond to the voltage V_{sense} with respect to ground, where V_{sense} changes as a function of V_L and V_A .

15 In Mode 1, V_A is greater than V_{out} (i.e., $V_A = V_{in} \cdot (N_s/N_p)$) and, therefore, V_{sense} is a positive voltage approximately equal to $V_{out} + V_{fd1}$, where V_{fd1} is the forward voltage drop across the diode D_1 . This results in the transistor Q_1 being biased on and Q_2 being biased off. The output from the emitter of Q_1 is therefore a positive voltage which causes Q_3 to turn on and Q_4 to turn off. Accordingly, the voltage at the gate of S_1 rises to about V_{ZZ} and S_1 turns on. Conversely, the output from the collector of Q_2 is about zero volts which causes Q_6 to turn on and sweep the charge off the gate of S_2 and turn it off.

25 In Mode 2, V_A is less than V_{out} (i.e., $V_A \approx 0$ volts) and, therefore, $V_{sense} = V_A \approx 0$ volts. This results in transistor Q_1 being biased off and Q_2 being biased on.

The output from the collector of Q_2 is therefore a positive voltage which causes Q_3 to turn on and Q_6 to turn off. Accordingly, the voltage at the gate of S_2 rises to about V_{ZZ} and S_2 turns on. Conversely, the output from
5 the emitter of Q_1 is about zero volts which causes Q_4 to turn on and sweep the charge off the gate of S_1 and turn it off.

Thus, the gating of S_1 and S_2 is a function of the voltage V_L across the inductor L , that is, when V_L is
10 positive, S_1 is biased on (the gate of S_1 is positive with respect to its source) and S_2 is biased off (the gate of S_2 is low with respect to its source). When V_L is negative, on the other hand, S_1 is biased off and S_2 is biased on.

Advantageously, the gate of the transistors are
15 "self driven" by sensing conditions in the secondary circuit 30, namely the inductor voltage, V_L . Thus, there is no need for expensive, unpredictable and slow opto-isolators or additional windings in the transformer 12.
20 Further, the efficient utilization of discrete components obviates the need for expensive integrated circuit type comparators.

It is noted that diode D_1 advantageously limits the voltage at V_{senc} to one diode drop above V_{out} which also
25 limits the voltage input to Q_1 and Q_2 . Thus, the circuit is immune to back oscillation at peak values of V_A because such peak values are not fed back in the circuit of the present invention. Further, by limiting maximum excursions of V_{senc} to about V_{out} , the transistors are off
30 when V_{out} is under voltage (i.e. when V_{out} is less than 1) thereby providing for enhanced start up characteristics of the converter.

It is noted that D_1 allows an extra diode drop of driving voltage for driving Q_1 - Q_6 (i.e., $V_{\text{sense}} = V_{\text{out}} + V_{D1}$). Nonetheless, if V_{out} is designed to be a very low output which would not allow proper drive voltage to Q_1 - Q_6 , then the cathode of diode D_1 may be connected to V_{ZZ} . Thus, a higher voltage would be obtained to drive Q_1 - Q_6 (i.e., $V_{\text{sense}} = V_{ZZ} + V_{D1}$).

Capacitors C_1 and C_2 are used to introduce respective time delays into the circuits of Q_1 and Q_2 in order to provide a requisite deadtime.

The reason for deadtime is as follows: The synchronous rectifier gate signals needs to be synchronized as closely as possible to the transitions in V_L (i.e., the zero crossing points). If the respective gates are on too long (i.e., turned on early, turned off late), current overshoot or oscillation due to cross conducting between S_1 and S_2 can occur. If the respective gates are turned on too late or turned off too early, the anti-parallel diode of the power MOSFETs will conduct giving higher conduction losses while it conducts and reverse recovery effects when turned off as the voltage swings to the opposite polarity.

Thus, to avoid cross-conduction, when V_A is greater than V_{out} , the transistor S_1 turns on after a deadtime and the transistor S_2 turns off. Conversely, when V_A is less than V_{out} , the transistor S_1 turns off and the transistor S_2 turns on after a deadtime. Advantageously, the amount of deadtime can be predetermined to allow for designs having different types of power MOSFETs.

The resistor R_3 , capacitor C_3 and diode D_2 serve as a driving power source or auxiliary source of DC

power. Alternatively, V_{out} can be used as V_{ZZ} if V_{out} is high enough to provide sufficient drive voltage to the gates of S_1 and S_2 to reduce the forward resistance thereof (i.e., to fully enhance the transistors S_1 and S_2).

R_3 serves as a bleeding resistor to charge C_3 . C_3 provides the current to the circuit and maintains V_{ZZ} according to the breakdown voltage V_{D2} of the zener diode D_2 . If V_A is greater than V_{D2} then V_{ZZ} is approximately equal to the breakdown voltage of the zener diode D_2 . On the other hand, if V_A is less than V_{D2} , then V_{ZZ} is approximately equal to the peak value of V_A .

Advantageously, the V_{ZZ} supply permits driving the power MOSFETs with high enough voltage to fully enhance the devices and lower their forward resistances. This mitigates the need for an extra winding on the transformer or an extra power supply.

Figure 6 shows an alternative embodiment 40' of the comparator 40 of Figure 5. In the embodiment of Figure 6, FET transistors Q_7 - Q_{11} are used in place of the bipolar transistors Q_1 - Q_6 of Figure 5. Operation of this embodiment is essentially the same as the embodiment of Figure 5. More specifically, when V_A is greater than V_{out} , a high voltage is inputted to the gate of S_1 and a low voltage is inputted to the gate of S_2 . Conversely, when V_A is less than V_{out} , a low voltage is applied to the gate of S_1 and a high voltage is applied to the gate of S_2 .

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is

preferred, therefore, that the present invention not be limited by the specific disclosure herein.



WHAT IS CLAIMED IS:

1. An isolated forward switching power converter, comprising:

a primary side circuit coupled to a primary winding of an isolation transformer; and

5 a secondary side circuit coupled to a secondary winding of the isolation transformer, the secondary side circuit including:

an output inductor coupled in series with the secondary winding at a first node and coupled at a second
10 node to an output capacitor across which an output voltage is taken;

a first MOS gated transistor coupled in series with the secondary winding and the output inductor;

15 a second MOS gated transistor coupled in shunt from the first node to ground; and

a synchronous rectifier control circuit coupled to the first and second MOS gated transistors, the synchronous rectifier circuit sensing the voltage across the output inductor and alternately biasing the first and
20 second transistors on and off in response thereto.

2. The isolated forward switching power converter of claim 1, wherein the peak value of the sensed inductor voltage is limited to the output voltage.

3. The isolated forward switching power converter of claim 2, wherein one terminal of a resistor is coupled to the first node, the cathode of a diode is coupled to the second node, the anode of the diode is
5 coupled to the other terminal of the resistor at a third





node and the sensed inductor voltage is obtained from the third node.

4. The isolated forward switching power converter of claim 1, wherein the secondary circuit further comprises an auxiliary source of DC voltage, the auxiliary source of DC voltage being taken across a zener diode, the zener diode coupled to the first node through a blocking diode and current limiting resistor.

5. The isolated forward switching power converter of claim 4, wherein the peak value of the sensed inductor voltage is limited to the auxiliary source of DC voltage.

6. The isolated forward switching power converter of claim 5, wherein one terminal of a resistor is coupled to the first node, the cathode of a diode is coupled to the auxiliary source of DC voltage, the anode of the diode is coupled to the other terminal of the resistor at a third node and the sensed inductor voltage is obtained from the third node.

7. The isolated forward switching power converter of claim 1, wherein the sensed voltage is coupled to a non-inverting sense circuit and an inverting sense circuit.

8. The isolated forward switching power converter of claim 7, wherein the non-inverting sense circuit includes a non-inverting amplifier coupled to a first drive circuit;





5 the first drive circuit is coupled to the gate
of the first transistor;

 the inverting sense circuit includes an
inverting amplifier coupled to a second drive circuit;
and

 the second drive circuit is coupled to the gate
of the second transistor.

9. The isolated forward switching power
converter of claim 8, wherein

 the non-inverting amplifier includes a bipolar
transistor connected in an emitter follower
configuration;

5 the first drive circuit includes a bipolar
push-pull transistor pair;

 the inverting amplifier includes a bipolar
transistor; and

 the second drive circuit includes a bipolar
push-pull transistor pair.

10. The isolated forward switching power
converter of claim 8, wherein

 the non-inverting amplifier includes a MOS
gated transistor;

5 the first drive circuit includes a MOS gated
push-pull transistor pair;

 the inverting amplifier includes a MOS gated
transistor; and

 the second drive circuit includes a MOS gated
push-pull transistor pair.