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(54) Title: DYNAMIC DEFERRED TRANSACTION MECHANISM

(57) Abstract

A method and apparatus for regulating the deferral of a transaction issued on a bus by a processor in a computer system is disclosed. A bus transaction recorder coupled to the bus processes encoded signals from the transaction issued on the bus. A line coupled to the bus sends an indication signal when a pending transaction request is issued on the bus. A CPU latency timer times the current transaction on the bus when a new pending transaction is waiting on the bus. The CPU latency timer outputs an expiration signal when the transaction takes more than a predetermined amount of time to complete. A transaction processor unit is coupled to the bus transaction recorder, the line, and the CPU latency timer. The transaction processor unit defers the transactions issued on the bus when the transaction processor receives the indication signal indicating that a pending transaction is waiting to be issued on the bus, when the encoded signals from the transaction issued on the bus indicate that the transaction issued on the bus is a candidate for deferral, and when the CPU latency timer outputs the expiration signal.

