

100

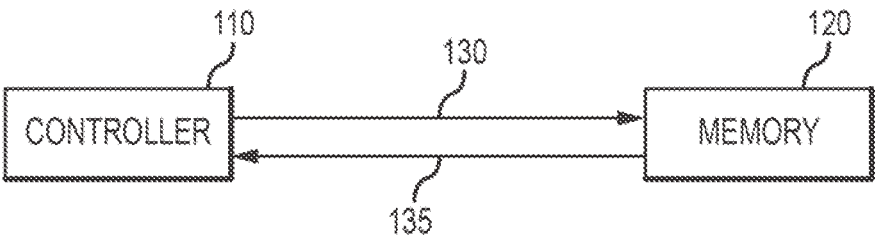


FIGURE 1A

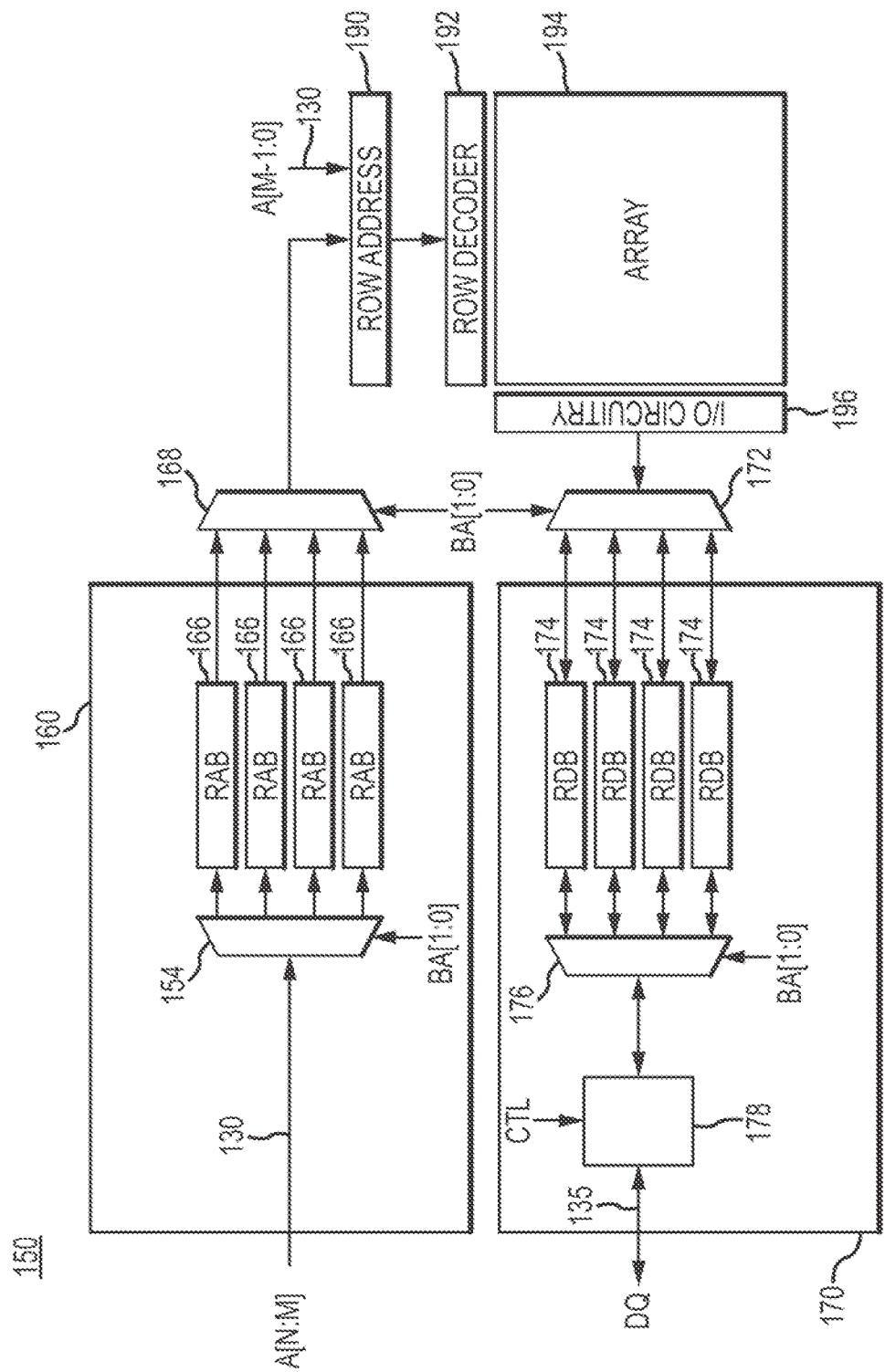


FIGURE 1B

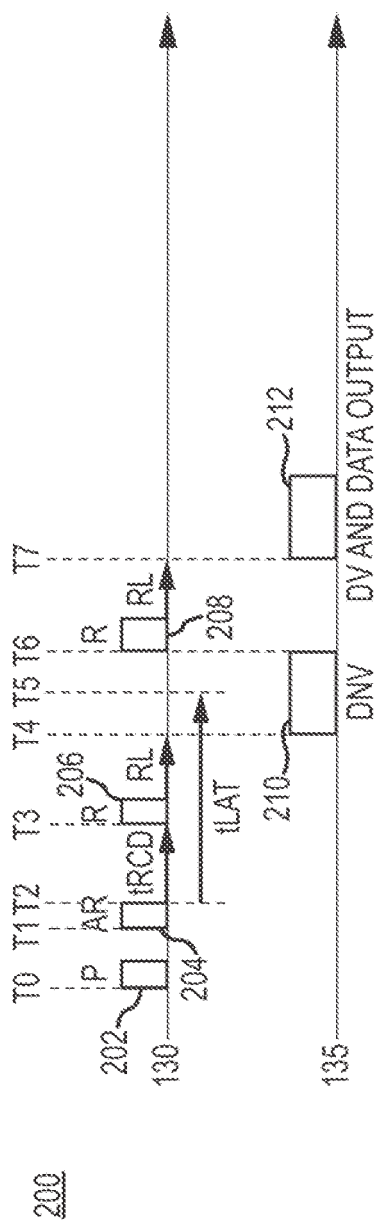


FIGURE 2A

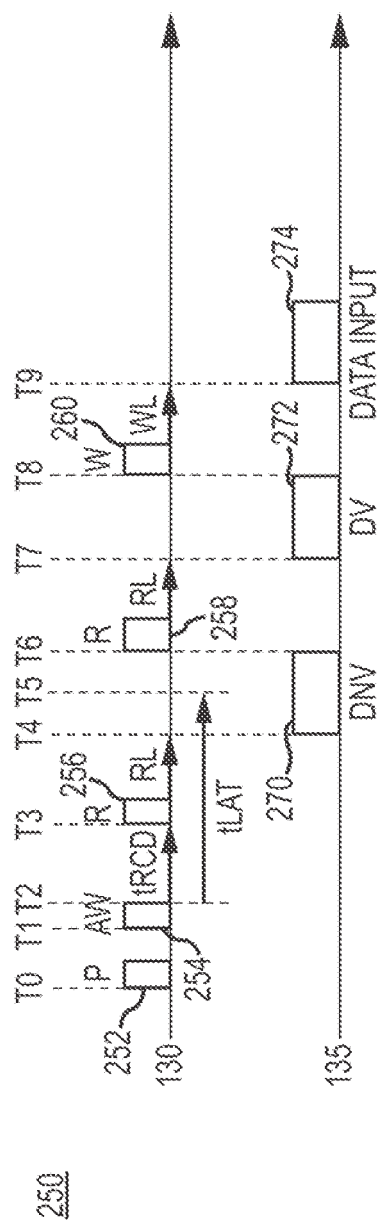


FIGURE 2B

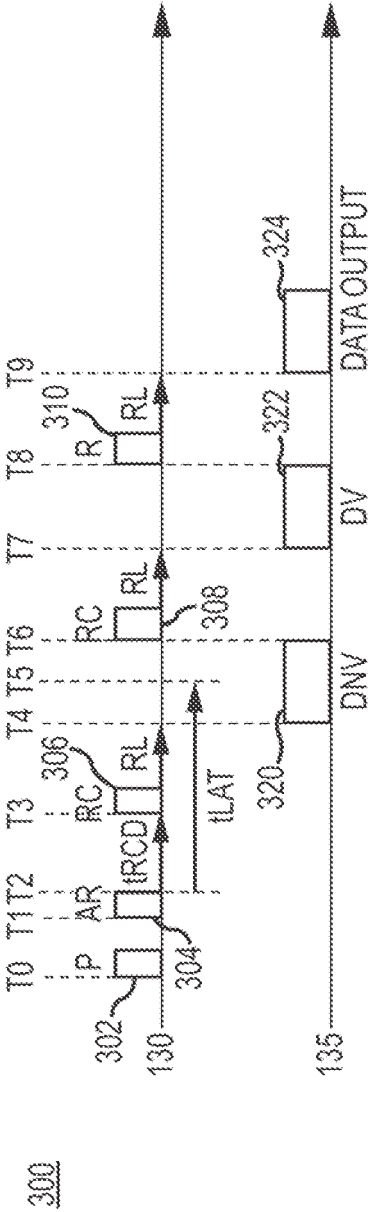


FIGURE 3A

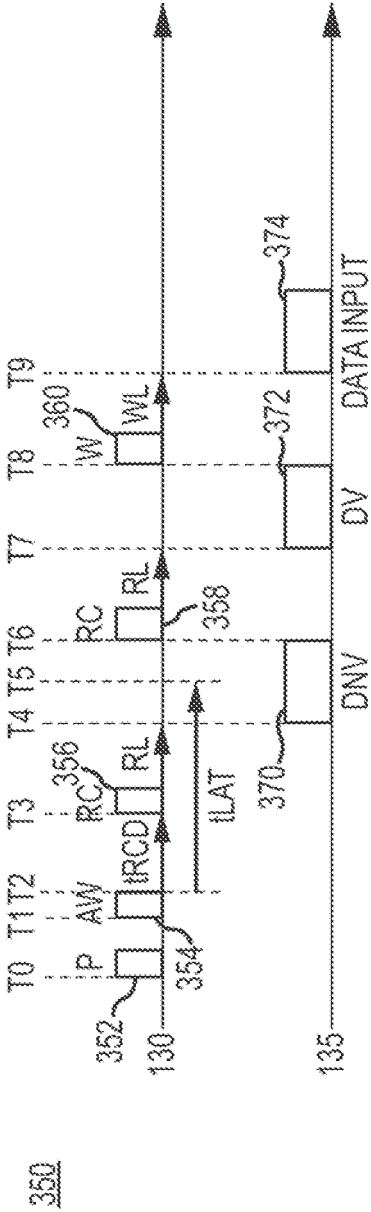


FIGURE 3B

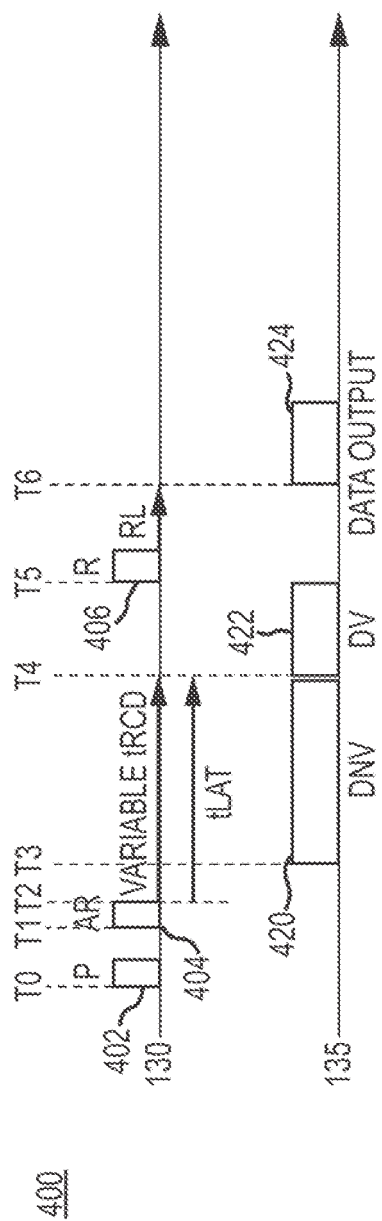


FIGURE 4A

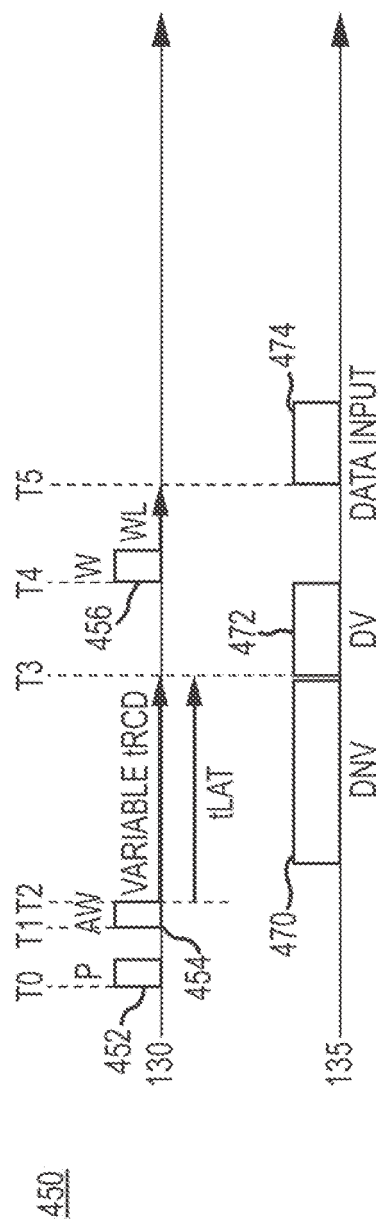


FIGURE 4B

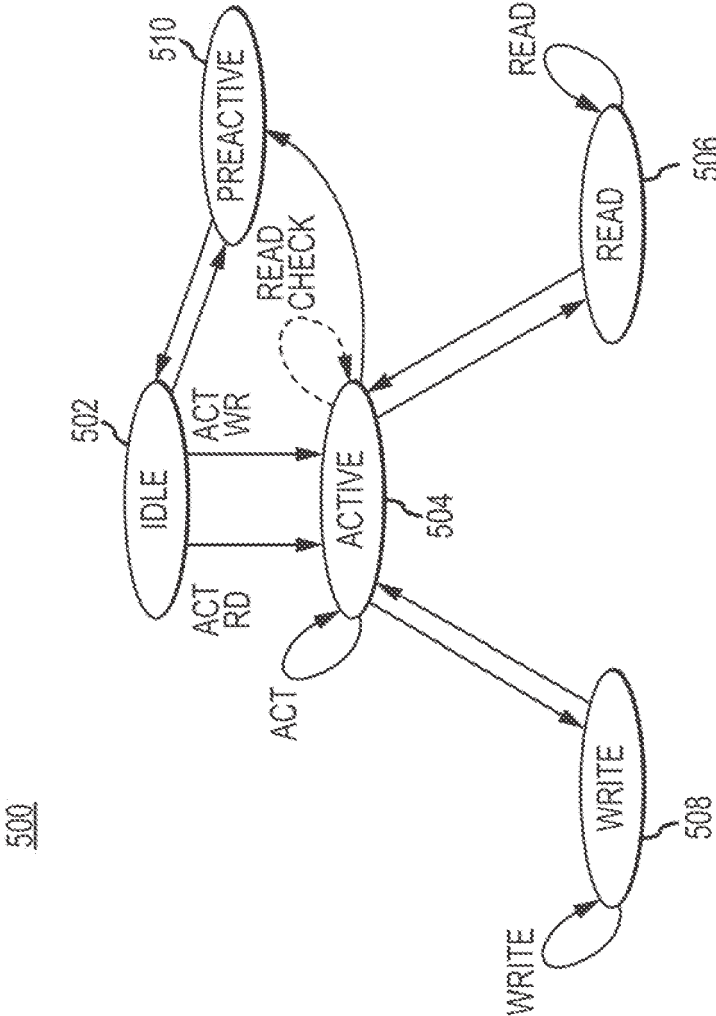


FIGURE 5

7/8

600

|          |                                                            |     |           |                                                                                                                                      |
|----------|------------------------------------------------------------|-----|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
| TOR[5:3] | TRANSPARENT<br>WRITE MAX<br>LATENCY TIME<br><br>(tMAXLATW) | 000 | UNLIMITED | tBUSY=LATENCY<br>CONFIGURATION<br>GRANULARITY (I.E. 25us)<br><br>UNLIMITED ALLOWS<br>MEMORY TO COMPLETE<br>ANY INTERNAL<br>OPERATION |
|          |                                                            | 001 | 1*tBUSY   |                                                                                                                                      |
|          |                                                            | 010 | 2*tBUSY   |                                                                                                                                      |
|          |                                                            | 011 | 3*tBUSY   |                                                                                                                                      |
|          |                                                            | 100 | 4*tBUSY   |                                                                                                                                      |
|          |                                                            | 101 | 5*tBUSY   |                                                                                                                                      |
|          |                                                            | 110 | 6*tBUSY   |                                                                                                                                      |
|          |                                                            | 111 | 7*tBUSY   |                                                                                                                                      |
| TOR[2:0] | TRANSPARENT<br>READ MAX<br>LATENCY TIME<br><br>(tMAXLATR)  | 000 | UNLIMITED | tBUSY=LATENCY<br>CONFIGURATION<br>GRANULARITY (I.E. 25us)<br><br>UNLIMITED ALLOWS<br>MEMORY TO COMPLETE<br>ANY INTERNAL<br>OPERATION |
|          |                                                            | 001 | 1*tBUSY   |                                                                                                                                      |
|          |                                                            | 010 | 2*tBUSY   |                                                                                                                                      |
|          |                                                            | 011 | 3*tBUSY   |                                                                                                                                      |
|          |                                                            | 100 | 4*tBUSY   |                                                                                                                                      |
|          |                                                            | 101 | 5*tBUSY   |                                                                                                                                      |
|          |                                                            | 110 | 6*tBUSY   |                                                                                                                                      |
|          |                                                            | 111 | 7*tBUSY   |                                                                                                                                      |

FIGURE 6

700

| BIT 3 | BIT 2 | BIT 1 | WAIT STATE                             |
|-------|-------|-------|----------------------------------------|
| 0     | 0     | 0     | "SHORT" → WAIT ASSERTED, <= 1us (E.G.) |
| 0     | 1     | 0     | "NORMAL" → WAIT ASSERTED, <= tBUSY     |
| 1     | 0     | 0     | "LONG" → WAIT ASSERTED, > tBUSY        |
| 1     | 1     | 0     | RESERVED                               |

FIGURE 7

800

| BIT3 | BIT2 | BIT1 | ACKNOWLEDGE EVENT | CURRENT READ<br>COMMAND                                                                                                       | CURRENT WRITE<br>COMMAND                                                                   |
|------|------|------|-------------------|-------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| 0    | 0    | 1    | WAIT DE-ASSERTED  | ACCEPTED                                                                                                                      |                                                                                            |
| 0    | 1    | 1    |                   | ACCEPTED BUT A HOUSE KEEPING<br>OPERATION IS SUGGESTED<br><br>ACTION: ISSUE HOUSE KEEPING<br>COMMAND                          |                                                                                            |
| 1    | 0    | 1    |                   | ACCEPTED BUT THERE HAS BEEN<br>AN ERROR DURING A PREVIOUS<br>OPERATION (E.G. LOCK ERROR)<br><br>ACTION: CHECK STATUS REGISTER |                                                                                            |
| 1    | 1    | 1    |                   | NA                                                                                                                            | REJECTED DUE<br>TO AN ERROR<br>(E.G. LOCK<br>ERROR)<br>ACTION: CHECK<br>STATUS<br>REGISTER |

FIGURE 8