

LINEAR AMPLIFIER

Background of the Invention

5 The present invention relates to amplifiers and, more particularly, to a linearized wide band amplifier.

 There are many applications which require the use of differential amplifiers in which it is not desirable to introduce non-linearities in the output signal produced
10 therefrom. One such application is in television receivers and, in particular, the differential IF input signal to the demodulator section of the TV demodulating system. Typically, a differential amplifier is used in the TV demodulating system as the interface between the IF
15 output stage and the demodulator. In general the IF output signal is a differential voltage that is applied to the differential amplifier. The differential amplifier converts the voltage to a differential current that is supplied to the demodulator of the TV demodulating system.
20 A problem associated with some prior art differential amplifiers is that distortion is introduced in the current outputs thereof due to the transistors base-emitter diode non-linearities. In monaural sound TV systems this may not be a problem. However, in high quality stereo TV
25 systems this distortion can lead to beat notes which can lie close to the sound carrier signal. If the distortion is high enough, these beat notes can become audible which is highly undesirable.

 In an attempt to eliminate this distortion, the prior
30 art has included linearizing stages coupled to the input stage of the differential amplifier. Because the linearizing stage of the prior art has a frequency response different than the direct signal path phase errors are introduced. Hence, although the prior art
35 linearizing scheme may work quite well at low frequencies,

distortion generated in the differential amplifier will not be cancelled at high frequencies due to the phase shift in the cancelling current path of the linearizing stage with respect to the direct input signal path.

5 Thus, a need exists for a wideband linearizing scheme for eliminating distortion in a differential amplifier.

Summary of the Invention

10 Accordingly, it is an object of the present invention to provide an improved differential amplifier.

It is another object of the invention to provide a linearized wide band differential amplifier.

15 In accordance with the above and other objects there is provided a differential amplifier comprising first and second differential amplifier sections each including first and second differentially connected transistor pairs with the bases of the first pair of transistors of the first and second differential amplifier sections coupled
20 respectively to first and second inputs of the amplifier while the bases of the second pair of transistors of the first and second differential amplifier sections are coupled to a terminal to which a reference potential is supplied, the collectors of the first pair of transistors
25 of the first differential amplifier section are interconnected with the collectors of one of the transistors of the second pair of transistors of the first and second differential amplifier sections respectively to a first output of the amplifier while the collectors of
30 the first pair of transistors of the second differential amplifier section are interconnected with the collectors of the other one of the transistors of the second pair of transistors of the first and second differential amplifier sections respectively to a second output of the amplifier;
35 and a linearizing element coupled between the emitters of

a respective transistor of the second pair of transistors of each of the first and second differential amplifier sections for providing a cancellation signal which cancels the non-linearity effects of the base-emitter diodes of the transistors of the amplifier.

Brief Description of the Drawing

The single Figure is a schematic diagram illustrating the differential amplifier of the present invention.

Detailed Description of the Preferred Embodiment

Turning to the single Figure there is shown linearized differential amplifier 10 of the present invention. It is understood that amplifier 10 is suited to be manufactured in monolithic integrated circuit form utilizing convention bipolar processing techniques. A load means 12 is coupled to first and second outputs 44 and 46 at which are supplied anti-phased output currents i_o and $-i_o$ respectively. Differential amplifier 10 converts a differentially applied input voltage V_i at inputs 14 and 16 to the differential output currents sourced at load means 12. A first differential amplifier section of amplifier 10 comprises first and second differentially connected pairs of transistors 18, 20: and 34:38. Similarly, a second differential amplifier section is formed by first and second differentially connected pairs of transistors 22:24 and 36:40. The bases of transistors 18 and 20 are coupled to input 14 while the bases of transistors 22 and 24 are coupled to input 16. The bases of transistors 34, 36, 38 and 40 are coupled to terminal 42 to which is supplied a reference voltage V_B . Transistors 18, 20, 38 and 40 have their collectors coupled to first output 44 while the collectors of

transistors 22, 24, 34 and 36 are coupled to second output 46. The emitters of the transistors are respectively coupled to constant current sources 26, 28, 30, 32, 48, 50, 52 and 54 which source equal currents I_E . The
5 emitter of transistor 18 is coupled to the emitter of transistor 34 via resistor 60 while the emitter of transistor 20 is coupled via resistor 62 to the emitter of transistor 38. Similarly, resistor 64 couples the emitter of transistor 24 to that of transistor 36 while resistor
10 66 couples the emitter of transistor 20 to the emitter of transistor 40. The operation of the differential amplifier sections is conventional as so far described in that a differential input voltage applied across inputs 14 and 16 causes transistors 18, 20, 36 and
15 40 to conduct while transistors 22, 24, 34 and 38 tend to be turned off and vice versa.

As will be described, non-linearity effects are created in the differential amplifier sections of amplifier 10 due to unequal changes in V_{BE} (the voltage
20 developed across the base-emitter diode of a transistor) of transistors 18 and 20 compared to transistors 34 and 38 in one section and transistors 22 and 24 compared to transistors 36 and 40 in the other section. For instance, as transistors 18 and 20 are turned on in response to a
25 positive voltage V_i at input 14 transistors 34 and 38 will be turned off. Similarly, transistors 36 and 40 will be turned on and transistors 22 and 24 will be turned off in response to the negative going voltage V_i at input 16. In this state the V_{BE} of transistors 18, 20, 36 and
30 40 will increase slightly while that of transistors 22, 24, 34 and 38 decreases greatly. Hence, the change in the current i_1 flowing through transistors 18, 20, 36 and 40 is not linear with respect to the change in the current $-i_1$ flowing through transistors 22, 24, 34 and 38 with
35 respect to the differential input voltage V_i and $-V_i$.

Thus, distortion is produced by the amplifier in converting the applied differential input voltage to a differential output current.

In the present invention the non-linear effects of the transistor base-emitter diodes in the differential amplifier sections is eliminated by use of a cancellation or linearizing circuit which, as illustrated, comprises resistor 56, that couples the emitter of transistor 36 to the emitter of transistor 38. The resistance of resistors 60, 62, 64 and 66 is equal to a value R_1 while that of resistor 56 is equal to a value R_2 .

In describing how the non-linear effects of the base-emitter diodes of the differential amplifier sections are cancelled it will be assumed that a positive going input voltage is applied at input 14 with respect to input 16 and that a voltage V_{BE1} is generated across the base-emitter of transistors 18 and 20 while a voltage V_{BE2} is developed across the base-emitter of transistors 22 and 24. As transistors 18 and 20 are turned on the current i_1 flows through the resistors 60 and 62 and via the transistors 34 and 38 to terminal 42. This develops a bias voltage across the base-emitter of these transistors equal to V_{BE2} . Similarly, as transistors 22 and 24 turn off, the current i_1 flows from transistors 36 and 38 through resistors 64 and 66 as shown. Thus, V_{BE1} is established across the base-emitter junction of these two transistors. The difference voltage between the emitters of transistors 36 and 38 establishes a current i_2 therethrough as well as resistor 56.

From the Figure is seen that the absolute magnitude of the anti-phase output currents produced at outputs 44 and 46 is equal to:

$$i_o = 3i_1 + i_2 - i_1; \text{ and} \quad (1)$$

$$i_o = 2i_1 + i_2 \quad (2)$$

Moreover,

$$V_i = i_1 R_1 + (V_{BE1} - V_{BE2}); \text{ or} \quad (3)$$

$$i_1 = \frac{V_i}{R_1} - \frac{(V_{BE1} - V_{BE2})}{R_1} \quad (4)$$

similarly,

$$i_2 = \frac{(V_{BE1} - V_{BE2})}{R_2} \quad (5)$$

Substituting equations 4 and 5 into equation 2 yields:

$$i_o = \frac{2V_i}{R_1} - \frac{2(V_{BE1} - V_{BE2})}{R_1} + \frac{(V_{BE1} - V_{BE2})}{R_2} \quad (6)$$

If $R_2 = R_1/2$, then:

$$i_o = \frac{2V_i}{R_1} \quad (7)$$

Thus, it is seen that the cancellation circuit of the present invention cancels the non-linear effects of the base-emitter diodes of the transistors of the input stage of differential amplifier 10 such that the output currents therefrom are a linear function of the differential applied input voltage V_i .

Hence, what has been described above is a novel differential amplifier the output of which is linear over a wideband of input signal frequencies. The amplifier includes first and second differential amplifier sections and a linearizing element the latter of which cancels the effect of diode non-linearities of the base-emitter junctions of the transistors comprising the differential amplifier.



Claims

5 1. An amplifier (10), comprising:

 a first differential amplifier section including
first and second differentially connected transistor pairs
(18,34; 20,38), the bases of the first pair of transistors
(18,20) being coupled to a first input (14) of the
10 amplifier, the bases of the second pair of transistors
(34,38) being coupled to a terminal (42) to which a
reference potential is supplied, the collectors of the
first pair of transistors and a first one of the second
pair of transistors being coupled to a first output of the
15 amplifier and the collector of the second one of the
second pair of transistors being coupled to a second
output of the amplifier;

 a second differential amplifier section including
first and second differentially connected transistor pairs
20 (22,40; 24,36), the bases of the first pair of transistors
(22,24) being coupled to a second input (16) of the
amplifier, the bases of the second pair of transistors
(36,40) being coupled to said terminal, the collectors of
the first pair of transistors and a first one of said
25 second pair of transistors being coupled to said second
output of the amplifier and the collector of the second
one of said second pair of transistors being coupled to
said first output of the amplifier; and

 circuitry (56) coupled between the emitters of
30 said first transistors (36,38) of said second pair of
transistors respectively of said first and second
differential amplifier sections for providing a signal
which cancels the non-linear effects of the base-emitter
junctions of said transistors of the amplifier.



2. The amplifier of claim 1 wherein said circuitry (56) includes a resistor (R2) having a first resistance value.

5 3. The amplifier of claim 2 wherein said first differential amplifier section includes:

a first resistor (60) coupled between the emitters of the first one of said first pair of transistors and said second one of said second pair of transistors having
10 a predetermined resistance value; and

a second resistor (62) coupled between the emitters of the second one of said first pair of transistors and the said first transistor of said second pair of transistors having said predetermined resistance
15 value.

4. The amplifier of claim 3 wherein said second differential amplifier section includes:

a first resistor (64) coupled between the emitters of the first one of said first pair of transistors and said second transistor of said second pair of transistors having said predetermined resistance value; and
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a second resistor (66) coupled between the emitters of the second one of said first pair of transistors and said first transistor of said second pair of transistors having said predetermined resistance value.
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5. The amplifier of claim 4 wherein said resistance value of said first and second resistors of said first and second differential amplifier sections is twice said
30 resistance value of said resistor of said circuitry.

6. The amplifier of claim 5 including current supply means (I_E) coupled to the emitters of said transistors
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of said first and second differential amplifier sections
for sourcing a substantially constant current
therethrough.

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