

CLAIMS

1. A package substrate comprising:
a substrate body comprising a plurality of first contact points on a surface thereof configured for electrical connection to a first die and a plurality of second contact points on the surface configured for electrical connection to a second die; and
a bridge embedded in the substrate body, the bridge comprising active device circuitry that is coupled to ones of the plurality of first contact points and ones of the plurality of second contact points, wherein the active device circuitry comprises a memory controller and a memory interface.
2. The package substrate of claim 1, wherein the active device circuitry comprises at least one repeater.
3. The package substrate of claim 2, wherein the at least one repeater is disposed in a signal path between one of the plurality of first contact points and one of the plurality of second contact points.
4. The package substrate of claim 1, wherein the active device circuitry comprises control logic.
5. The package substrate of claim 1, wherein the first plurality of contact points are operable for connection to a microprocessor and the second plurality of contact points are operable for connection to at least one memory die.
6. The package substrate of claim 1, wherein the bridge comprises at least one passive signal line coupled to one of the plurality of first contact points and one of the plurality of second contact points.

7. A package assembly comprising:
 - a package substrate body comprising a plurality of first contact points on a surface thereof configured for electrical connection to a first die and a plurality of second contact points on the surface configured for electrical connection to a second die;
 - a bridge embedded in the substrate body, the bridge comprising active device circuitry that is coupled to ones of the plurality of first contact points and ones of the plurality of second contact points; and
 - the first die coupled to the plurality of first contact points and the second die coupled to the plurality of second contact points, wherein the active device circuitry comprises a memory controller and a memory interface.
8. The package assembly of claim 7, wherein the active device circuitry is configured to route input/output electrical signals.
9. The package assembly of claim 7, wherein the active device circuitry comprises at least one repeater.
10. The package assembly of claim 9, wherein the at least one repeater is disposed in a signal path between one of the plurality of first contact points and one of the plurality of second contact points.
11. The package assembly of claim 7, wherein the active device circuitry comprises control logic.
12. The package assembly of claim 7, wherein the active device circuitry comprises a memory circuit.
13. The package assembly of claim 7, wherein the first die is a microprocessor and the second die is at least one memory die.

14. The package assembly of claim 7, wherein the first die is a microprocessor and the second die is a microprocessor.
15. The package assembly of claim 7, wherein the bridge comprises at least one passive signal line coupled to one of the plurality of first contact points and one of the plurality of second contact points.
16. A method of forming a package assembly comprising:
 - coupling a first die to a package substrate, the package substrate comprising a bridge substrate comprising active device circuitry; and
 - coupling a second die to the package substrate,
 - wherein coupling the first die and the second die to the package substrate comprises coupling the first die and the second die to the active device circuitry, wherein the active device circuitry comprises a memory controller and a memory interface.
17. The method of claim 16, wherein the active device circuitry comprises a repeater.
18. The method of claim 16, wherein the first die is a microprocessor and the second die is at least one memory die.
19. The method of claim 16, wherein the first die is a microprocessor and the second die is a microprocessor.
20. The package substrate of claim 1, wherein the bridge comprises at least one of a transistor or a memory element.
21. The package substrate of claim 1, wherein the bridge comprises one or more through silicon vias (TSVs).
22. The package substrate of claim 1, wherein the bridge comprises a DRAM controller.

23. The package substrate of claim 1, wherein the bridge comprises a semiconductor material.
24. The package assembly of claim 7, wherein the bridge comprises at least one of a transistor or a memory element.
25. The package assembly of claim 7, wherein the bridge comprises one or more through silicon vias (TSVs).
26. The package assembly of claim 7, wherein the bridge comprises a DRAM controller.
27. The package assembly of claim 7, wherein the bridge comprises a semiconductor material.
28. The method of claim 16, further comprising:
forming at least one of a transistor or a memory element in the bridge substrate.
29. The method of claim 16, further comprising:
forming one or more through silicon vias (TSVs) in the bridge substrate.
30. The method of claim 16, further comprising:
forming a DRAM controller in the bridge substrate.
31. The method of claim 16, wherein the bridge substrate comprises a semiconductor material.