

ABSTRACT

An integrated circuit device includes a shuffler, a logic unit and registers each including two or more bit storages. The shuffler receives an address indicating one of the registers and data bits, selects target bit storages at which the data bits are to be stored from among bit storages of the registers depending on a shuffle configuration and the address, stores the data bits into the target bit storages, and transfers the data bits from the target bit storages depending on the shuffle configuration. The logic unit receives the data bits transferred from the shuffler and operates using the received data bits. The shuffle configuration is adjusted when a reset operation is performed.

FIG. 3