

Description

This invention relates to semiconductor memories or arrays and more particularly to a stacked double density memory module which uses industry standard memory chips.

Integrated circuit semiconductor memory chips are widely employed in data processing systems ranging from inexpensive home or personal computers to large mainframe systems. Integrated circuit memory chips, hereinafter referred to as memory chips or chips, comprise a packaged (encapsulated) semiconductor memory array, provided with a plurality of input/output pins. Presently, read/write memory chips, also referred to as Dynamic Random Access Memories (DRAMs), are available from many suppliers worldwide. The package dimensions and pin assignments for all memory chips having the same bit storage capacity are standardized, so that memory chips of the same bit storage capacity are interchangeable, regardless of the supplier.

One commonly used memory chip is the 64K DRAM. The 64K DRAM stores approximately 65,000 bits of data and is widely available in dual-in-line plastic, ceramic or plastic/ceramic packages. Regardless of the supplier, all 64K DRAMs are interchangeable in that the package dimensions and pin assignments are standardized. In particular, the industry standard 64K DRAM is available in a 16 pin package having the following pin assignments (with the pins being numbered counterclockwise from the upper left corner of the chip):

Pin Number(s) Pin Function

1 No connect—unused

2 Data Input

3 Write Enable

4 Row Address Select-Chip Enable

5-7, 9-13 Address

8, 16 Power Supply

14 Data Output

15 Column Address Select

In the quest for ever increasing storage density, computer designers have realized that stacked memory chips may be employed to double the storage density on a given printed circuit board. More particularly, since corresponding address, power supply, and data lines may be paralleled, two memory chips can be physically stacked upon one another with the bottom chip mounted on a printed circuit board or other second level package. Separate chip enable pin locations must be provided for each chip in order to select either

the top or bottom chip. When stacked memory modules are employed, the memory storage density per printed circuit board unit area is effectively doubled. With this advantage in mind, the art (US-A-4 364 620) has employed two basic approaches for stacking memory chips while still providing separate chip select pin locations for the top and bottom chips:

1. Larger Printed Circuit Board Footprint:

Since two chip select paths are required at every stacked chip location on the circuit board, the chip select pins from the upper and lower chips may be routed to two separate printed circuit board locations. Thus, for example, two standard 16 pin 64K DRAMs may be mounted in an 18 pin socket, with the socket providing separate wiring paths for the chip enable pins from the top and bottom chips. Such an approach clearly wastes printed circuit board space because an 18 pin footprint is required for stacking two 16 pin chips. Moreover, a connector or housing for mounting the stacked DRAMs is generally required in order to provide the wiring paths from 16 pins to 18 pins. A connector or housing also wastes space on the printed circuit board, increases cost, and decreases the reliability of the stacked module, thereby offsetting some of the advantages of stacked chips.

2. Customized Pin Assignments:

The pin assignments of one or both of the chips may be rearranged from the industry standard to permit stacking. Thus, for example, in the 64K DRAM industry standard pin assignment, pin 1 is a no-connect (unused) pin and pin 4 is the row address select (chip enable) pin. Customized 64K DRAM chips may be procured wherein pin 1 is the row address select (chip enable) pin and pin 4 is a no-connect (unused) pin. Then, an industry standard and a customized 64K DRAM may be stacked. While such an approach does provide a 16 pin footprint on the printed circuit board, it will be understood that customized chips are much more expensive than industry standard chips because they are not available as off-the-shelf items. Accordingly, the increased cost of the non-standard chip offsets some of the advantage of stacked chips.

In conclusion, although the 64K DRAM is widely used in personal, mini, and mainframe computers, and in noncomputer oriented products such as video games, it has not been heretofore recognized that two 64K DRAMs may be stacked to obtain a double density memory module, without increasing the printed circuit board footprint size, without requiring the use of a socket or housing and without requiring customized pin assignments.

It is therefore an object of the invention to provide a stacked double density memory module which uses the same size printed circuit board footprint as that of the individual chips.

It is another object of the invention to provide a stacked double density memory module which

may be directly mounted on a printed circuit board, multilayer ceramic substrate or other second level package, without a connector or housing.

It is yet another object of the invention to provide a stacked double density memory module which employs two industry standard integrated circuit memory chips.

It is still another object of the invention to provide a method of stacking industry standard memory chips in a manner that is amenable to high volume manufacturing.

These and other objects are realized by the invention as defined in Claims 1, 7 and 13. The stacked double density memory module comprises two industry standard chips each of which includes a no-connect (unused) pin and a chip enable (select) pin. The no-connect and chip enable pins on the top chip are electrically jumpered. The chip select pin on the top chip is bent, or the end of the chip select pin is removed, so that the chip select pin on the top chip does not touch the chip select pin on the bottom chip when the two chips are stacked.

The jumpered (top) chip is then stacked on the bottom chip with each pin on the top chip contacting the corresponding pin on the bottom chip, except for the chip select pins. The bottom chip may be mounted on a printed circuit board or other second level package. Accordingly, for the stacked memory module, the industry standard no-connect pin position becomes the top chip select pin position. The bottom chip select pin position is the industry standard chip select pin position.

For the 64K DRAM described above, pins 1 (no-connect) and 4 (row address select) on the top chip are jumpered, and pin 4 is either bent or the end thereof is cut off. The chips are stacked with all pins touching except pins 4. For the stacked memory module, pin 1 becomes the top chip select while pin 4 becomes the bottom chip select.

In a preferred embodiment of the invention, for 64K DRAMs, the row/address select pin, (pin 4) and the no-connect pin (pin 1) are jumpered by means of a metal U-shaped strap. Each end of the U-strap has a hole therein, and the dimensions of the U-strap are such that pins 1 and 4 fit into a respective one of the holes, with the body of the U-strap running along the body of the chip. After placement of the U-strap, pin 4 is bent toward the body of the chip to hold the U-strap in place. The upper chip is then placed on top of the lower chip and the assembly is dip or wave soldered in a conventional manner. The soldering process also solders the U-strap to pins 1 and 4.

The above described double density memory module, and the above described process for fabricating the module permits industry standard 16 pin 64K DRAMs to be stacked in a 16 pin integrated circuit board footprint. A housing or connector is not needed. The individual process steps are conventional and the process adds little cost over the combined cost of the two 64K DRAMs. A double density memory module may

thus be realized with insignificant cost or reliability impact.

It will be recognized by those having skill in the art that the invention may be employed for stacking any DRAM chip, the industry standard pin assignment of which includes a no-connect pin. Accordingly, the invention may be employed with one megabit DRAMs, which have an 18 pin industry standard pin assignment including a no-connect pin. The invention may also be employed with any read/write or read only memory chip, as long as the industry standard pin assignment includes a no-connect pin. Accordingly, the invention may be employed for stacking static RAMs, ROMs (read only memories), PROMs (programmable read only memories) and EPROMs (erasable programmable read only memories). It will also be recognized that the invention may be applied to stack other array chips, e.g., programmable logic array chips, as long as the industry standard chip pin assignment includes a chip select pin and a no-connect pin.

Indeed, it will be recognized that the stacked chips need not be identical chips, as long as both industry standard chips include a chip select pin and a no-connect pin, and the function of each pin position is the same on both chips (i.e., the same pin positions are employed for address, power supply, data, enable and the no-connect functions). Thus, for example, a ROM and a PROM may be stacked according to the invention. The stacked chips need not even have the same footprint size, as long as both chips include a chip select pin and a no-connect pin, and the function of each overlapping pin position is the same on both chips.

It will also be recognized that jumpering techniques other than as described above may be employed. For example, a C, V or other shaped strap may be employed. Alternatively, the strap may be replaced by a wire wrap connecting the chip enable and no-connect pins. It will also be recognized that the jumper may be incorporated into a housing or connector to provide easy removability of the chips if desired.

An embodiment of the invention is described in the following with reference to three drawings.

Fig. 1 illustrates a preferred embodiment of the top chip of a stacked 64K DRAM module according to the present invention.

Fig. 2 illustrates a preferred embodiment of a stacked double density 64K DRAM module according to the present invention.

Fig. 3 illustrates the pin assignment of the stacked double density memory module of Fig. 2.

Referring now to Fig. 1, the top chip of a stacked module according to the present invention is illustrated. Top 64K DRAM chip 20 includes pins 1-16 which are labelled with reference to notch 21 according to the industry standard pin assignment outlined above. In the industry standard pin assignment, pin 1 is a no-connect, i.e., an unused pin, and pin 4 is the row address select pin which is the chip enable for the 64K DRAM. According to the invention, pins 1 and 4 are jumpered. As

shown in Fig. 1, the jumper is a U-shaped metal strap 22 having holes 23 and 24 at respective ends thereof. The dimensions of U-strap 22 are such that holes 23 and 24 are aligned with pins 1 and 4, respectively. After the U-strap is inserted on pins 1 and 4 as shown, pin 4 is bent toward the DRAM body as shown, in order to ensure that pin 4 does not touch corresponding pin 4 of the bottom chip when the chips are stacked, and also to ensure that U-strap 22 is held in place. In a preferred embodiment, U-strap 22 is tin plated brass to provide compatibility with the tin plated chip pins and with conventional lead-tin solders.

It will be recognized by those having skill in the art that strap 22 may be in the shape of a C (semicircle), V or other shape, and that the strap may be placed on pins 1 and 4 so that the body thereof runs along the side or top of chip 20. It will also be understood by those having skill in the art that strap 22 need not include holes 23 and 24. Rather, the ends of the strap may be abutted against pins 1 and 4 and pin 4 may be bent to hold the strap in place. Glue may also be employed to retain the strap in place against the chip prior to soldering.

It will also be recognized that rather than bending pin 4, the end thereof may be cut to ensure that it does not touch corresponding pin 4 of the lower chip when the chips are stacked. If pin 4 is cut rather than bent, glue may be employed to retain strap 22 in place. Finally, it will also be understood that a conductive wire may be wrapped around pin 1, routed underneath or on top of chip 20, and wrapped around pin 4 to provide the requisite jumpering.

Referring now to Fig. 2, there is illustrated a stacked double density module 30 according to the present invention. Module 30 provides 128K bits of storage. Top chip 20 is placed on bottom chip 25 so that the pins on top chip 20 touch corresponding pins on bottom chip 25, except for row address select pin 4. Module 30 may then be dip soldered or wave soldered in a conventional manner. The soldering process also solders the conductive U-strap to pins 1 and 4. It will be understood by those having skill in the art that if a conductive strap without holes is abutted against pins 1 and 4 on top chip 20, a high temperature solder process may first be employed to solder the strap to pins 1 and 4. Then the upper chip 20 and lower chip 25 may be stacked and soldered together using a low temperature solder process, thus ensuring that the strap is not disturbed.

It will also be understood that rather than soldering, an electrical connector or housing may be provided for mounting chips 20 and 25 therein. The housing may also include a built in jumper for electrically connecting pins 1 and 4 on top chip 20. Such a housing provides easy removability of the chips, at the expense of reliability and packaging density.

Fig. 3 illustrates the pin assignments for the 128K stacked memory module 30 according to the present invention. The pin assignments correspond to the industry standard 64K DRAM pin

assignments, except that pin 1 is now the top chip row address select (chip enable) pin while pin 4 is the bottom chip row address select (chip enable) pin. The module no longer includes a no-connect pin position. The module may be mounted on a printed circuit board or other second level package in a conventional manner, with separate signal lines being routed to top chip row address select pin position 1 and bottom chip row address select pin position 4.

It will be understood by those having skill in the art, that the word "chip", as used herein, refers to one or more pieces of semiconductor material which comprise a memory array, encapsulated or packaged in plastic, ceramic or other material and provided with a plurality of input/output pins. The word "module", as used herein, refers to two chips stacked according to the present invention. It will be noted that other references sometimes use the words IC (integrated circuit), LSI (large scale integrated circuit), DIP (dual-in-line package), or module, as synonymous for the word "chip" as used herein, and use the word chip to refer to the semiconductor material itself.

Claims

1. A method of forming a stacked double density memory module (30) from first (20) and second (25) industry standard memory chips, each of which includes a plurality of address, power supply and data pins, a chip select (4), and an unused pin (1), in the same pin positions on said first and second chips, characterized by the steps of:

jumpering the chip select pin (4) and the unused pin (1) on said first chip (20); and,

mounting said first chip on top of said second chip (25) with the pins on said first chip electrically contacting the corresponding pins on said second chip, except for the chip select pins (4).

2. The method of claim 1 wherein said jumpering step is characterized by:

placing a conductive strap (22) on said first chip (20), extending from said chip select pin (4) to said unused pin (1).

3. The method of claim 1 wherein said jumpering step is characterized by:

placing a conductive strap (22) having a hole (23, 24) at both ends thereof, along the bottom surface of said first chip (20), with the chip select pin (4) extending through one hole (24) and the unused pin (1) extending through the other hole (23).

4. The method of claim 2 or 3 wherein said mounting step is characterized by:

bending the chip select pin (4) on said first chip (20) toward said chip so that it retains said conductive strap (22) in place.

5. The method of claim 2 or 3 wherein said mounting step is characterized by:

removing the end of the chip select pin (4) on said first chip (20).

6. The method of claim 2 or 3, characterized in that said conductive strap (22) is a V, C, or U shaped strap.

shown in Fig. 1, the jumper is a U-shaped metal strap 22 having holes 23 and 24 at respective ends thereof. The dimensions of U-strap 22 are such that holes 23 and 24 are aligned with pins 1 and 4, respectively. After the U-strap is inserted on pins 1 and 4 as shown, pin 4 is bent toward the DRAM body as shown, in order to ensure that pin 4 does not touch corresponding pin 4 of the bottom chip when the chips are stacked, and also to ensure that U-strap 22 is held in place. In a preferred embodiment, U-strap 22 is tin plated brass to provide compatibility with the tin plated chip pins and with conventional lead-tin solders.

It will be recognized by those having skill in the art that strap 22 may be in the shape of a C (semicircle), V or other shape, and that the strap may be placed on pins 1 and 4 so that the body thereof runs along the side or top of chip 20. It will also be understood by those having skill in the art that strap 22 need not include holes 23 and 24. Rather, the ends of the strap may be abutted against pins 1 and 4 and pin 4 may be bent to hold the strap in place. Glue may also be employed to retain the strap in place against the chip prior to soldering.

It will also be recognized that rather than bending pin 4, the end thereof may be cut to ensure that it does not touch corresponding pin 4 of the lower chip when the chips are stacked. If pin 4 is cut rather than bent, glue may be employed to retain strap 22 in place. Finally, it will also be understood that a conductive wire may be wrapped around pin 1, routed underneath or on top of chip 20, and wrapped around pin 4 to provide the requisite jumpering.

Referring now to Fig. 2, there is illustrated a stacked double density module 30 according to the present invention. Module 30 provides 128K bits of storage. Top chip 20 is placed on bottom chip 25 so that the pins on top chip 20 touch corresponding pins on bottom chip 25, except for row address select pin 4. Module 30 may then be dip soldered or wave soldered in a conventional manner. The soldering process also solders the conductive U-strap to pins 1 and 4. It will be understood by those having skill in the art that if a conductive strap without holes is abutted against pins 1 and 4 on top chip 20, a high temperature solder process may first be employed to solder the strap to pins 1 and 4. Then the upper chip 20 and lower chip 25 may be stacked and soldered together using a low temperature solder process, thus ensuring that the strap is not disturbed.

It will also be understood that rather than soldering, an electrical connector or housing may be provided for mounting chips 20 and 25 therein. The housing may also include a built in jumper for electrically connecting pins 1 and 4 on top chip 20. Such a housing provides easy removability of the chips, at the expense of reliability and packaging density.

Fig. 3 illustrates the pin assignments for the 128K stacked memory module 30 according to the present invention. The pin assignments correspond to the industry standard 64K DRAM pin

assignments, except that pin 1 is now the top chip row address select (chip enable) pin while pin 4 is the bottom chip row address select (chip enable) pin. The module no longer includes a no-connect pin position. The module may be mounted on a printed circuit board or other second level package in a conventional manner, with separate signal lines being routed to top chip row address select pin position 1 and bottom chip row address select pin position 4.

It will be understood by those having skill in the art, that the word "chip", as used herein, refers to one or more pieces of semiconductor material which comprise a memory array, encapsulated or packaged in plastic, ceramic or other material and provided with a plurality of input/output pins. The word "module", as used herein, refers to two chips stacked according to the present invention. It will be noted that other references sometimes use the words IC (integrated circuit), LSI (large scale integrated circuit), DIP (dual-in-line package), or module, as synonymous for the word "chip" as used herein, and use the word chip to refer to the semiconductor material itself.

Claims

1. A method of forming a stacked double density memory module (30) from first (20) and second (25) industry standard memory chips, each of which includes a plurality of address, power supply and data pins, a chip select (4), and an unused pin (1), in the same pin positions on said first and second chips, characterized by the steps of:

jumpering the chip select pin (4) and the unused pin (1) on said first chip (20); and,

mounting said first chip on top of said second chip (25) with the pins on said first chip electrically contacting the corresponding pins on said second chip, except for the chip select pins (4).

2. The method of claim 1 wherein said jumpering step is characterized by:

placing a conductive strap (22) on said first chip (20), extending from said chip select pin (4) to said unused pin (1).

3. The method of claim 1 wherein said jumpering step is characterized by:

placing a conductive strap (22) having a hole (23, 24) at both ends thereof, along the bottom surface of said first chip (20), with the chip select pin (4) extending through one hole (24) and the unused pin (1) extending through the other hole (23).

4. The method of claim 2 or 3 wherein said mounting step is characterized by:

bending the chip select pin (4) on said first chip (20) toward said chip so that it retains said conductive strap (22) in place.

5. The method of claim 2 or 3 wherein said mounting step is characterized by:

removing the end of the chip select pin (4) on said first chip (20).

6. The method of claim 2 or 3, characterized in that said conductive strap (22) is a V, C, or U shaped strap.



7. A double density memory module characterized by:

first and second industry standard memory chips (20, 25), each of which includes a plurality of address, power supply and data pins, a chip select pin (4) and an unused pin (1), in the same pin positions on said first and second chips, with the pins on said first chip (20) electrically contacting the corresponding pins on said second chip (25), except for said chip select pins (4); and,

jumpering means (22) for electrically connecting said chip select pin (4) and said unused pin (1) on said first chip (20).

8. The double density memory module of claim 7 characterized in that said jumpering means (22) is a U, V, or C shaped conductive strap which runs from said chip select pin (4) to said unused pin (1) on said first chip (20).

9. The double density memory module of claim 8 characterized in that said U, V, or C shaped strap (22) has a hole (23, 24) at each end thereof, with the chip select pin (4) extending through the hole (24) at one end and the unused pin (1) extending through the hole (23) at the other end.

10. The double density memory module of claim 7 or 8, characterized in that the chip select pin (4) in said first chip (20) is bent toward the first chip, so that the chip select pin on said first chip does not contact the chip select pin (4) on said second chip (25).

11. The double density memory module of claim 7 or 8, characterized in that the end of the chip select pin (4) on said first chip (20) is removed so that the chip select pin on said first chip does not contact the chip select pin (4) on said second chip (20).

12. The double density memory module of claim 7, characterized in that said first and second industry standard memory chips (20, 25) do not have the same number of pins; the plurality of address, power supply, data, chip select and unused pins being in the same pin positions on said first and second chips to the extent that the corresponding pin positions overlap.

13. A double density memory board comprising a circuit board having a plurality of chip mounting positions thereon; and a first plurality of industry standard memory chips, each of which includes a plurality of address, power supply and data pins, a chip select pin and an unused pin, said first plurality of chips being mounted in at least some of the chip mounting positions on said circuit board; characterized by:

a second plurality of industry standard memory chips, each of which includes a plurality of address, power supply and data pins, a chip select pin and an unused pin, in the same pin positions as in said first plurality of chips, said second plurality of chips being mounted on top of at least some chips of said first plurality of chips, with each pin on each chip of said second plurality of chips being in electrical contact with the corresponding pin on the associated chip of the first plurality of chips, except for said chip select pins, each chip of said second plurality of chips

including jumpering means for electrically connecting the chip select pin and the unused pin on the respective chip.

14. The double density memory board of claim 13, characterized in that said circuit board includes at least one top chip select line routed to at least one of the unused pins in said first plurality of chips, and at least one bottom chip select line routed to at least one of the chip select pins in said first plurality of chips.

Patentansprüche

1. Verfahren zur Herstellung eines Stapel-Speichermoduls (30) doppelter Dichte aus ersten (20) und zweiten (25) Industriestandard-Speicherbausteinen, von denen jeder eine Mehrzahl von Adress-, Stromversorgungs- und Datenanschlüssen aufweist sowie einen Bausteinauswahlanschluss (4) und einen unbenutzten Anschluss (1), und zwar in den gleichen Anschlusspositionen auf den ersten und den zweiten Bausteinen, gekennzeichnet durch folgende Schritte:

Direktverbinden des Bausteinauswahlanschlusses (4) und des unbenutzten Anschlusses (1) auf dem ersten Baustein (20), und

Montieren des ersten Bausteins über dem zweiten Baustein (25), so dass die Anschlüsse des ersten Bausteins mit den Anschlüssen des zweiten Bausteins elektrischen Kontakt haben mit Ausnahme der Bausteinauswahlanschlüsse (4).

2. Verfahren gemäss Anspruch 1, wobei der Direktverbindungs-Schritt gekennzeichnet ist durch:

Anbringen eines leitenden Bügels (22) auf dem ersten Baustein (20), welcher sich von dem Bausteinauswahlanschluss (4) bis zu dem unbenutzten Anschluss (1) erstreckt.

3. Verfahren gemäss Anspruch 1, wobei der Direktverbindungs-Schritt gekennzeichnet ist durch:

Anbringen eines leitenden Bügels (22), welcher an beiden Enden je ein Loch (23, 24) hat, an der unteren Seite des ersten Bausteins (20), wobei sich der Bausteinauswahlanschluss (4) durch das eine Loch (24) und der unbenutzte Anschluss (23) durch das andere Loch erstreckt.

4. Verfahren gemäss Anspruch 2 oder 3, wobei der Montier-Schritt gekennzeichnet ist durch:

Umbiegen des Bausteinauswahlanschlusses (4) des ersten Bausteins (20) gegen diesen Baustein, so dass er den leitenden Bügel in seiner Lage festhält.

5. Verfahren gemäss Anspruch 2 oder 3, wobei der Montier-Schritt gekennzeichnet ist durch:

Entfernen des Endes des Bausteinauswahlanschlusses (4) beim ersten Baustein (20).

6. Verfahren gemäss Anspruch 2 oder 3, dadurch gekennzeichnet, dass der leitende Bügel (22) die Form eines V, C oder U hat.

7. Speichermodul doppelter Dichte, gekennzeichnet durch:

erste und zweite Industriestandard-Speicherbausteine (20, 25), von denen jeder eine Mehrzahl von Adress-, Stromversorgungs- und Datenan-



schlüssen aufweist sowie einen Bausteinwahlanschluss (4) und einen unbenutzten Anschluss (1), und zwar auf dem ersten und zweiten Baustein in den gleichen Anschlusspositionen, wobei die Anschlüsse des ersten Bausteins (20) mit den entsprechenden Anschlüssen des zweiten Bausteins (25) elektrischen Kontakt haben mit Ausnahme der Bausteinwahlanschlüsse (4), und eine Brücke (22) zur elektrischen Verbindung des Bausteinwahlanschlusses (4) und des unbenutzten Anschlusses (1) auf dem ersten Baustein (20).

8. Speichermodul doppelter Dichte gemäß Anspruch 7, dadurch gekennzeichnet, dass die Brücke (22) ein leitender Bügel in Form eines U, V oder C ist, welcher sich auf dem ersten Baustein (20) von dem Bausteinwahlanschluss (4) bis zu dem unbenutzten Anschluss (1) erstreckt.

9. Speichermodul doppelter Dichte gemäß Anspruch 8, dadurch gekennzeichnet, dass der Bügel (22) in Form eines U, V oder C je ein Loch (23, 24) an jedem Ende aufweist, wobei der Bausteinwahlanschluss (4) sich durch das eine Loch (24) und der unbenutzte Anschluss (1) sich durch das andere Loch (23) erstreckt.

10. Speichermodul doppelter Dichte gemäß Anspruch 7 oder 8, dadurch gekennzeichnet, dass der Bausteinwahlanschluss (4) des ersten Bausteins (20) gegen den ersten Baustein umgebogen wird, so dass der Bausteinwahlanschluss des ersten Bausteins keinen Kontakt mit dem Bausteinwahlanschluss (4) des zweiten Bausteins (25) hat.

11. Speichermodul doppelter Dichte gemäß Anspruch 7 oder 8, dadurch gekennzeichnet, dass das Ende des Bausteinwahlanschlusses (4) beim ersten Baustein (20) entfernt wird, so dass der Bausteinwahlanschluss des ersten Bausteins keinen Kontakt mit dem Bausteinwahlanschluss (4) des zweiten Bausteins (25) hat.

12. Speichermodul doppelter Dichte gemäß Anspruch 7, dadurch gekennzeichnet, dass die ersten und zweiten Industriestandard-Speicherbausteine (20, 25) nicht die gleiche Anzahl von Anschlüssen haben, wobei die Mehrzahl von Adress-, Stromversorgungs- und Datenanschlüssen sowie Bausteinwahlanschlüsse und unbenutzte Anschlüsse sich beim ersten und zweiten Baustein an den gleichen Anschlusspositionen befinden, soweit sich die betreffenden Anschlusspositionen überlappen.

13. Speicherkarte doppelter Dichte, mit einer Schaltungsplatte, welche eine Mehrzahl von Baustein-Montagepositionen aufweist, und mit einer ersten Mehrzahl von Industriestandard-Speicherbausteinen, deren jeder eine Mehrzahl von Adress-, Stromversorgungs- und Datenanschlüssen aufweist sowie einen Bausteinwahlanschluss und einen unbenutzten Anschluss, wobei diese erste Mehrzahl von Bausteinen auf mindestens einigen der Baustein-Montagepositionen der Schaltungskarte montiert sind; gekennzeichnet durch:

eine zweite Mehrzahl von Industriestandard-Speicherbausteinen, deren jeder eine Mehrzahl

von Adress-, Stromversorgungs- und Datenanschlüssen sowie einen Bausteinwahlanschluss und einen unbenutzten Anschluss aufweist, und zwar in den gleichen Anschlusspositionen wie bei der ersten Mehrzahl von Speicherbausteinen, wobei die zweite Mehrzahl von Bausteinen über wenigstens einigen Bausteinen der ersten Mehrzahl von Bausteinen montiert ist, und wobei jeder Anschluss eines jeden Bausteins der zweiten Mehrzahl von Bausteinen in elektrischem Kontakt ist mit dem entsprechenden Anschluss des zugehörigen Bausteins der ersten Mehrzahl von Bausteinen, mit Ausnahme der Bausteinwahlanschlüsse, und wobei jeder Baustein der zweiten Mehrzahl von Bausteinen eine Brücke enthält zur elektrischen Verbindung des Bausteinwahlanschlusses und des unbenutzten Anschlusses auf dem betreffenden Baustein.

14. Speicherkarte doppelter Dichte gemäß Anspruch 13, dadurch gekennzeichnet, dass die Schaltungsplatte wenigstens eine obere Bausteinwahlleitung aufweist, die zu wenigstens einem der unbenutzten Anschlüsse der ersten Mehrzahl von Bausteinen geführt ist, sowie wenigstens eine untere Bausteinwahlleitung, die zu wenigstens einem der Bausteinwahlanschlüsse der ersten Mehrzahl von Bausteinen geführt ist.

Revendications

1. Procédé pour former un module de mémoire empilé à double densité (30) à partir d'un premier (20) et d'un deuxième (25) circuits intégrés de mémoire industriels normalisés, chacun d'entre eux comportant une pluralité de broches d'adresses, d'alimentation et de données, une broche (4) de sélection de circuit intégré et une broche inutilisée (1) dans la même position de broche sur lesdits premier et deuxième circuits intégrés, caractérisé par les étapes suivantes:

la liaison de la broche (4) de sélection de circuit intégré et de la broche inutilisée (1) sur ledit premier circuit intégré (20); et

le montage dudit premier circuit intégré au-dessus dudit deuxième circuit intégré (25), les broches sur ledit premier circuit intégré venant électriquement en contact avec les broches correspondantes sur ledit deuxième circuit intégré, à l'exception des broches (4) de sélection de circuit intégré.

2. Procédé selon la revendication 1, dans lequel ladite étape de liaison est caractérisée par:

la disposition d'une pièce conductrice (22) sur ledit premier circuit intégré (20), s'étendant de ladite broche de sélection de circuit intégré (4) à ladite broche inutilisée (1).

3. Procédé de la revendication 1, dans lequel ladite étape de liaison est caractérisée par:

la disposition d'une pièce conductrice (22), possédant un trou (23, 24) à ses deux extrémités, le long de la surface inférieure dudit premier circuit intégré (20), la broche (4) de sélection de circuit intégré s'étendant à travers l'un (24) des trous et la broche inutilisée (1) s'étendant à travers l'autre trou (23).



14

4. Procédé de la revendication 2 ou 3 dans lequel ladite étape de montage est caractérisée par:

le pliage de la broche (4) de sélection de circuit intégré sur ledit premier circuit intégré (20) vers ledit circuit intégré de telle sorte qu'elle maintienne ladite pièce conductrice (22) en place.

5. Procédé de la revendication 2 ou 3 dans lequel ladite étape de montage est caractérisée par:

le retrait de l'extrémité de la broche (4) de sélection de circuit intégré sur ledit premier circuit intégré (20).

6. Procédé de la revendication 2 ou 3, caractérisé en ce que ladite pièce conductrice (22) est une pièce en forme de V, de C ou de U.

7. Module de mémoire à double densité caractérisé par:

des premier et deuxième circuits intégrés de mémoire industriels normalisés (20, 25), comportant chacun une pluralité de broches d'adresses, d'alimentation et de données, une broche (4) de sélection de circuit intégré et une broche inutilisée (1), dans les mêmes positions de broches sur lesdits premier et deuxième circuits intégrés, les broches sur ledit premier circuit intégré (20) établissant un contact électrique avec les broches correspondantes sur ledit deuxième circuit intégré (25), à l'exception desdites broches de sélection de circuit intégré (4); et

des moyens de liaison (22) pour connecter électriquement ladite broche (4) de sélection de circuit intégré et ladite broche inutilisée (1) sur ledit premier circuit intégré (20).

8. Module de mémoire à double densité de la revendication 7, caractérisé en ce que lesdits moyens de liaison (22) sont une pièce conductrice en forme de U, de V ou de C qui va de ladite broche (4) de sélection de circuit intégré à ladite broche inutilisée (1) sur ledit premier circuit intégré (20).

9. Module de mémoire à double densité de la revendication 8, caractérisé en ce que ladite pièce (22) en forme de U, de V ou de C possède un trou (23, 24) à chaque extrémité de celle-ci, la broche (4) de sélection de circuit intégré s'étendant à travers le trou (24) à l'une des extrémités et la broche inutilisée (1) s'étendant à travers le trou (23) à l'autre extrémité.

10. Module de mémoire à double densité de la revendication 7 ou 8, caractérisé en ce que la broche (4) de sélection de circuit intégré sur ledit premier circuit intégré (20) est pliée vers le premier circuit intégré, de telle sorte que la broche de sélection de circuit intégré sur ledit premier circuit intégré ne vienne pas en contact avec la broche (4) de sélection de circuit intégré sur ledit deuxième circuit intégré (25).

11. Module de mémoire à double densité de la revendication 7 ou 8, caractérisé en ce que l'extrémité de la broche (4) de sélection de circuit intégré sur ledit premier circuit intégré (20) est

retirée, de telle sorte que la broche de sélection de circuit intégré sur ledit premier circuit intégré ne vienne pas en contact avec la broche de sélection de circuit intégré (4) sur ledit deuxième circuit intégré (25).

12. Module de mémoire à double densité de la revendication 7, caractérisé en ce que lesdits premier et deuxième circuits intégrés de mémoire industriels normalisés (20, 25) n'ont pas le même nombre de broches, la pluralité de broches d'adresses, d'alimentation, de données, de sélection de circuit intégré et de broches inutilisées se trouvant dans les mêmes positions de broches sur lesdits premier et deuxième circuits intégrés dans la mesure où les positions de broches correspondantes se chevauchent.

13. Carte de mémoires à double densité comportant une carte de circuit imprimé ayant sur celle-ci une pluralité de positions de montage de circuits intégrés; et une première pluralité de circuits intégrés de mémoire industriels normalisés, chacun d'entre eux comportant une pluralité de broches d'adresses, d'alimentation et de données, une broche de sélection de circuit intégré et une broche inutilisée, ladite première pluralité de circuits intégrés étant montée au moins dans quelques-unes des positions de montage de circuits intégrés sur ladite carte de circuit imprimé; caractérisé par:

une deuxième pluralité de circuits intégrés de mémoire industriels normalisés, chacun d'entre eux comportant une pluralité de broches d'adresses, d'alimentation et de données, une broche de sélection de circuit intégré et une broche inutilisée, dans les mêmes positions de broches que dans ladite première pluralité de circuits intégrés, ladite deuxième pluralité de circuits intégrés étant montée au moins au-dessus de certains des circuits intégrés de ladite première pluralité de circuits intégrés, chaque broche sur chaque circuit intégré de ladite deuxième pluralité de circuits intégrés établissant un contact électrique avec la broche correspondante sur le circuit intégré associé de la première pluralité de circuits intégrés, à l'exception desdites broches de sélection de circuit intégré, chaque broche de ladite deuxième pluralité de circuits intégrés comportant des moyens de liaison pour connecter électriquement la broche de sélection de circuit intégré et la broche inutilisée sur le circuit intégré respectif.

14. Carte de mémoires à double densité de la revendication 13, caractérisée en ce que ladite carte de circuit imprimé comporte au moins une ligne de sélection de circuits intégrés supérieurs allant jusqu'à au moins l'une des broches inutilisées dans ladite première pluralité de circuits intégrés, et au moins une ligne de sélection de circuits intégrés inférieurs allant jusqu'à au moins l'une des broches de sélection de circuit intégré dans ladite première pluralité de circuits intégrés.

