

FIG. 1

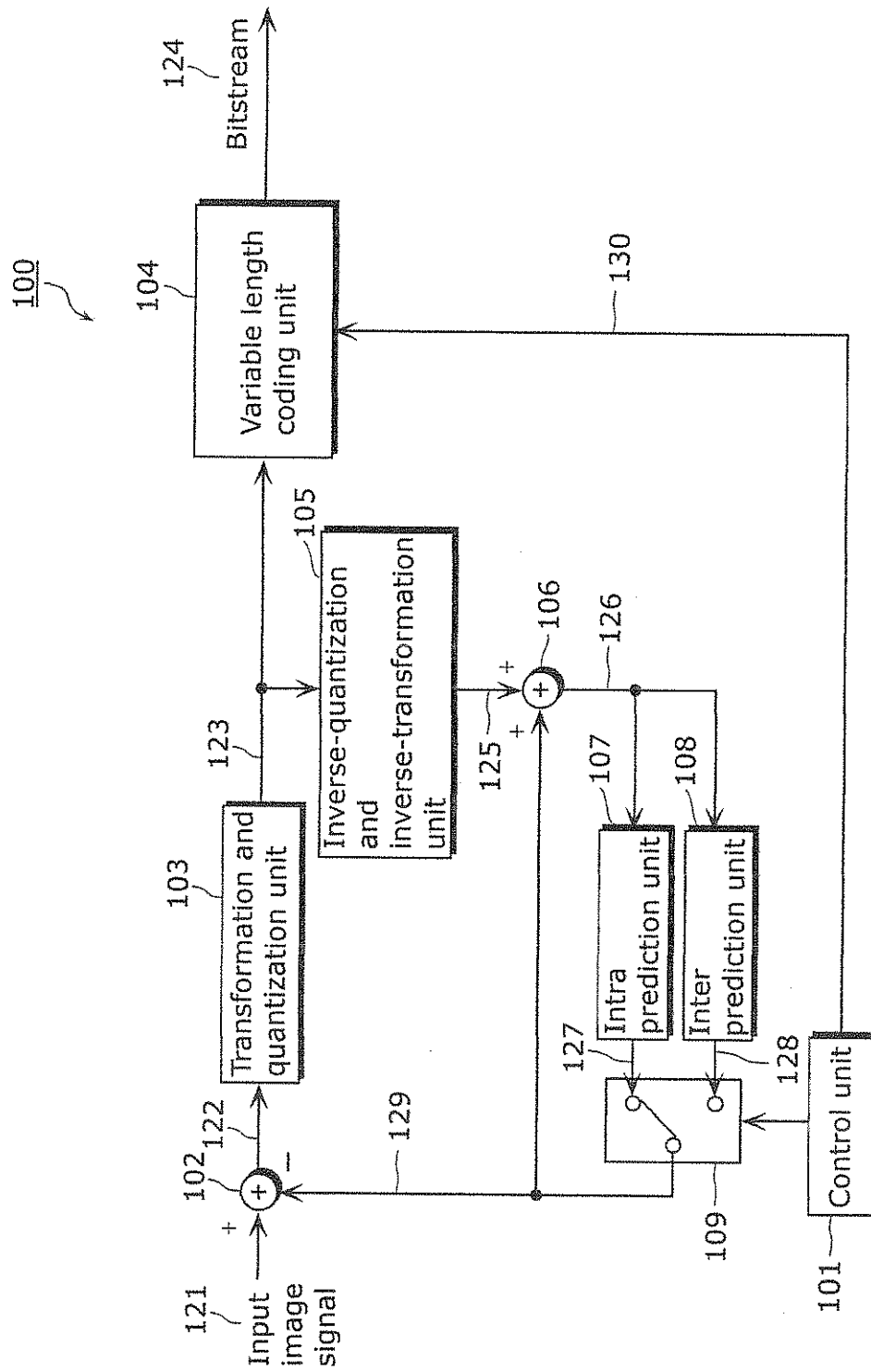


FIG. 2

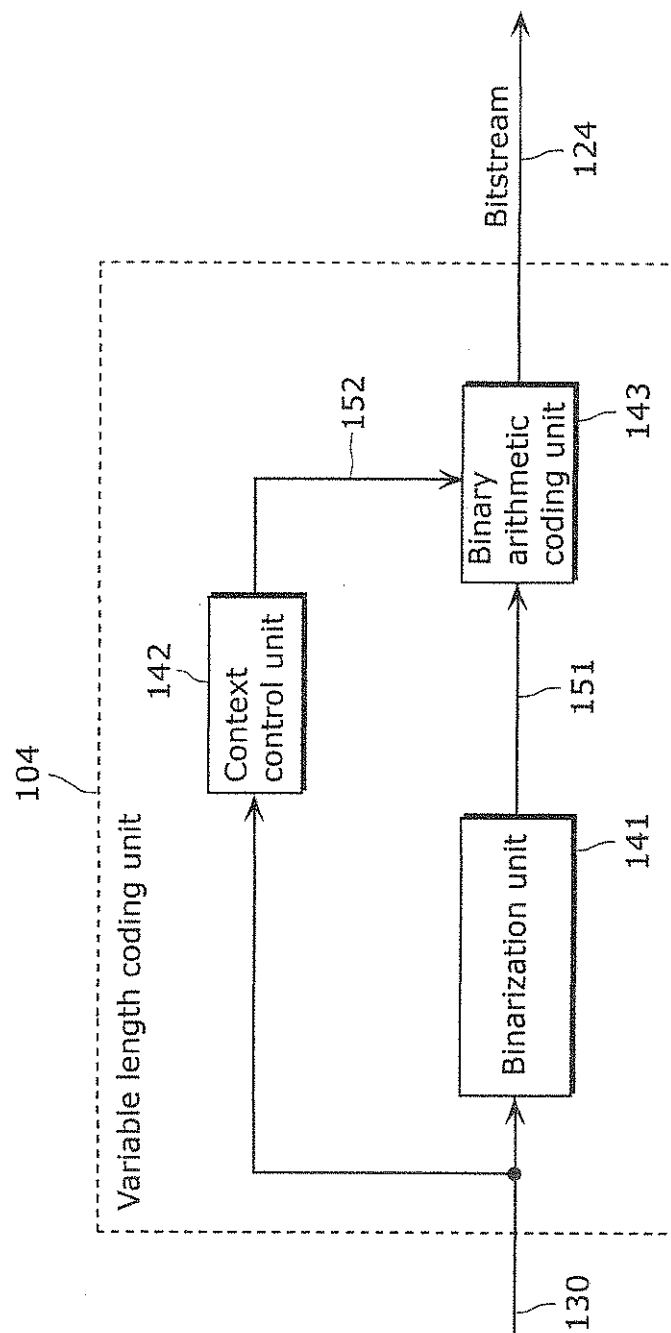


FIG. 3

	c2 Signal type	c3 Binanzization scheme	c4 Context model for first element	c5 Left block condition L condL	c6 Upper block condition A conda
s1	split_coding_unit_flag	Fixed length	0, 1, or 2 (condL && availableL) + (conda && availableA)	cuDepth[xL][yL] > cuDepth[xP][yP]	cuDepth[xA][yA] > cuDepth[xP][yP]
s2	skip_flag	Fixed length	0, 1, 2	skip_flag[xL][yL]	skip_flag[xA][yA]
s3	merge_flag	Fixed length	0, 1, 2	merge_flag[xL][yL]	merge_flag[xA][yA]
s4	intra_chroma_pred_mode	Variable length	0, 1, 2	IntraPredMode[xL][yL] == 4	IntraPredMode[xA][yA] == 4
s5	inter_pred_flag	Fixed length	0, 1, 2	inter_pred_flag[xL][yL]	inter_pred_flag[xA][yA]
s6	mvd_lc mvd_l0 mvd_l1	Variable length	0, 1, 2	mvd_lc[xL][yL] > 16 mvd_l0[xL][yL] > 16 mvd_l1[xL][yL] > 16	mvd_lc[xA][yA] > 16 mvd_l0[xA][yA] > 16 mvd_l1[xA][yA] > 16
s7	ref_idx_lc ref_idx_l0 ref_idx_l1	Variable length	0, 1, 2, or 3 (condL && availableL) + (conda && availableA) < 1	ref_idx_lc[xL][yL] > 0 ref_idx_l0[xL][yL] > 0 ref_idx_l1[xL][yL] > 0	ref_idx_lc[xA][yA] > 0 ref_idx_l0[xA][yA] > 0 ref_idx_l1[xA][yA] > 0
s8	Cbf_cb(MODE_INTRA)	Fixed length	0, 1, 2, 3	cbf_cb[xL][yL]	cbf_cb[xA][yA]
s9	Cbf_cr(MODE_INTRA)	Fixed length	0, 1, 2, 3	cbf_cr[xL][yL]	cbf_cr[xA][yA]
s10	Cbf_luma	Fixed length	0, 1, 2, 3	cbf_luma[xL][yL]	cbf_luma[xA][yA]
s10	no_residual_data_flag	Fixed length	0, 1, 2, 3	no_residual_data_flag[xL][yL]	no_residual_data_flag[xA][yA]
NA	alf_cu_flag	1bin	0, 1, 2	alf_cu_flag[xL][yL]	alf_cu_flag[xA][yA]

FIG. 4

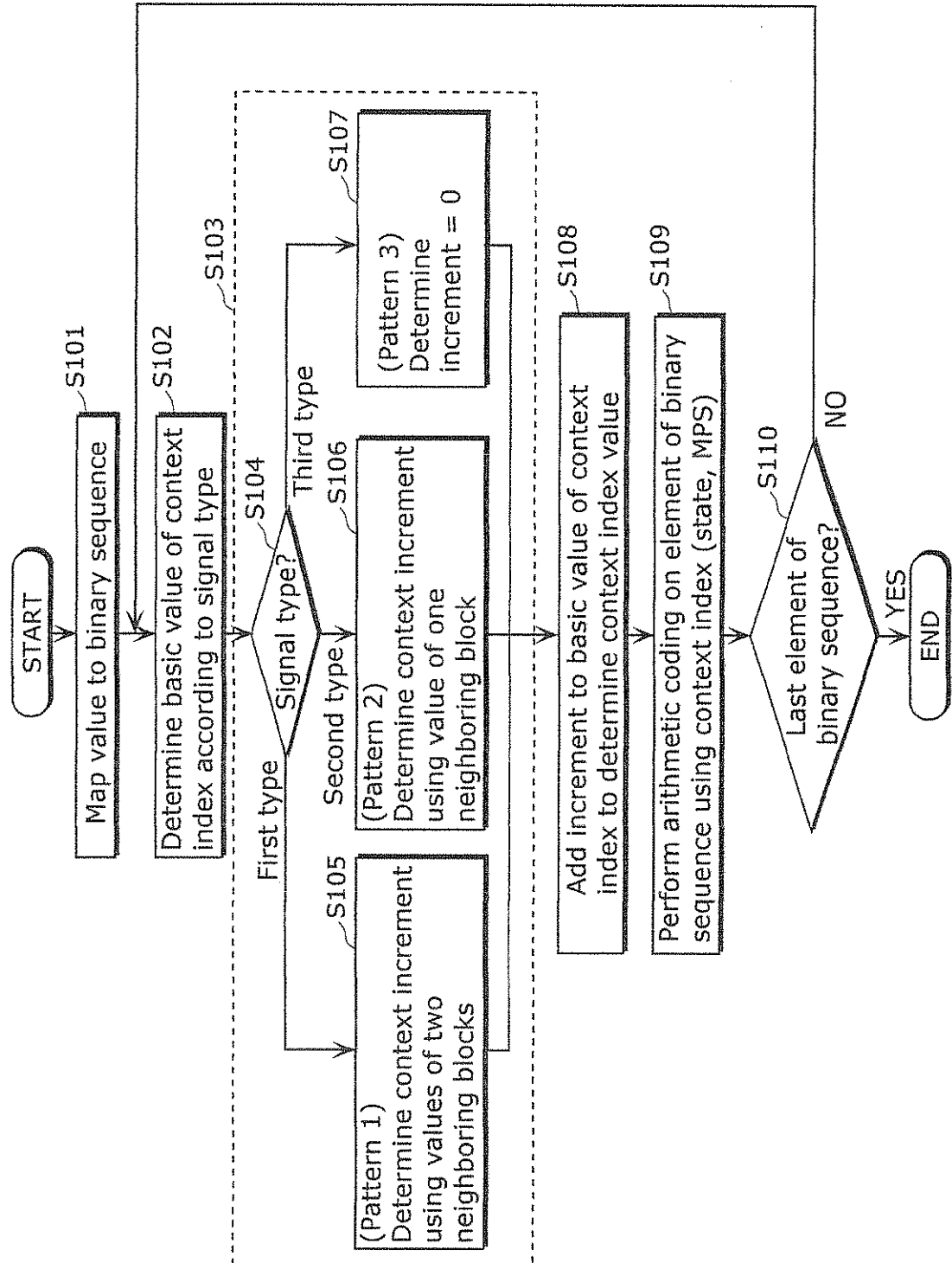


FIG. 5

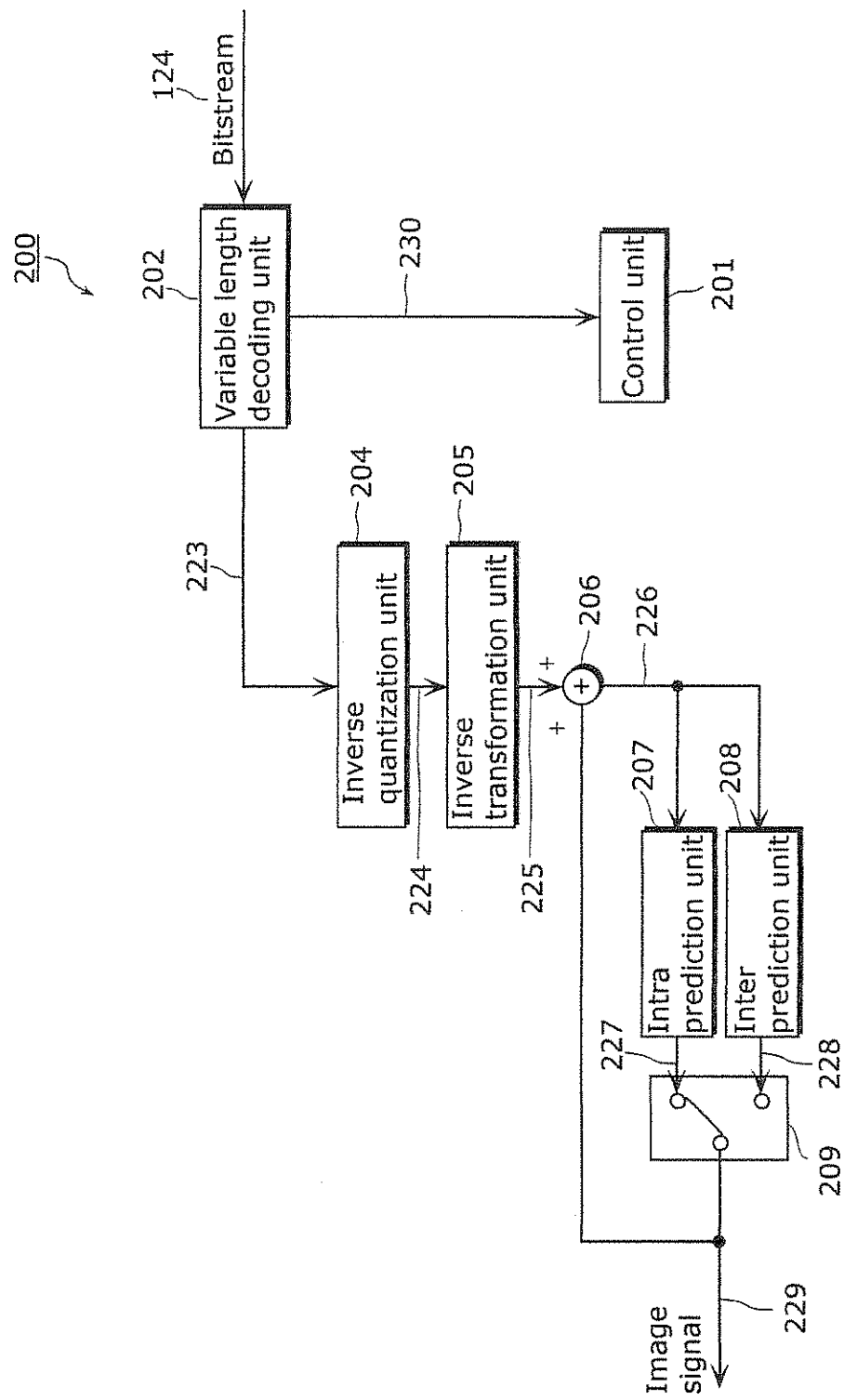


FIG. 6

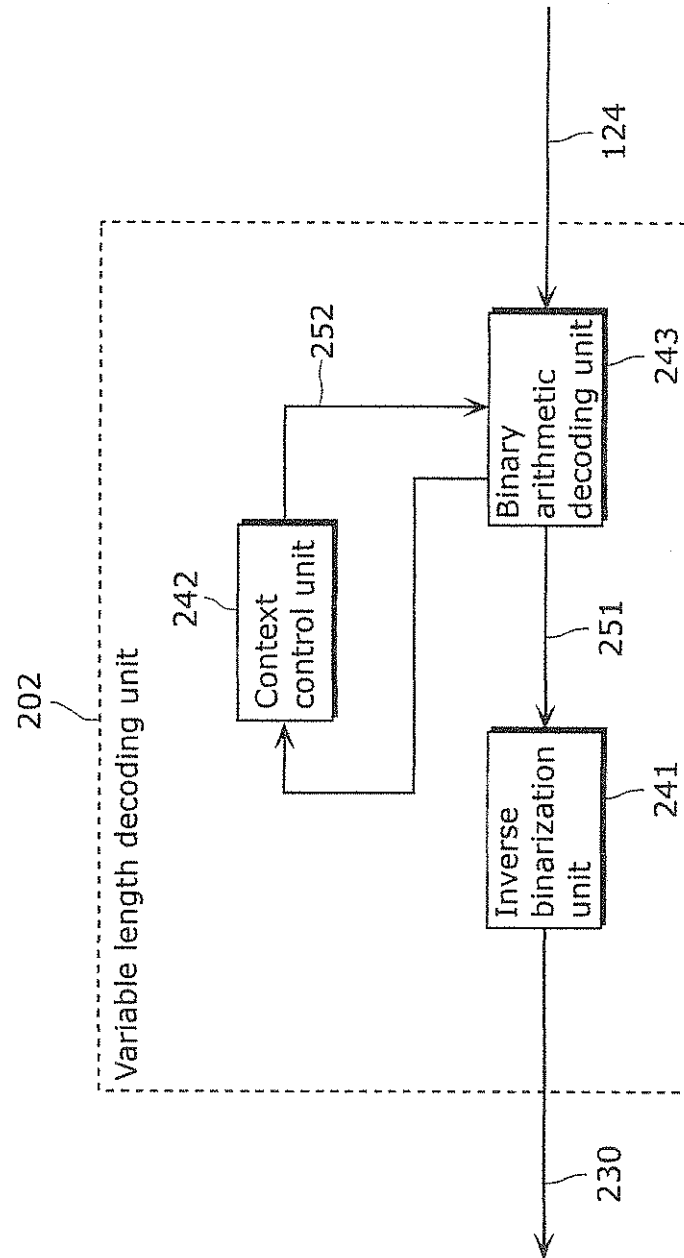


FIG. 7

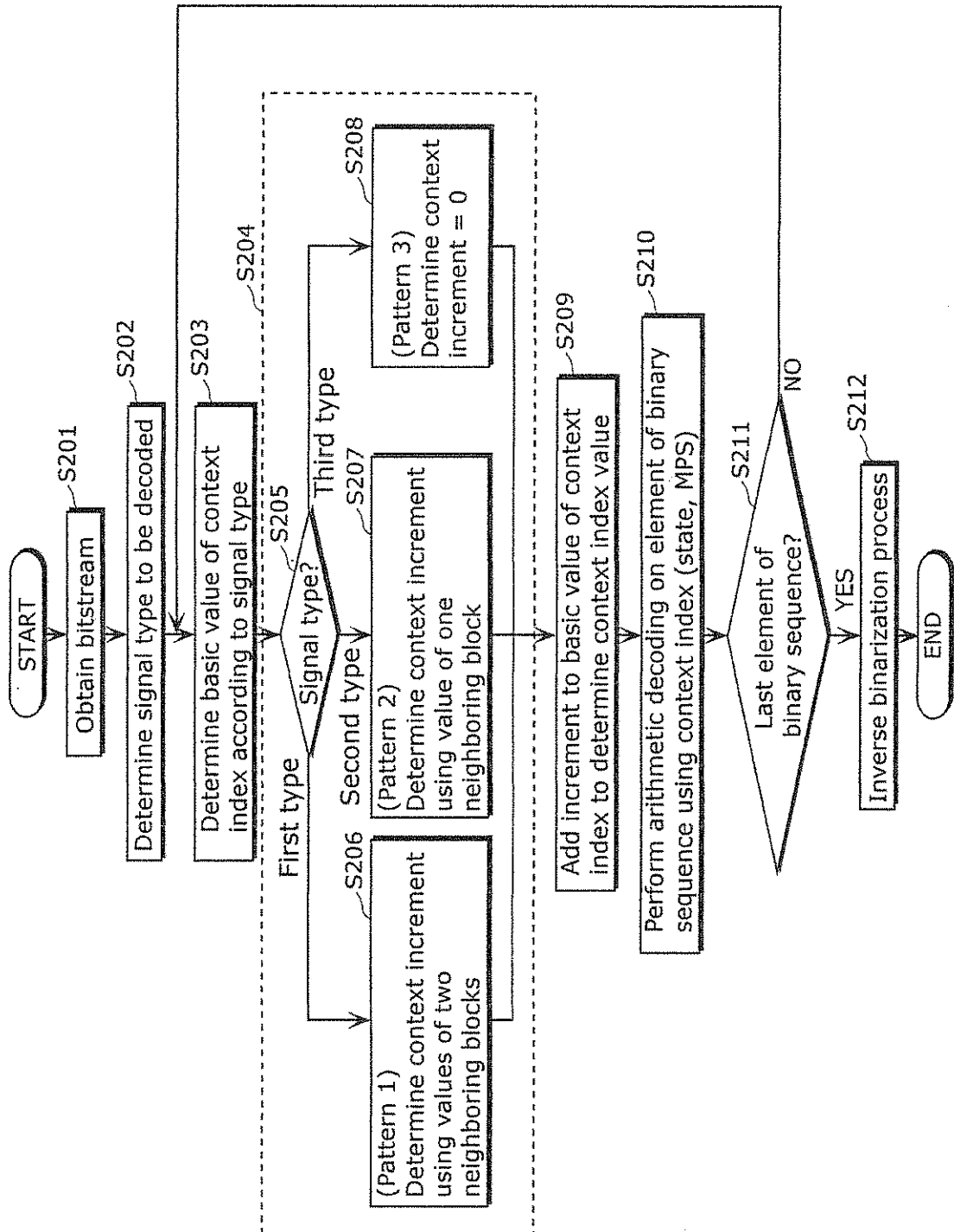


FIG. 8

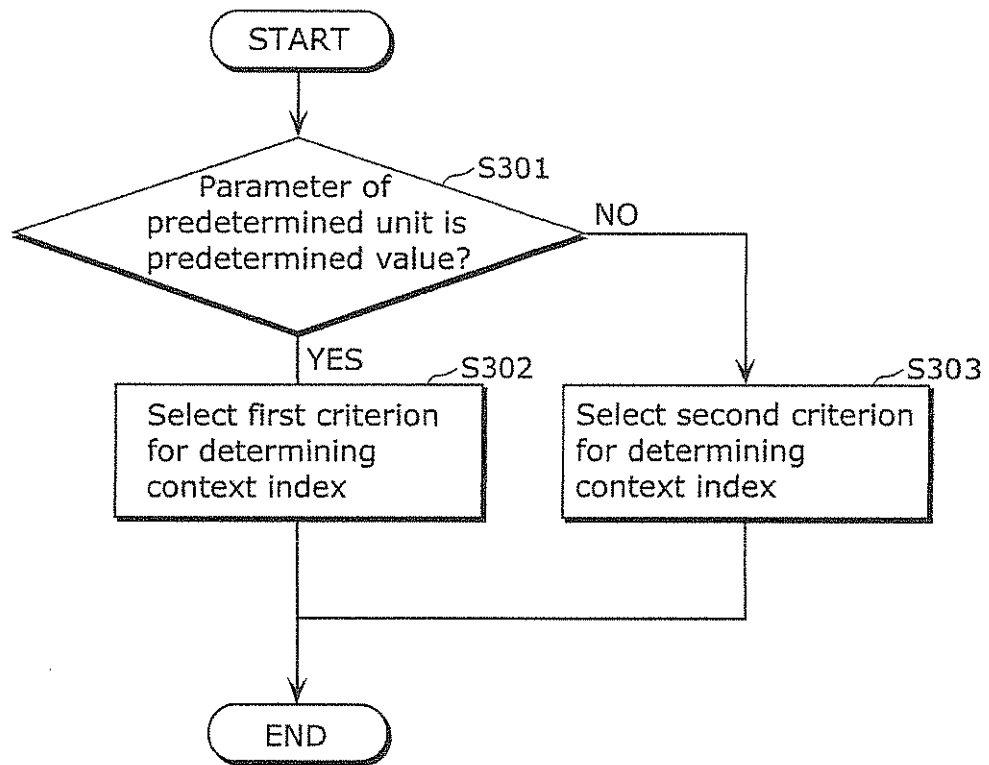


FIG. 9A

Same applies for all syntax elements

P picture													B picture															
mvd_10 [0] [0] Direction 1													mvd_10 [0] [0] mvd_11 [0] [0] mvd_1c [0] [0]															
901B																												
Relative value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
Context SET 1	ctxInc 0, 1, 2		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		ctxInc 0, 1, 2		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0	
(28 consumed)																												
902B																												
Relative value	0	1	2		3	4	5	6	7	8		9	10	11	12	13	14		15	16	17	18	19	20		21	22	23
Context SET 2	ctxInc 0, 1		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		ctxInc 0, 1		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0	
(24 consumed)																												
903B																												
Relative value	0	1		2	3	4	5	6	7	8		9	10	11	12	13	14		15	16	17	18	19	20		21	22	23
Context SET 3	ctxInc 0, 1		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		ctxInc 0, 1		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0	
(20 consumed)																												
904B																												
Relative value	0	1		2	3	4	5	6		7	8	9																
Context SET k	ctxInc 0, 1		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0		Reserved for binIdx > 0																	
(10 consumed)													904B															
													18 context indexes (28 to 10) reduction															

FIG. 9B

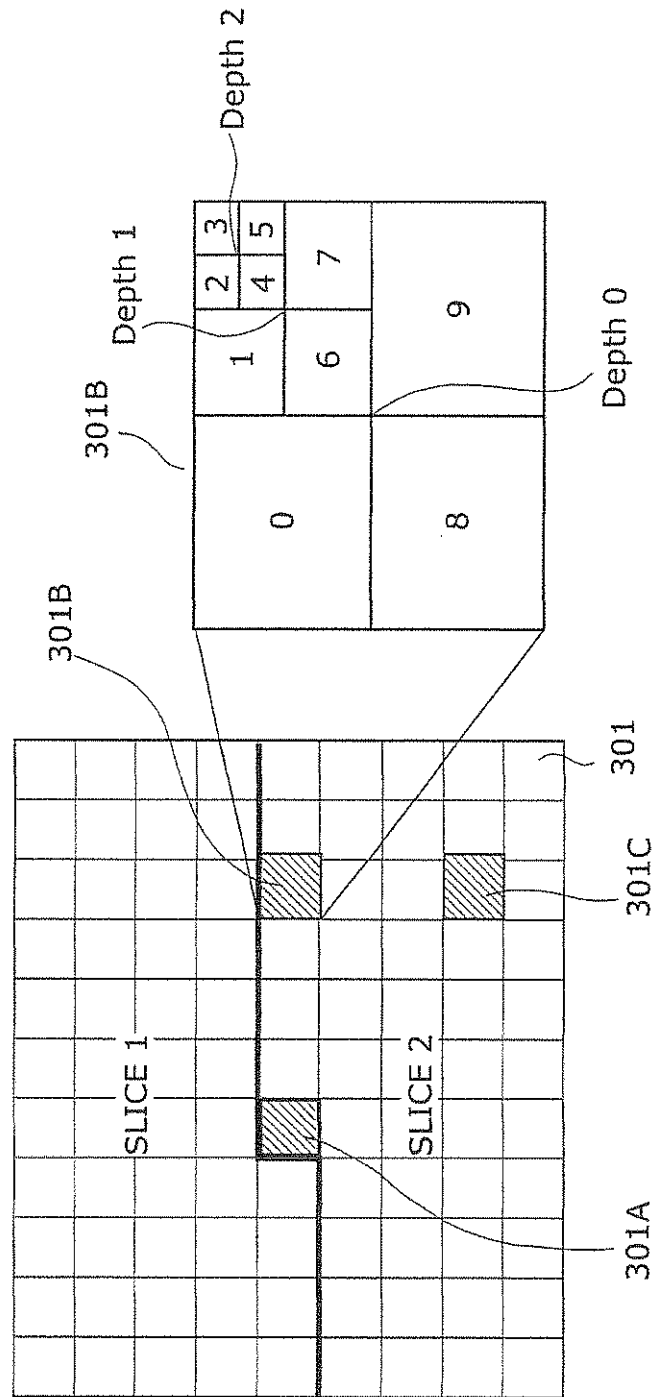


FIG. 10

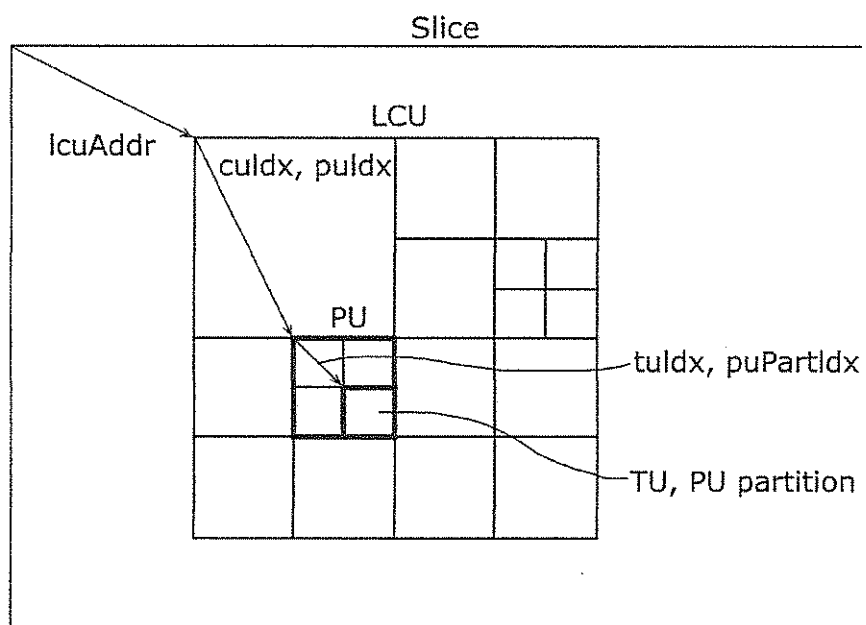


FIG. 11

Verification pattern	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1			0, 1, or 2 (condL && availableL) + (condA && availableA)	cuDepth[xL][yL] > cuDepth[xP][yP]	cuDepth[xA][yA] > cuDepth[xP][yP]
Pattern 2	split_coding_unit_flag	Fixed length	0 or 1 (condL && availableL)	cuDepth[xL][yL] > cuDepth[xP][yP]	Fixed (not held in memory)
Pattern 3			Fixed to 0	Fixed	Fixed (not held in memory)

FIG. 12A

Pattern 2: using only left block (split_coding_unit_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.02	-0.07	0.04	0.09	0.56	-0.12	0.15	0.33	0.28	0.16	0.17	-0.13
Class B	0.02	0.04	0.03	0.06	0.08	0.18	0.16	0.22	0.08	0.25	0.23	0.69
Class C	0.03	0.09	0.06	0.18	0.16	0.20	0.06	0.35	0.87	0.12	-0.21	0.85
Class D	0.05	-0.05	0.06	0.32	0.39	0.18	0.36	0.79	-0.89	0.38	0.90	-0.72
Class E	0.13	-0.02	0.01									
All	0.05	0.01	0.03	0.17	0.18	0.18	0.17	0.40	0.16	0.21	0.22	0.21
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			102 %			103 %		

FIG. 12B

Pattern 3: using neither left block nor upper block (split_coding_unit_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.05	-0.05	0.01	0.15	0.56	-0.27	0.32	0.20	0.53	0.36	0.27	0.54
Class B	0.11	-0.01	0.04	0.23	0.16	0.49	0.32	0.20	0.35	0.22	0.05	0.52
Class C	0.04	0.09	0.13	0.18	0.46	0.23	0.25	0.57	0.65	0.26	0.41	0.46
Class D	0.07	-0.05	0.02	0.29	-0.13	-0.05	0.65	0.44	-0.65	0.61	1.03	-0.06
Class E	0.20	-0.13	-0.33									
All	0.10	-0.01	-0.01	0.24	0.17	0.22	0.36	0.34	0.29	0.35	0.39	0.41
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 13

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	skip_flag	Fixed length	0, 1, 2	skip_flag[xL][yL]	skip_flag[xA][yA]
Pattern 2			0 or 1	skip_flag[xL][yL]	Fixed
Pattern 3			Fixed to 0	Fixed	Fixed

FIG. 14A

Pattern 2: using only left block (skip_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.05	-0.23	-0.01	0.12	0.21	0.23	0.07	-0.03	-0.04
Class B	0.00	0.00	0.00	0.11	0.03	0.02	0.08	0.24	0.11	0.11	0.19	0.44
Class C	0.00	0.00	0.00	0.06	0.16	0.10	0.09	0.39	0.07	0.26	-0.09	0.37
Class D	0.00	0.00	0.00	0.11	-0.11	-0.10	0.03	0.13	-0.33	0.28	0.32	0.16
Class E	0.00	0.00	0.00									
All	0.00	0.00	0.00	0.09	-0.02	-0.02	0.08	0.25	0.05	0.17	0.07	0.22
Enc Time [%]	1.00			0.99			0.99			0.99		
Dec Time [%]												
	101 %			103 %			102 %			103 %		

FIG. 14B

Pattern 3: using neither left block nor upper block (skip_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.11	0.11	-0.04	0.20	0.45	0.15	0.17	0.32	0.36
Class B	0.00	0.00	0.00	0.21	0.06	0.14	-0.01	0.06	0.12	0.15	0.03	0.18
Class C	0.00	0.00	0.00	0.04	0.20	-0.17	0.26	0.20	0.26	0.16	-0.32	-0.18
Class D	0.00	0.00	0.00	0.15	-0.31	-0.08	0.22	-0.05	-0.20	0.31	0.31	-0.07
Class E	0.00	0.00	0.00									
All	0.00	0.00	0.00	0.14	-0.00	-0.02	0.17	0.20	0.11	0.19	0.09	0.10
Enc Time [%]	1.00			0.99			0.99			0.99		
Dec Time [%]												
	101 %			103 %			102 %			103 %		

FIG. 15

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	merge_flag	Fixed length	0, 1, 2	merge_flag[xL][yL]	merge_flag[xA][yA]
Pattern 2			0 or 1	merge_flag[xL][yL]	Fixed
Pattern 3			Fixed to 0	Fixed	Fixed

FIG. 16A

Pattern 2: using only left block (merge_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.00	-0.00	0.09	-0.06	0.22	0.16	-0.03	0.07	0.12
Class B	0.00	0.00	0.00	-0.03	-0.08	0.11	-0.09	0.06	0.15	0.05	0.09	0.23
Class C	0.00	0.00	0.00	-0.04	0.19	0.06	-0.01	-0.02	0.04	-0.00	-0.20	0.33
Class D	0.00	0.00	0.00	-0.01	-0.47	-0.26	0.07	0.04	-0.40	0.06	0.05	-0.51
Class E	0.00	0.00	0.00	-0.02	-0.11	-0.03	-0.03	0.09	0.02	0.01	0.00	0.08
All	0.00	0.00	0.00	-0.02	-0.11	-0.03	-0.03	0.09	0.02	0.01	0.00	0.08
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			102 %			103 %		

FIG. 16B

Pattern 3: using neither left block nor upper block (merge_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.03	0.16	0.06	-0.03	0.19	0.05	-0.04	0.37	0.34
Class B	0.00	0.00	0.00	0.02	0.06	0.27	-0.03	0.21	0.10	0.06	-0.03	0.36
Class C	0.00	0.00	0.00	-0.01	0.19	0.11	0.02	-0.09	0.01	-0.02	-0.57	-0.09
Class D	0.00	0.00	0.00	0.02	-0.04	-0.33	-0.02	0.18	-0.41	0.05	0.29	-0.34
Class E	0.00	0.00	0.00	0.01	0.05	0.04	-0.02	0.12	-0.03	0.01	0.02	0.11
All	0.00	0.00	0.00	0.01	0.05	0.04	-0.02	0.12	-0.03	0.01	0.02	0.11
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 17

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	ref_idx_lc	Variable length	0, 1, 2, or 3 00: condAfalse condLfalse 01: condAfalse condLtrue 10: condAtrue condLfalse 11: condAtrue condLtrue	ref_idx_lc[xL][yL] > 0	ref_idx_lc[xA][yA] > 0
	ref_idx_l0			ref_idx_l0[xL][yL] > 0	ref_idx_l0[xA][yA] > 0
	ref_idx_l1			ref_idx_l1[xL][yL] > 0	ref_idx_l1[xA][yA] > 0
Pattern 2	ref_idx_lc		fixed_0: condLfalse fixed_1: condLtrue	ref_idx_lc[xL][yL] > 0	Fixed
	ref_idx_l0			ref_idx_l0[xL][yL] > 0	
	ref_idx_l1			ref_idx_l1[xL][yL] > 0	
Pattern 3	ref_idx_lc ref_idx_l0 ref_idx_l1		Fixed	Fixed	Fixed

FIG. 18A

Pattern 2: using only left block (ref_idx)

ref_idx	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	-0.01	-0.09	-0.14	-0.07	0.16	0.14	-0.05	0.11	0.20
Class B	0.00	0.00	0.00	-0.01	-0.06	-0.07	0.01	0.03	0.08	-0.05	-0.21	0.06
Class C	0.00	0.00	0.00	0.04	0.11	-0.10	-0.04	0.41	0.18	-0.07	-0.62	-0.41
Class D	0.00	0.00	0.00	0.13	-0.25	-0.09	0.09	0.09	-0.47	-0.04	-0.08	-0.11
Class E	0.00	0.00	0.00	0.04	-0.07	-0.07	-0.01	0.18	0.02	-0.05	-0.19	-0.05
All	0.00	0.00	0.00	0.04	-0.07	-0.07	-0.01	0.18	0.02	-0.05	-0.19	-0.05
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 18B

Pattern 3: using neither left block nor upper block (ref_idx)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.02	0.23	-0.02	-0.03	0.11	-0.00	-0.03	0.05	0.14
Class B	0.00	0.00	0.00	-0.02	0.06	0.01	-0.03	0.02	0.12	0.05	0.01	0.07
Class C	0.00	0.00	0.00	-0.04	0.04	0.13	-0.09	0.39	-0.06	0.01	-0.22	0.10
Class D	0.00	0.00	0.00	0.04	-0.60	-0.24	0.06	-0.15	-0.55	0.02	0.19	-0.53
Class E	0.00	0.00	0.00	-0.01	-0.14	-0.02	-0.02	0.11	-0.09	0.01	-0.00	-0.01
All	0.00	0.00	0.00	-0.01	-0.14	-0.02	-0.02	0.11	-0.09	0.01	-0.00	-0.01
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 18C

Signal type (syntax element)	Context model	Left block condition L condL	Upper block condition A condA
ref_idx_lc	(condL && availableL) + (condA && availableA) < < 1	ref_idx_lc[xL][yL] > 0	ref_idx_lc[xA][yA] > 0
ref_idx_l0	(condL && availableL) + (condA && availableA) < < 1	ref_idx_l0[xL][yL] > 0	ref_idx_l0[xA][yA] > 0
ref_idx_l1	(condL && availableL) + (condA && availableA) < < 1	ref_idx_l1[xL][yL] > 0	ref_idx_l1[xA][yA] > 0

FIG. 18D

Signal type (syntax element)	Context model	Left block condition L condL	Upper block condition A condA
ref_idx_lc	Derived from l0 and l1	Derived from l0 and l1	Derived from l0 and l1
ref_idx_l0	(condL && availableL) + (condA && availableA) < < 1	ref_idx_l0[xL][yL] > 0	ref_idx_l0[xA][yA] > 0
ref_idx_l1	(condL && availableL) + (condA && availableA) < < 1	ref_idx_l1[xL][yL] > 0	ref_idx_l1[xA][yA] > 0

FIG. 19

Verification pattern	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	inter_pred_flag	Fixed length	0, 1, or 2	inter_pred_flag[xL][yL]	inter_pred_flag[xA][yA]
Pattern 2			(condL && availableL) + (condA && availableA)		
Pattern 3			(condL && availableL)	inter_pred_flag[xL][yL]	Fixed
			Fixed	Fixed	Fixed

FIG. 20A

Pattern 2: using only left block (inter_pred_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.01	-0.07	-0.06						
Class B	0.00	0.00	0.00	0.02	0.03	-0.02	0.00	0.06	-0.06	0.00	0.00	0.00
Class C	0.00	0.00	0.00	-0.02	-0.02	0.02	-0.02	0.03	0.22	0.00	0.00	0.00
Class D	0.00	0.00	0.00	0.08	-0.06	-0.12	-0.01	0.18	-0.01	0.00	0.00	0.00
Class E	0.00	0.00	0.00				0.02	-0.28	-0.75	0.00	0.00	0.00
All	0.00	0.00	0.00	0.03	-0.04	-0.04	-0.00	0.02	-0.11	0.00	0.00	0.00
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 20B

Pattern 3: using neither left block nor upper block (inter_pred_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.01	-0.14	-0.14						
Class B	0.00	0.00	0.00	-0.02	-0.12	0.01	-0.02	0.18	-0.16	0.00	0.00	0.00
Class C	0.00	0.00	0.00	-0.00	0.08	0.34	-0.04	-0.10	-0.09	0.00	0.00	0.00
Class D	0.00	0.00	0.00	0.00	-0.22	-0.12	-0.07	0.30	-0.09	0.00	0.00	0.00
Class E	0.00	0.00	0.00				0.05	0.57	-0.51	0.00	0.00	0.00
All	0.00	0.00	0.00	-0.01	-0.10	0.06	-0.02	0.21	-0.19	0.00	0.00	0.00
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 21

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	mvd_lc	Variable length	0, 1, or 2 (condL && availableL) + (condA && availableA)	mvd_lc[xL][yL] > 16	mvd_lc[xA][yA] > 16
	mvd_l0			mvd_l0[xL][yL] > 16	mvd_l0[xA][yA] > 16
	mvd_l1			mvd_l1[xL][yL] > 16	mvd_l1[xA][yA] > 16
Pattern 2	mvd_lc		(condL && availableL)	mvd_lc[xL][yL] > 16	Fixed
	mvd_l0			mvd_l0[xL][yL] > 16	
	mvd_l1			mvd_l1[xL][yL] > 16	
Pattern 3	mvd_lc		Fixed	Fixed	Fixed
	mvd_l0				
	mvd_l1				

FIG. 22A

Pattern 2: using only left block (mvd)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.02	0.20	-0.06						
Class B	0.00	0.00	0.00	-0.01	-0.09	-0.13	0.01	0.19	0.11	-0.04	0.21	0.19
Class C	0.00	0.00	0.00	0.01	0.00	-0.14	-0.06	-0.03	0.05	-0.01	0.04	0.20
Class D	0.00	0.00	0.00	0.10	-0.22	0.08	-0.06	-0.02	-0.16	0.02	-0.35	-0.41
Class E	0.00	0.00	0.00				0.13	0.24	-0.39	0.05	0.56	-0.04
All	0.00	0.00	0.00	0.02	-0.11	-0.07	-0.00	0.09	-0.07	0.00	0.09	0.00
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 22B

Pattern 3: using neither left block nor upper block (mvd)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.00	0.13	0.08						
Class B	0.00	0.00	0.00	-0.03	-0.02	-0.11	0.05	0.21	0.14	-0.07	-0.02	0.05
Class C	0.00	0.00	0.00	-0.04	0.25	-0.12	-0.04	-0.20	0.21	0.06	0.00	0.29
Class D	0.00	0.00	0.00	0.01	-0.13	0.15	0.05	-0.01	-0.08	-0.02	-0.22	-0.29
Class E	0.00	0.00	0.00				0.11	-0.00	-0.44	-0.04	-0.17	-0.39
All	0.00	0.00	0.00	-0.02	0.03	-0.04	0.04	0.01	-0.01	-0.02	-0.09	-0.06
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 22C

Signal type (syntax element)	Context model	Left block condition L condL	Upper block condition A condA
mvd_lc	(condL && availableL) + (condA && availableA)	mvd_lc[xL][yL] > 16	mvd_lc[xA][yA] > 16
mvd_l0	(condL && availableL) + (condA && availableA)	mvd_l0[xL][yL] > 16	mvd_l0[xA][yA] > 16
mvd_l1	(condL && availableL) + (condA && availableA)	mvd_l1[xL][yL] > 16	mvd_l1[xA][yA] > 16

FIG. 22D

Signal type (syntax element)	Context model	Left block condition L condL	Upper block condition A condA
mvd_lc	Derived from l0 and l1	Derived from l0 and l1	Derived from l0 and l1
mvd_l0	(condL && availableL) + (condA && availableA)	mvd_l0[xL][yL] > 16	mvd_l0[xA][yA] > 16
mvd_l1	(condL && availableL) + (condA && availableA)	mvd_l1[xL][yL] > 16	mvd_l1[xA][yA] > 16

FIG. 23A

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	no_residual_data_flag	Fixed length	0, 1, 2, or 3 00: condAfalse condLfalse 01: condAfalse condLtrue 10: condAtrue condLfalse 11: condAtrue condLtrue	no_residual_data_flag [xL][yL]	no_residual_data_flag [xA][yA]
Pattern 2			fixed_0: condLfalse fixed_1: condLtrue	no_residual_data_flag [xL][yL]	Fixed
Pattern 3			Fixed	Fixed	Fixed

FIG. 23B

Transform tree syntax	
Transform_tree(x0, y0, log2TrafoSize,trafoDepth, blkIdx){	Descriptor
if(entropy_coding_mode_flag && trafoDepth == 0 && IntraSplitFlag == 0)	
{	
if(Predmode != MODE_INTRA)	
no_residual_data_flag	u(1) ae(v)
residualDataPresentFlag = !no_residual_data_flag	

FIG. 24A

Pattern 2: using only left block (no_residual_data_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.01	0.23	-0.07	0.03	0.11	-0.18	-0.04	-0.08	0.09
Class B	0.00	0.00	0.00	-0.01	-0.09	-0.16	0.02	-0.21	-0.04	0.04	0.11	0.10
Class C	0.00	0.00	0.00	-0.06	0.02	-0.06	0.09	0.41	0.05	0.04	-0.42	-0.33
Class D	0.00	0.00	0.00	-0.02	-0.24	-0.23	-0.04	-0.58	-0.42	0.11	-0.03	-0.22
Class E	0.00	0.00	0.00	-0.02	-0.09	-0.13	0.03	-0.02	-0.14	0.03	-0.11	-0.07
All	0.00	0.00	0.00									
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 24B

Pattern 3: using neither left block nor upper block (no_residual_data_flag)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.00	0.00	0.00	0.04	0.12	-0.27	-0.01	0.14	0.29	0.01	0.20	0.20
Class B	0.00	0.00	0.00	0.02	-0.00	-0.00	-0.05	-0.07	0.09	0.09	-0.22	0.36
Class C	0.00	0.00	0.00	-0.01	0.10	0.07	-0.06	0.10	0.06	-0.00	-0.16	-0.35
Class D	0.00	0.00	0.00	0.05	-0.44	-0.28	-0.13	-0.20	-0.80	0.12	0.49	0.12
Class E	0.00	0.00	0.00	0.02	-0.11	-0.08	-0.06	0.01	-0.02	0.05	0.06	0.09
All	0.00	0.00	0.00									
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 25A

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	intra_chroma_pred_mode	Variable length	0, 1, or 2 (condL && availableL) + (condA && availableA)	intraPredMode[xL][yL] == 4	intraPredMode[xA][yA] == 4
Pattern 2			(condL && availableL)	intraPredMode[xL][yL] == 4	Fixed
Pattern 3			Fixed	Fixed	Fixed

FIG. 25B

intra_chroma_pred_mode	intraPredMode[xB][yB]				
	0	1	2	3	X(4 ≤ X < 34)
0	0	1	2	3	X
1	1	0	0	0	0
2	2	2	1	1	1
3	3	3	2	2	2
4	n/a	n/a	n/a	n/a	3

FIG. 26A

Pattern 2: using only left block (intra_chroma_pred_mode)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.02	-0.17	0.00	0.01	0.51	-0.09	0.01	0.15	0.03	-0.03	-0.11	-0.02
Class B	-0.00	0.06	-0.05	-0.01	-0.01	0.20	0.01	-0.07	0.09	0.02	-0.04	0.11
Class C	0.00	-0.02	0.01	-0.01	0.57	-0.19	-0.02	-0.59	-0.63	-0.13	-0.32	-0.81
Class D	0.02	-0.12	-0.19	0.08	-0.04	0.01	-0.12	0.69	-1.13	-0.12	0.72	-0.20
Class E	0.03	-0.12	0.12				-0.12	0.01	-0.34	-0.08	0.01	-0.22
All	0.01	-0.04	-0.04	0.02	0.16	0.04	-0.06	99 %			99 %	
Enc Time [%]	100 %			99 %			103 %			103 %		
Dec Time [%]	101 %			103 %								

FIG. 26B

Pattern 3: using neither left block nor upper block (intra_chroma_pred_mode)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.03	0.05	-0.05	-0.03	0.85	-0.99	0.00	-0.22	0.49	-0.02	-0.19	0.69
Class B	-0.00	0.00	-0.03	-0.06	0.14	0.08	0.01	0.25	0.42	0.00	0.11	0.67
Class C	0.01	0.09	0.06	-0.11	0.38	0.12	0.08	0.46	-0.70	-0.04	-0.33	-0.39
Class D	-0.02	0.01	-0.15	0.04	-0.18	0.44	-0.11	-0.17	-0.81	-0.09	-0.04	-1.49
Class E	-0.00	-0.10	0.26				0.00	0.08	-0.26	-0.03	-0.12	0.01
All	-0.00	0.02	0.02	-0.04	0.10	0.15		99 %			99 %	
Enc Time [%]	100 %			99 %			103 %			104 %		
Dec Time [%]	101 %			103 %								

FIG. 27

Verification number	Signal type (syntax element)	Binarization scheme	Context index increment of binary sequence element (binIdx = 0)	c5 Left block condition L condL	c6 Upper block condition A condA
Pattern 1	Cbf_cb(MODE_INTRA)	Fixed length	0, 1, 2, or 3 00: condAfalse condLfalse 01: condAfalse condLtrue 10: condAtrue condLfalse 11: condAtrue condLtrue	Cbf_cb[xL][yL]	Cbf_cb[xA][yA]
	Cbf_cr(MODE_INTRA)			Cbf_cr[xL][yL]	Cbf_cr[xA][yA]
	Cbf_luma			Cbf_luma[xL][yL]	Cbf_luma[xA][yA]
Pattern 2	Cbf_cb(MODE_INTRA)		fixed_0: condLfalse fixed_1: condLtrue	Cbf_cb[xL][yL]	Fixed
	Cbf_cr(MODE_INTRA)			Cbf_cr[xL][yL]	
	Cbf_luma			Cbf_luma[xL][yL]	
Pattern 3	Cbf_cb(MODE_INTRA)	Fixed		Fixed	Fixed
	Cbf_cr(MODE_INTRA)				
	Cbf_luma				

FIG. 28A

Pattern 2: using only left block (cbf_luma, cbf_cr, cbf_cb)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.01	0.05	0.02	-0.01	0.45	-0.26	-0.06	0.16	0.18	-0.08	0.26	0.47
Class B	0.02	0.05	0.10	-0.03	-0.05	0.08	-0.07	-0.02	-0.15	0.00	0.06	0.31
Class C	0.02	0.12	0.06	-0.11	0.39	-0.03	-0.01	0.58	-0.13	0.03	0.19	-0.43
Class D	0.02	-0.03	0.06	0.14	-0.52	0.04	-0.04	-0.52	-1.42	0.00	-0.12	-1.21
Class E	0.03	0.13	0.18	-0.00	-0.05	0.01	-0.04	0.09	-0.28	-0.02	0.12	-0.11
All	0.02	0.06	0.08									
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 28B

Pattern 3: using neither left block nor upper block (cbf_luma, cbf_cr, cbf_cb)

	Intra			Random access			Low delay			Low delay (P)		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.04	0.06	0.15	-0.04	0.37	-0.13	0.06	0.46	0.20	0.04	0.38	0.32
Class B	0.07	0.10	0.15	-0.00	0.23	-0.06	-0.06	0.23	0.35	0.06	0.24	0.53
Class C	0.03	0.13	0.20	-0.09	0.59	0.53	-0.09	0.90	-0.79	0.03	0.17	-0.77
Class D	-0.00	0.07	0.19	0.12	0.16	0.19	0.02	-0.13	-1.29	0.05	-0.45	-0.42
Class E	0.12	0.14	0.26				-0.02	0.40	-0.29	0.04	0.14	-0.04
All	0.05	0.10	0.19	0.01	0.30	0.15						
Enc Time [%]	100 %			99 %			99 %			99 %		
Dec Time [%]	101 %			103 %			103 %			103 %		

FIG. 29A

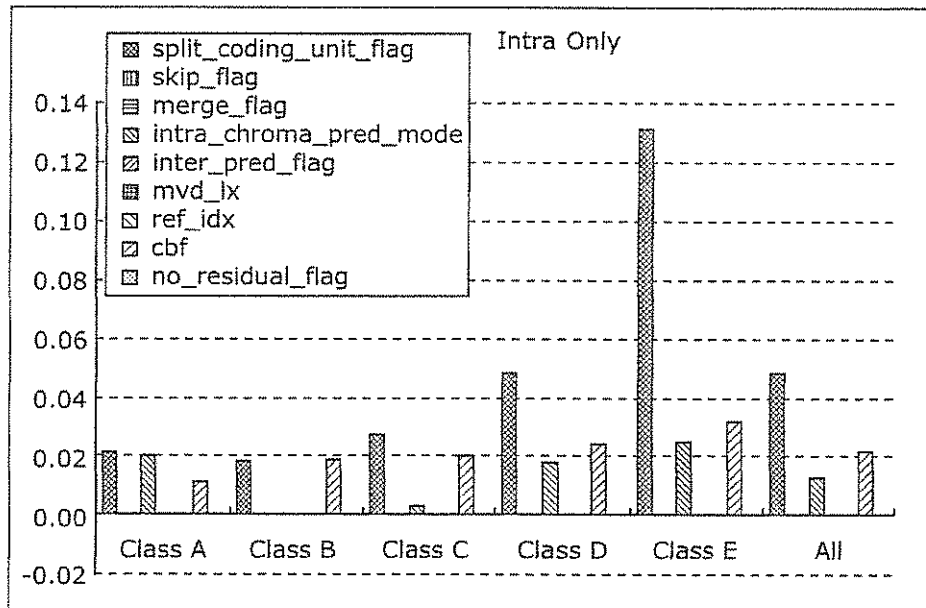


FIG. 29B

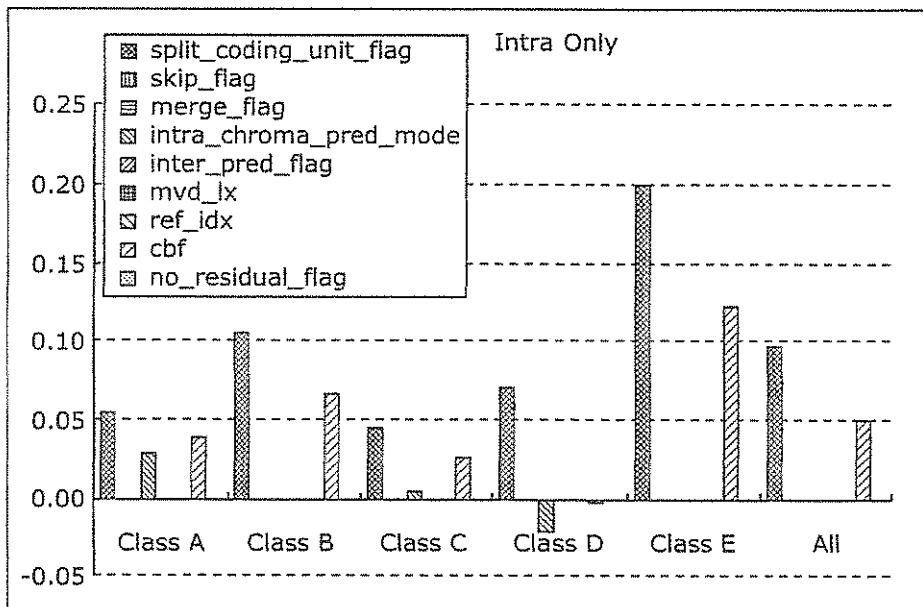


FIG. 30A

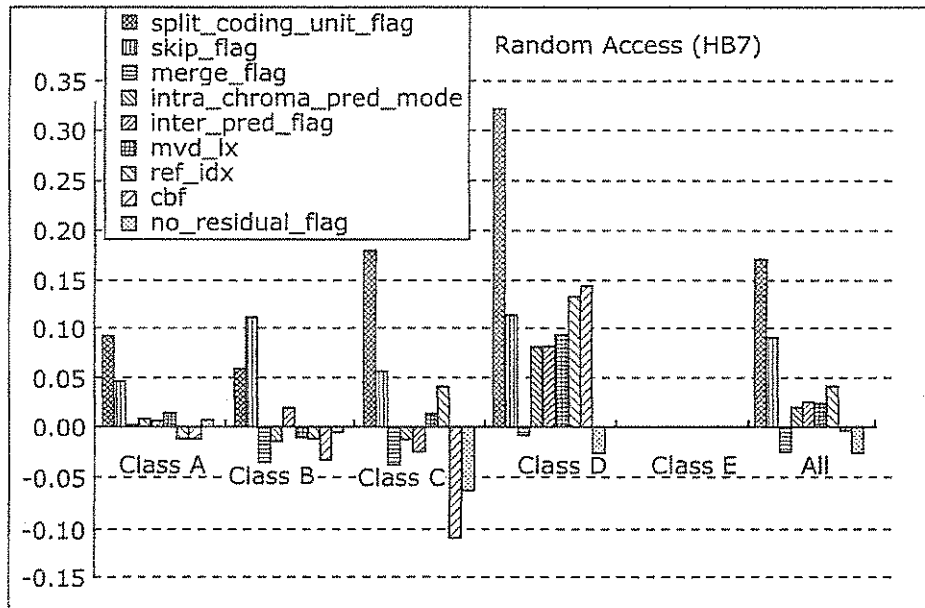


FIG. 30B

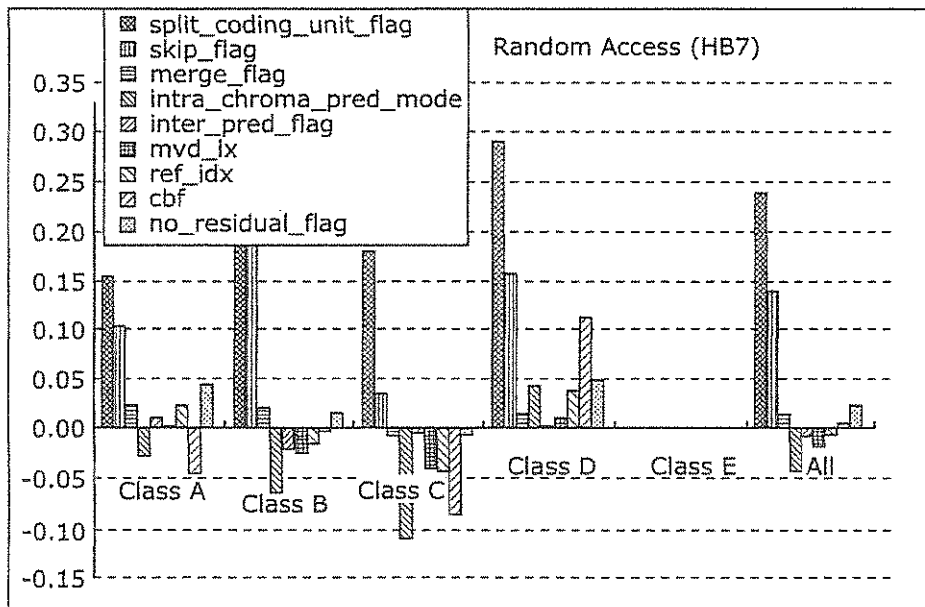


FIG. 31A

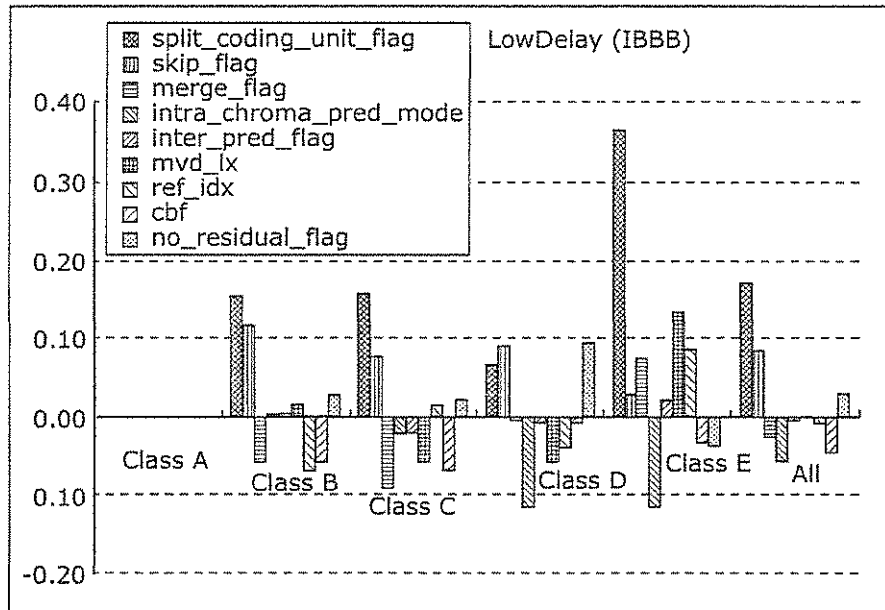


FIG. 31B

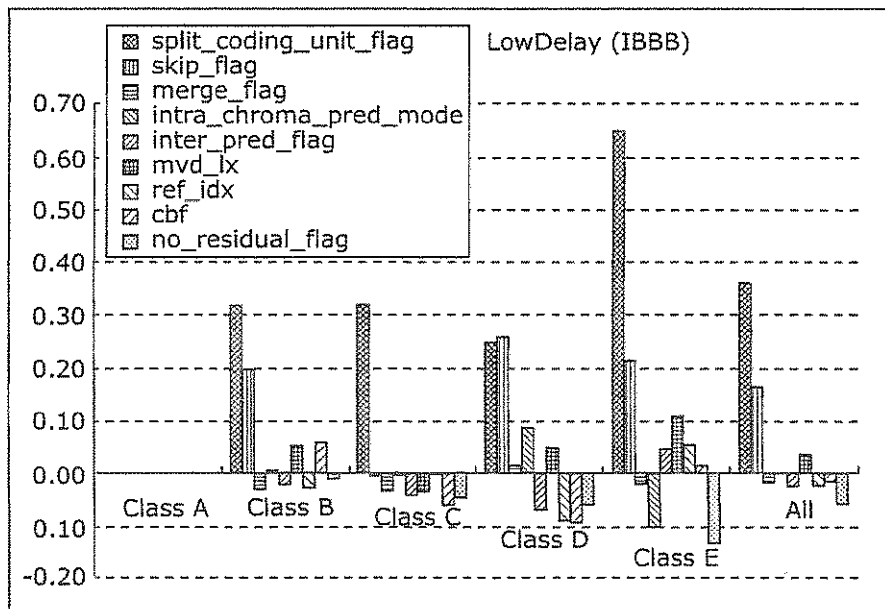


FIG. 32A

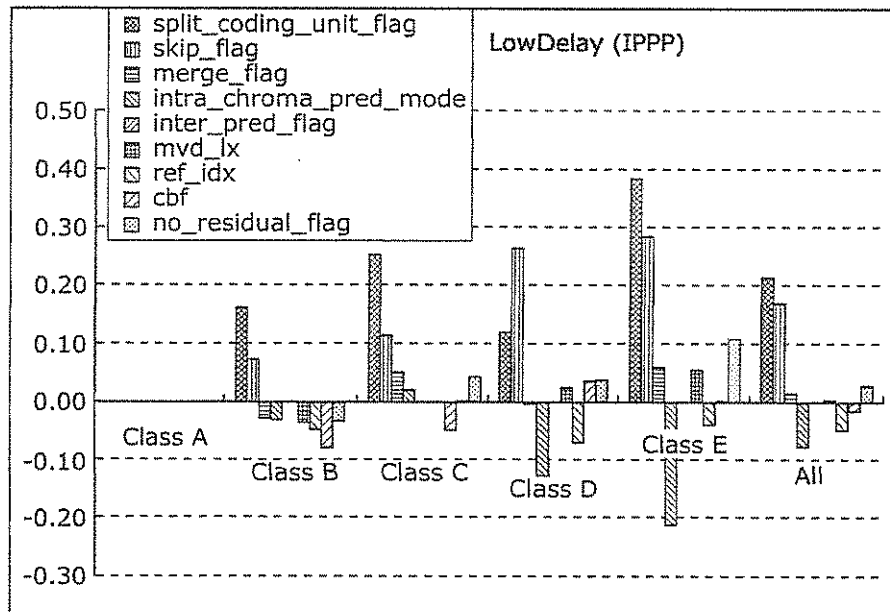


FIG. 32B

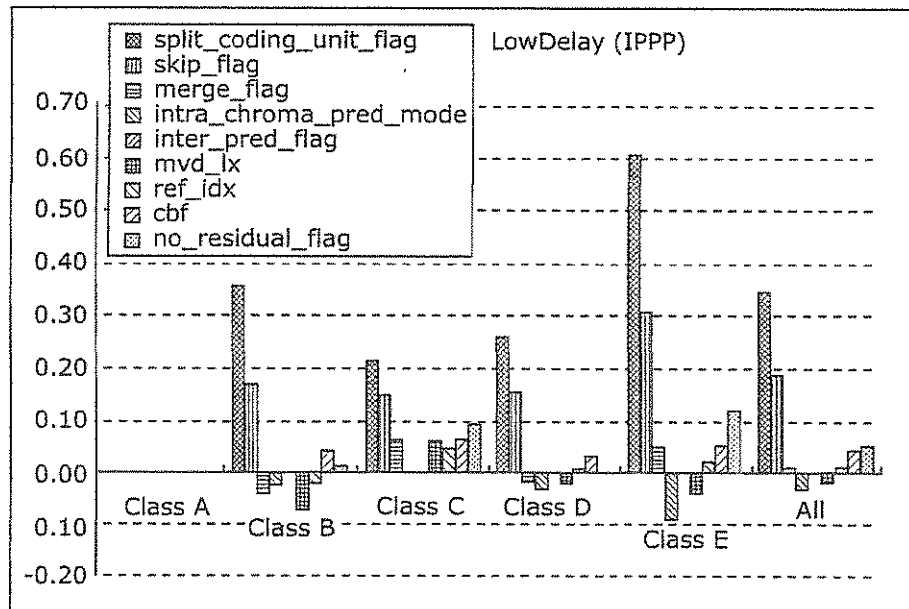


FIG. 33A

Param	Above	Left
skip	Yes	Yes
split	Yes	Yes
merge	No	No
intra-chroma	No	No
inter_pred	No	No
ref_idx	No	No
mvd	No	No
noRes	No	No
cbf	No	No

FIG. 33B

	Intra		Random access		Low delay IBPP		Low delay IPPP	
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate
Class A	0.06	0.18	0.22	-0.01	0.36	0.69		
Class B	0.08	0.14	0.21	0.05	0.29	0.33	0.01	1.05
Class C	0.04	0.18	0.25	-0.02	0.34	0.17	-0.11	0.49
Class D	0.02	0.35	0.34	0.00	-0.03	0.02	-0.05	0.56
Class E	0.06	0.40	0.39				0.06	2.11
All	0.05	0.24	0.27	0.01	0.24	0.30	-0.03	0.99
Enc Time[%]	100%		100%		100%		100%	
Dec Time[%]	99%		99%		99%		98%	

FIG. 34A

Param	Above	Left
skip	Yes	Yes
split	Yes	Yes
merge	No	No
intra-chroma	No	Yes
inter_pred	No	No
ref_idx	No	No
mvd	No	No
noRes	No	No
cbf	No	Yes

FIG. 34B

	Intra			Random access			Low delay IBPP			Low delay IPPP		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.02	-0.02	0.14	-0.04	0.52	-0.01						
Class B	0.03	0.15	0.1	-0.03	0.06	-0.18	0.01	0.3	0.4	0.08	0.39	0.64
Class C	0.03	0.13	0.08	-0.02	0.32	-0.05	-0.07	0.64	0.36	0.04	0.62	0.5
Class D	0.04	0.03	0.15	0.06	-0.27	-0.49	-0.11	0.89	-0.57	0.05	0.71	-0.68
Class E	0.07	0.16	0.22				0	1.62	-1.45	0.28	1.96	-1.06
All	0.04	0.09	0.13	-0.01	0.15	-0.18	-0.04	0.78	-0.2	0.1	0.82	-0.05
Enc Time[%]	103%			103%			103%			100%		
Dec Time[%]	100%			101%			102%			100%		

FIG. 35

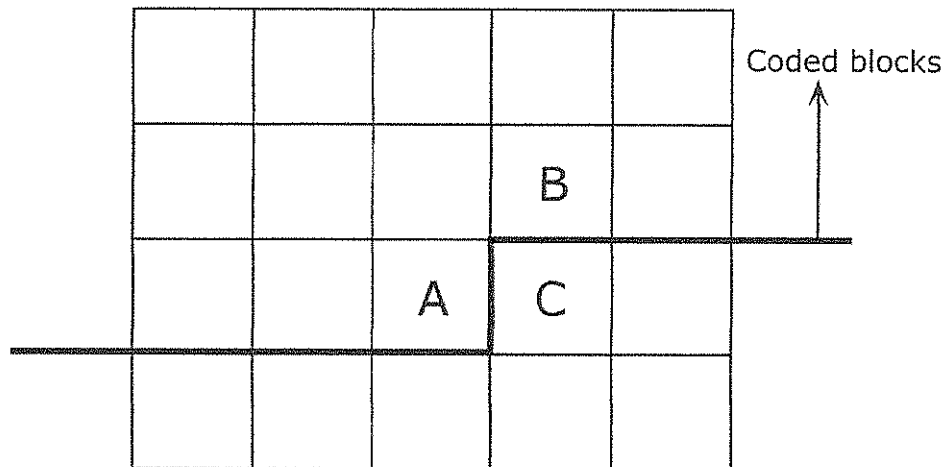


FIG. 36

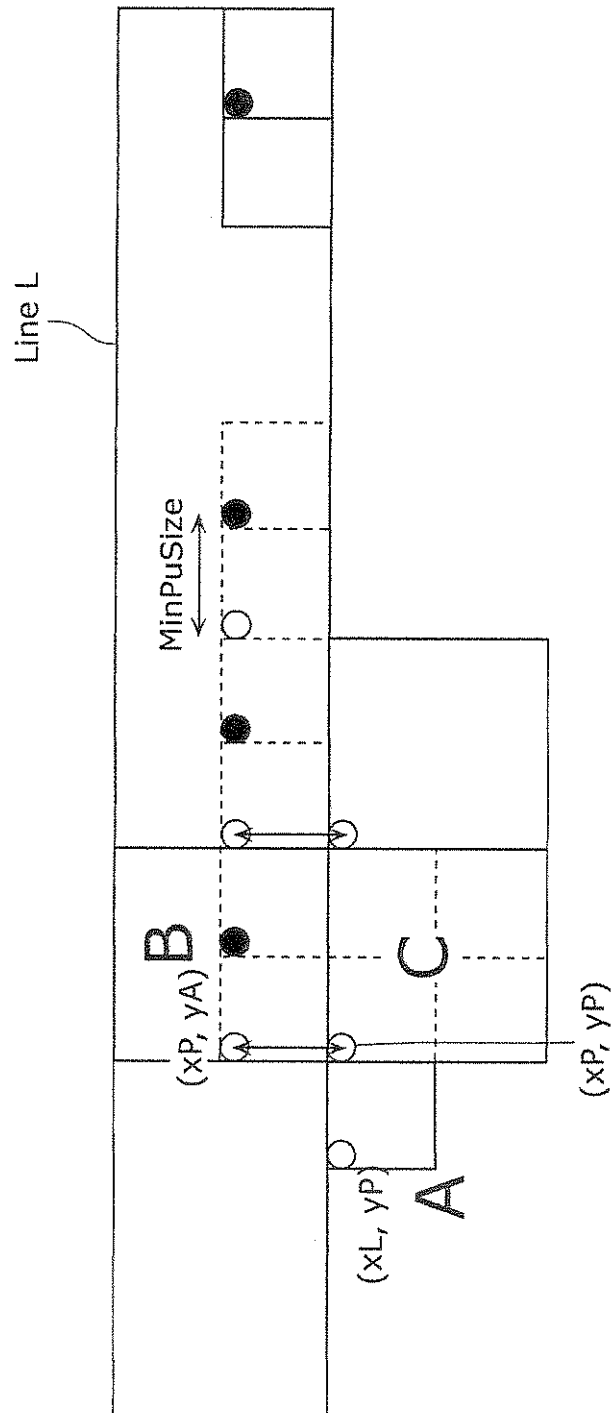


FIG. 37

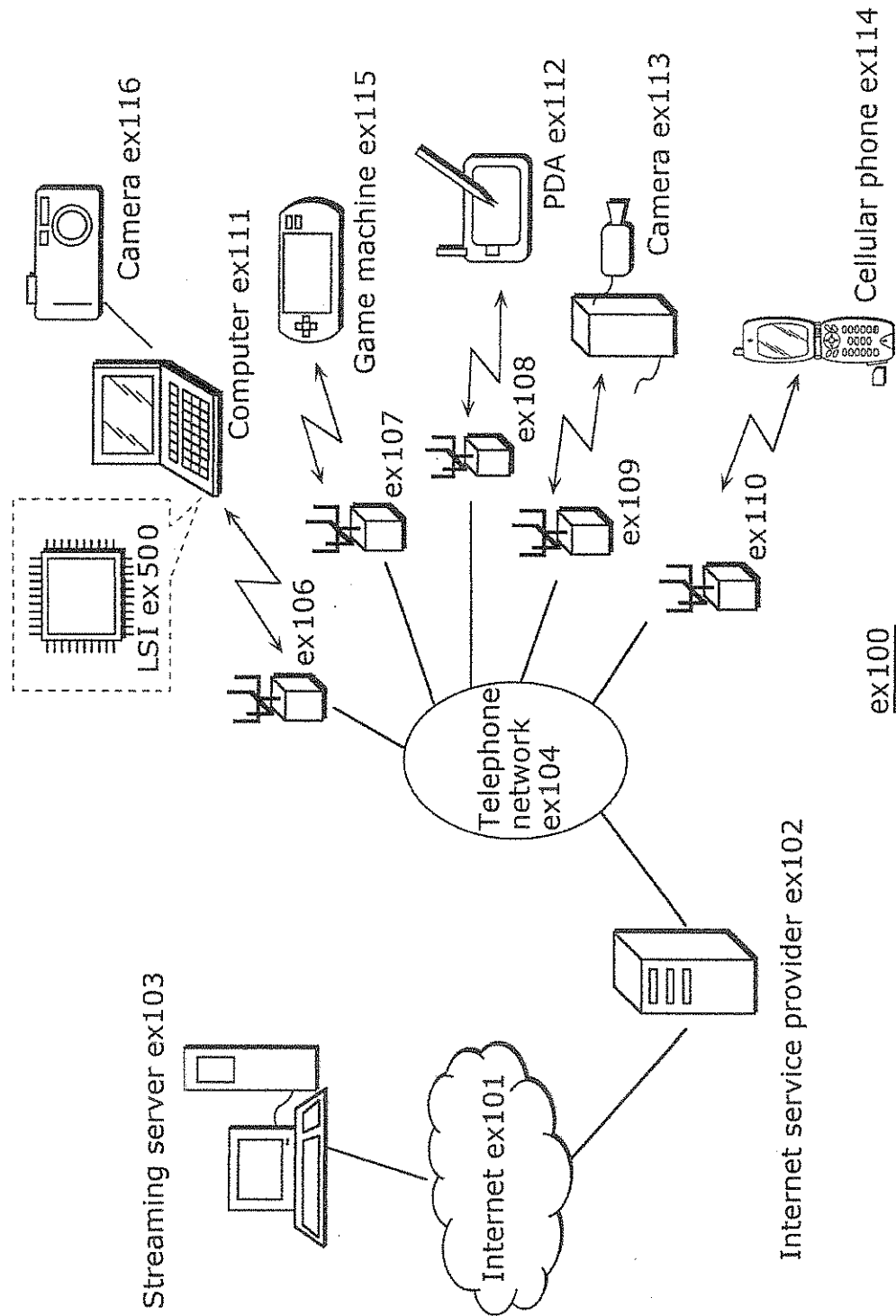


FIG. 38

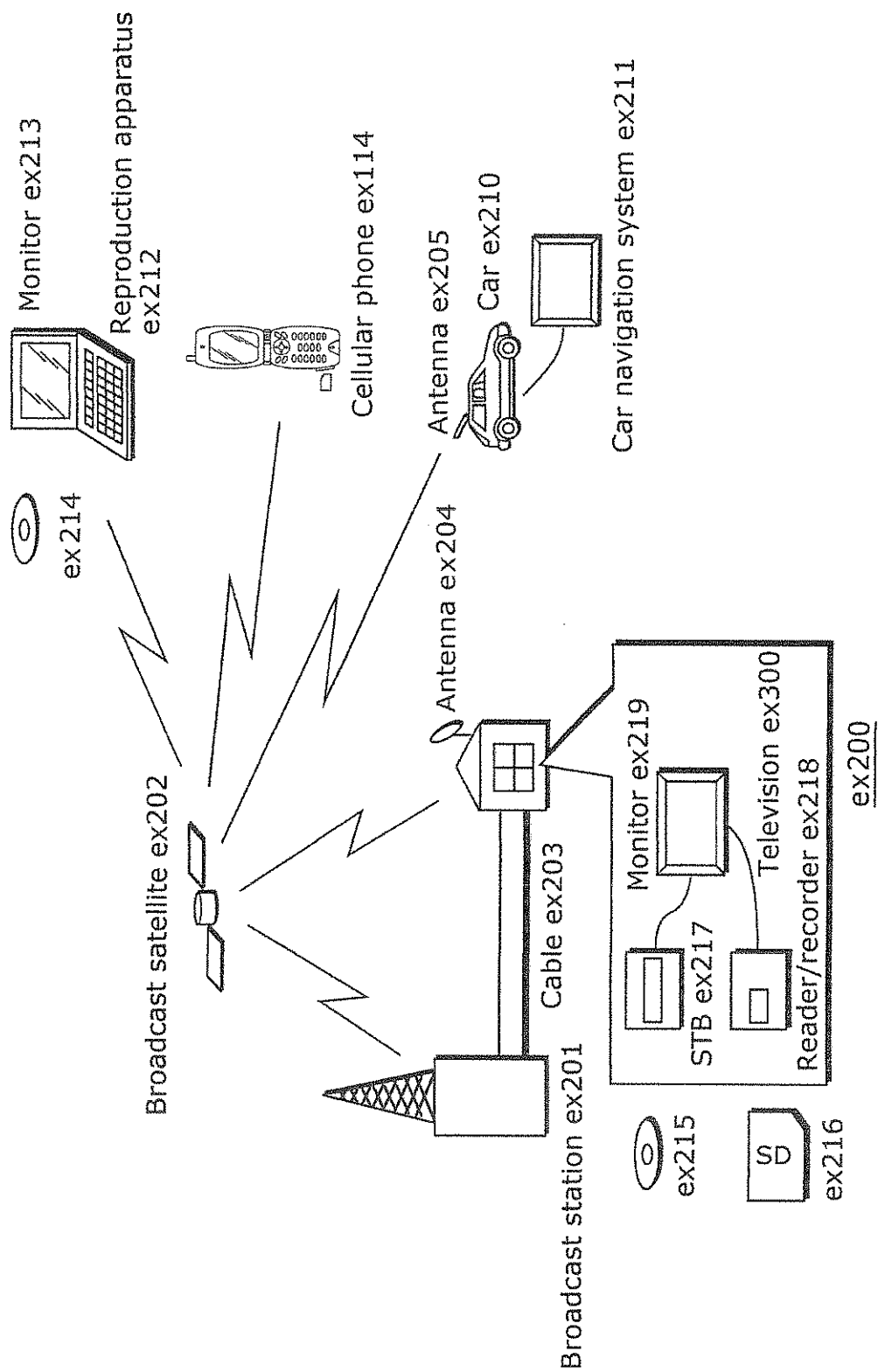


FIG. 39

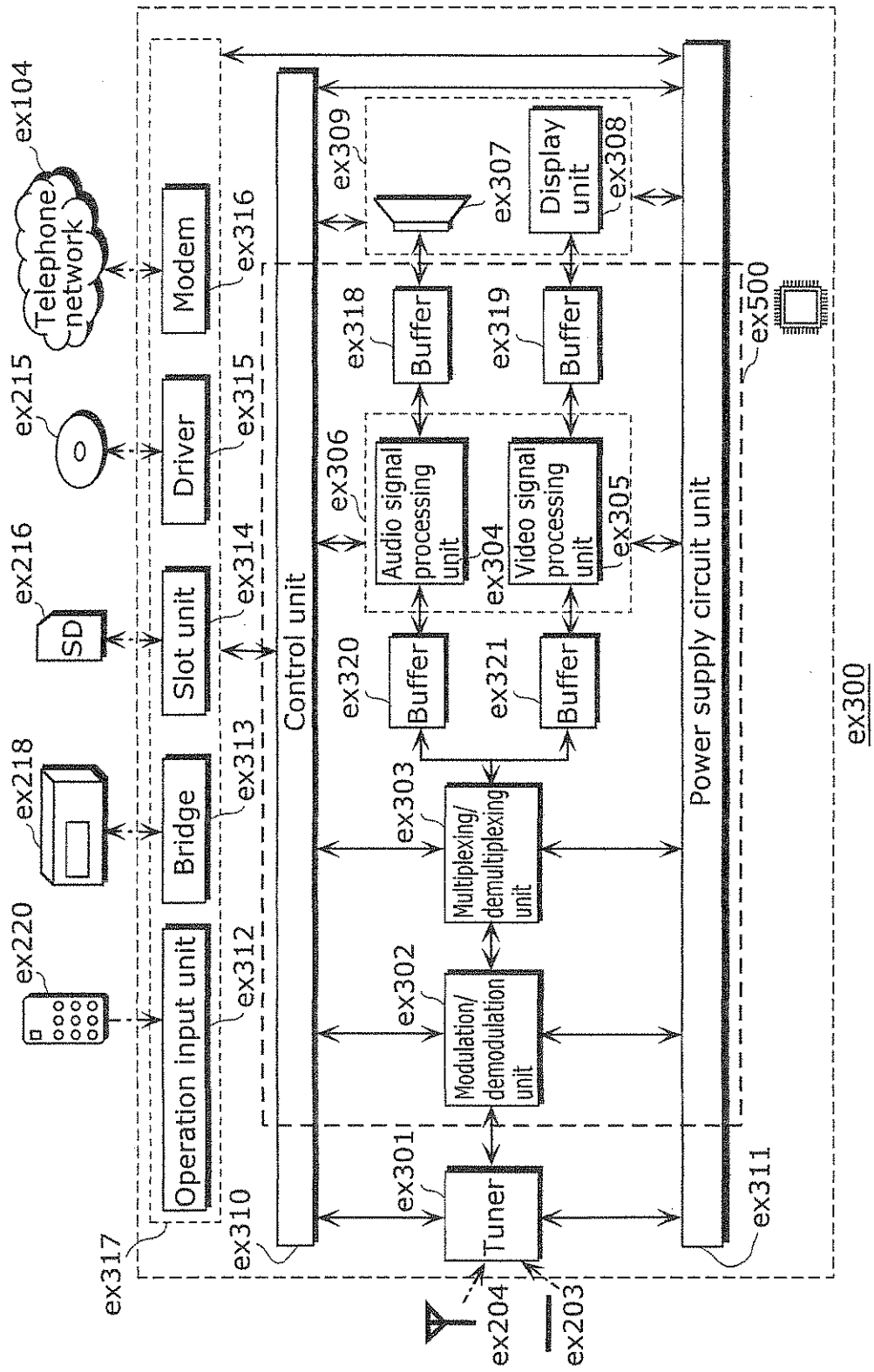
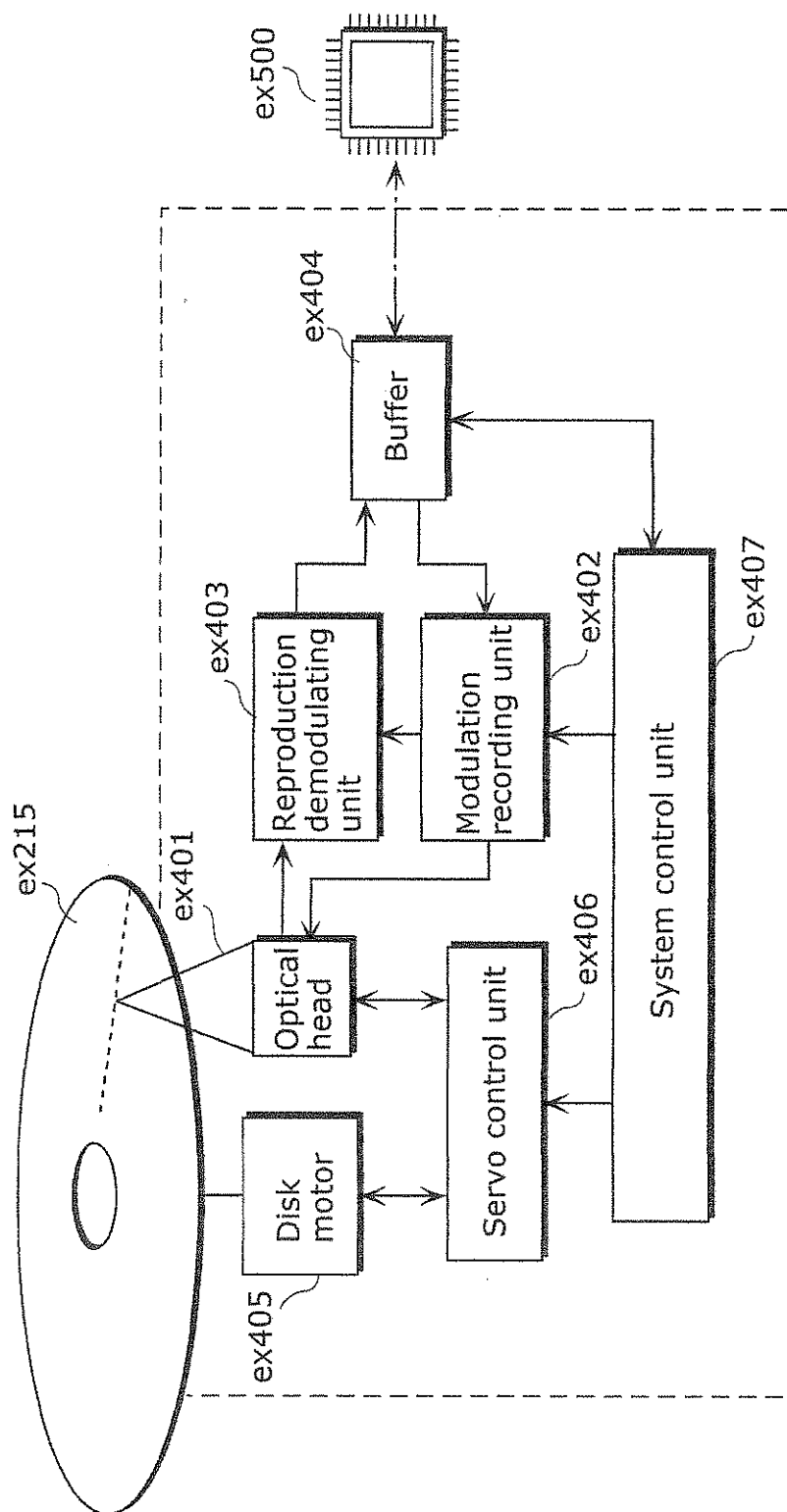


FIG. 40



ex400

FIG. 41

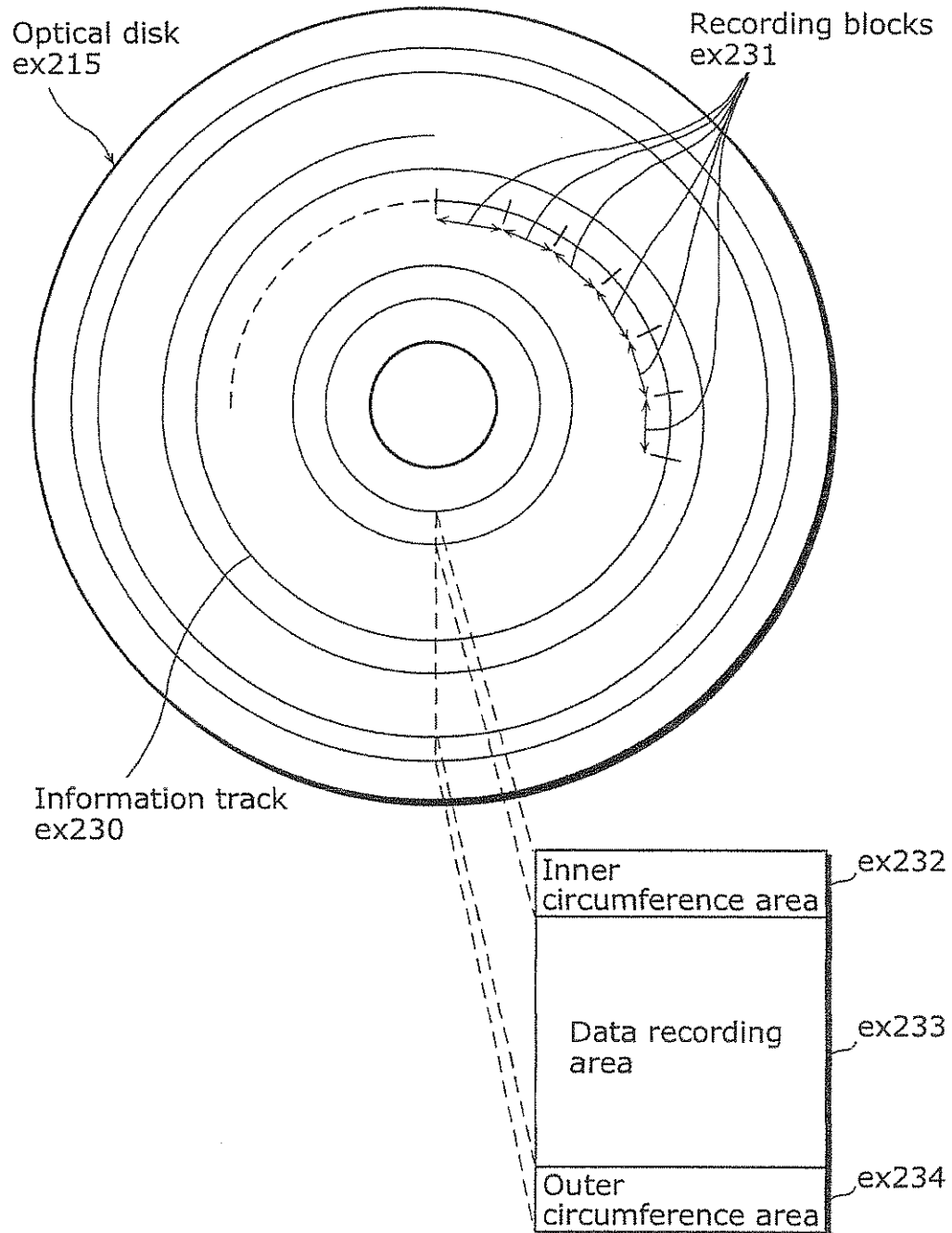


FIG. 42A

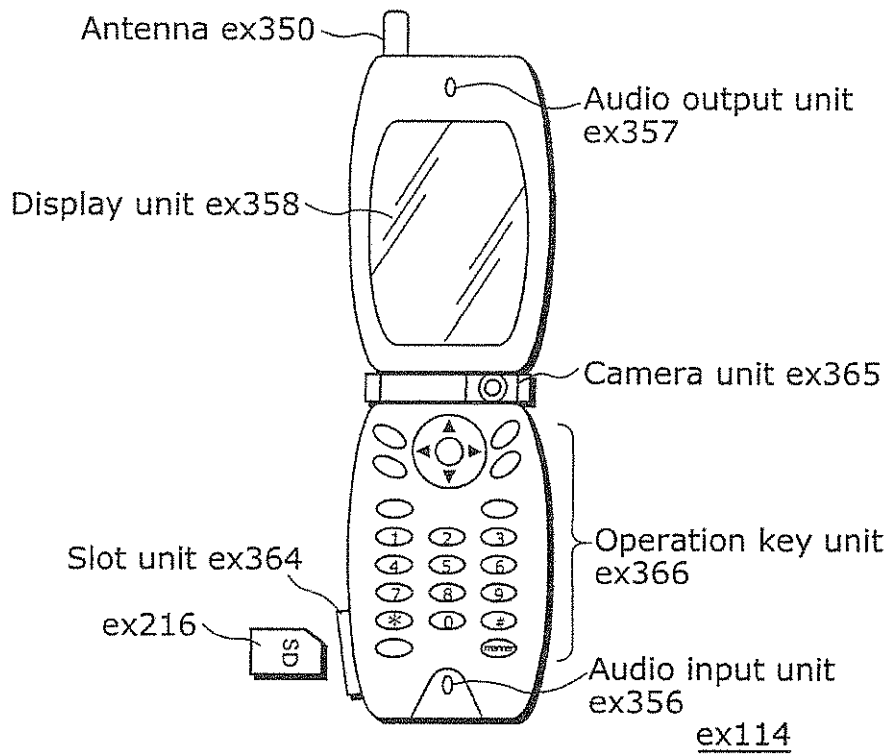


FIG. 42B

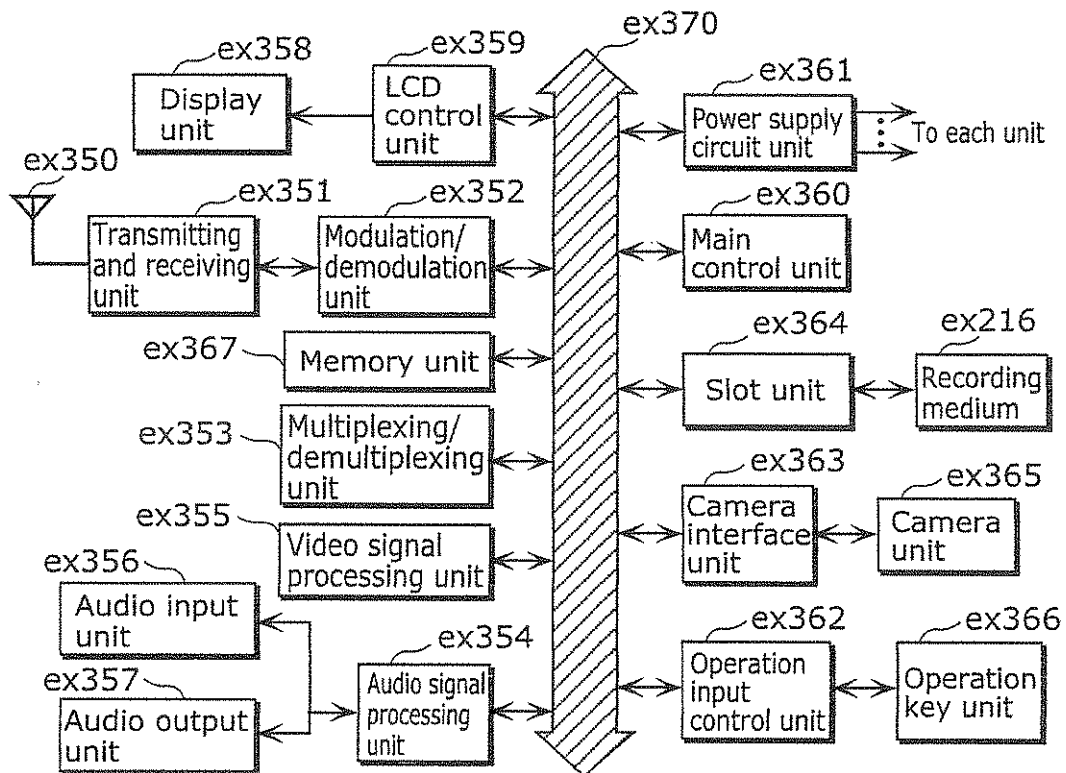


FIG. 43

Video stream (PID=0x1011, Primary video)
Audio stream (PID=0x1100)
Audio stream (PID=0x1101)
Presentation graphics stream (PID=0x1200)
Presentation graphics stream (PID=0x1201)
Interactive graphics stream (PID=0x1400)
Video stream (PID=0x1B00, Secondary video)
Video stream (PID=0x1B01, Secondary video)

FIG. 44

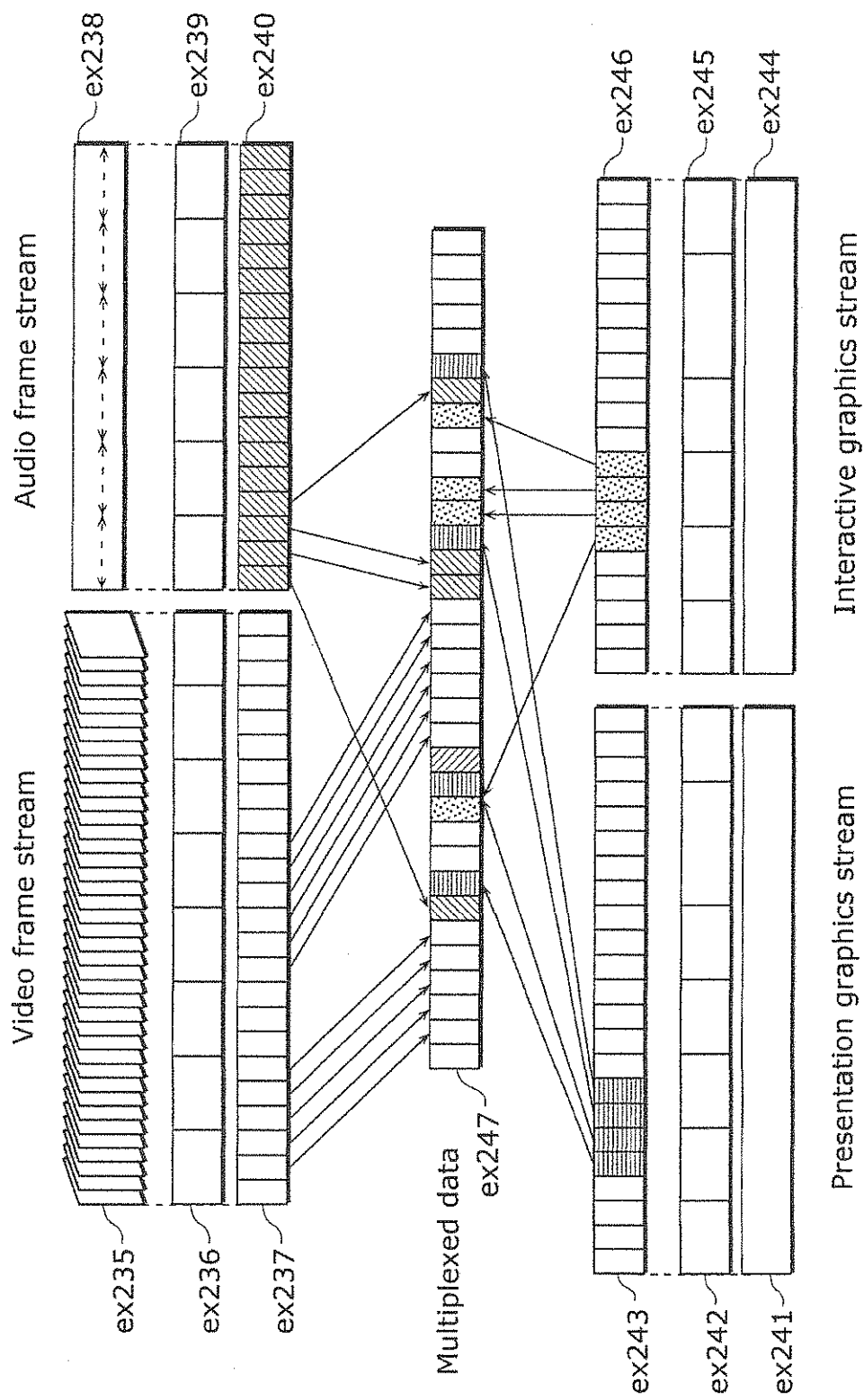


FIG. 45

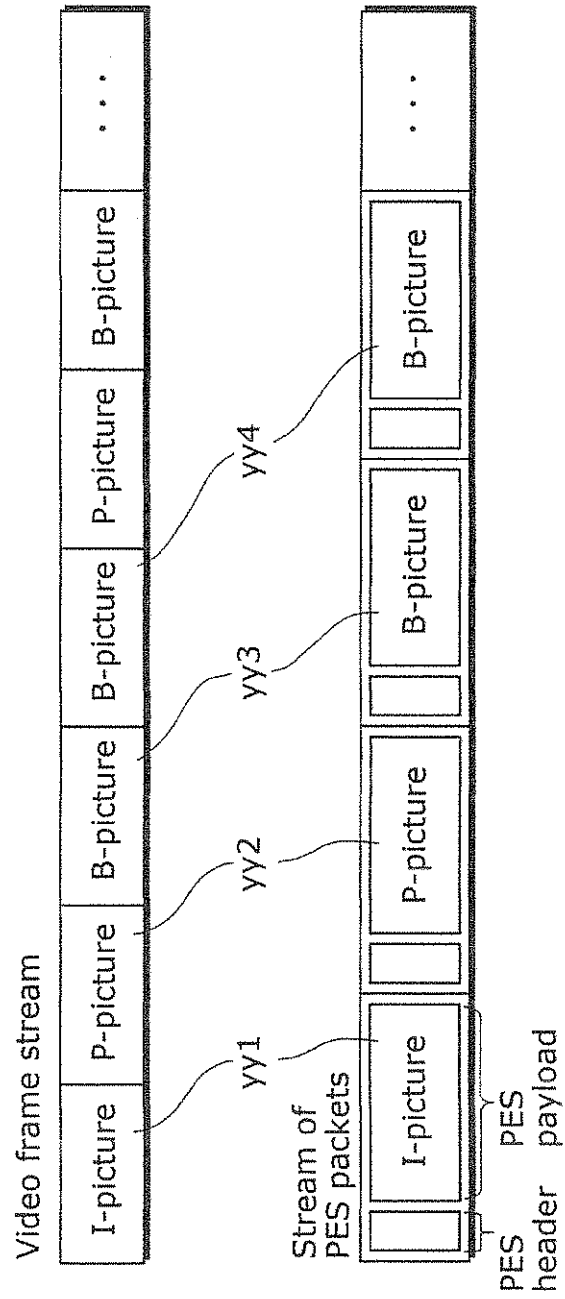
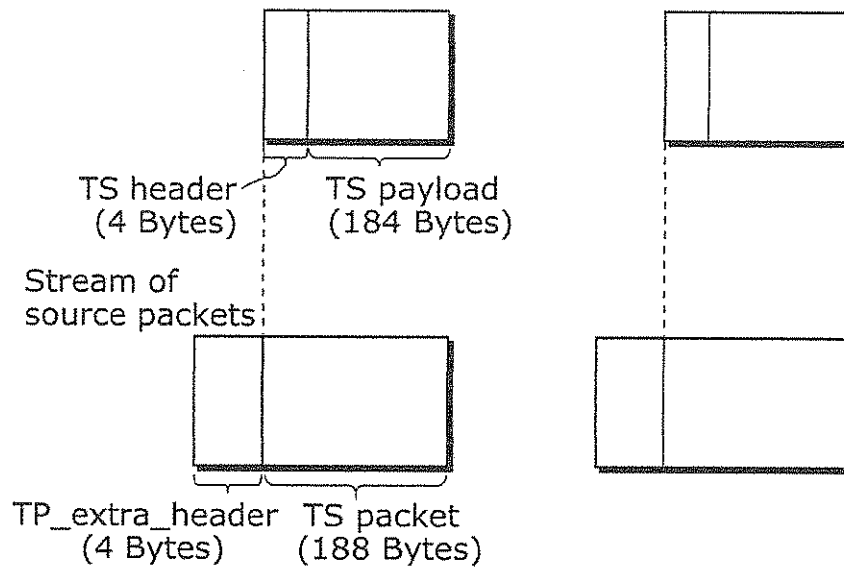


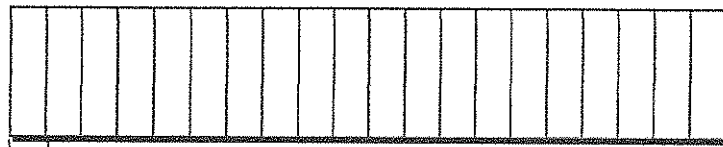
FIG. 46

Stream of TS packets



Multiplexed data

SPN 0 1 2 3 4 5 6 7 ...



Source packet

FIG. 47

Data structure of PMT

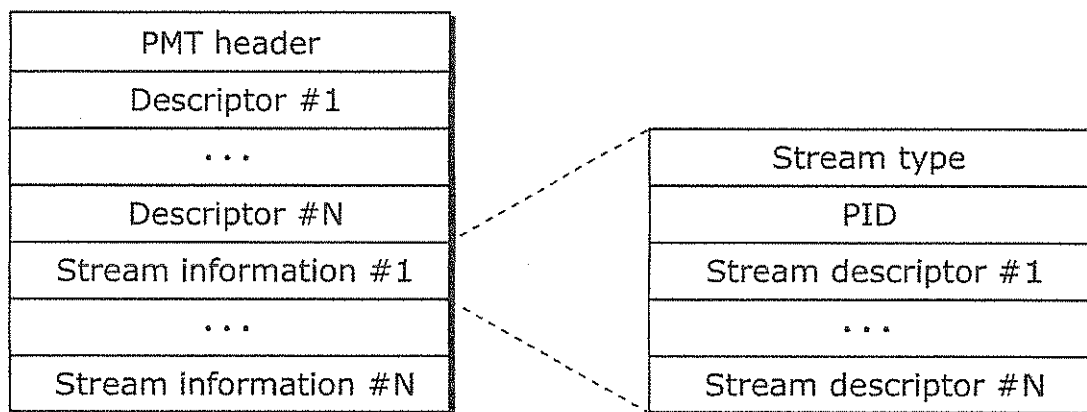


FIG. 48

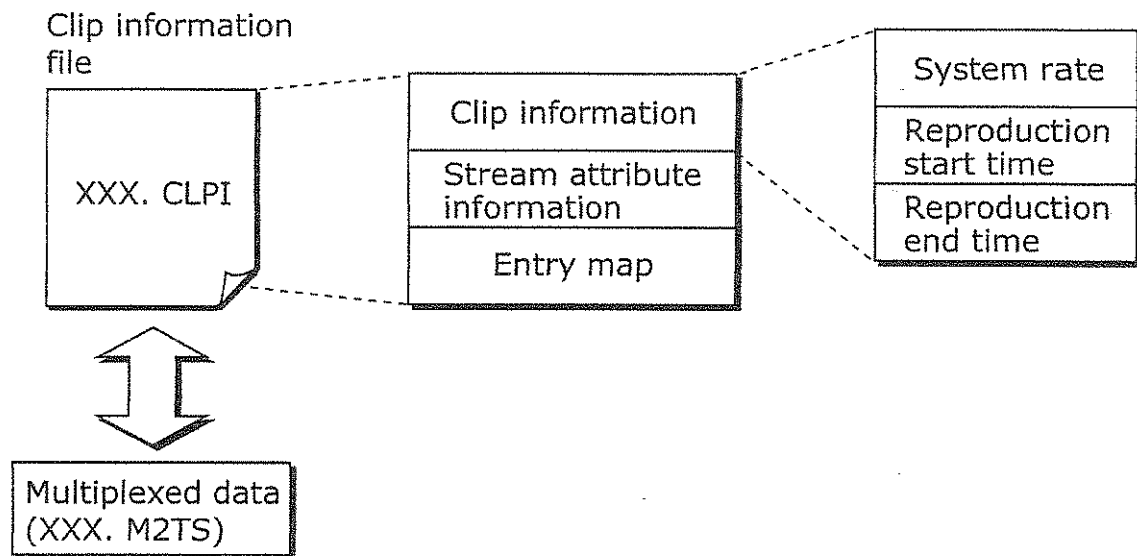


FIG. 49

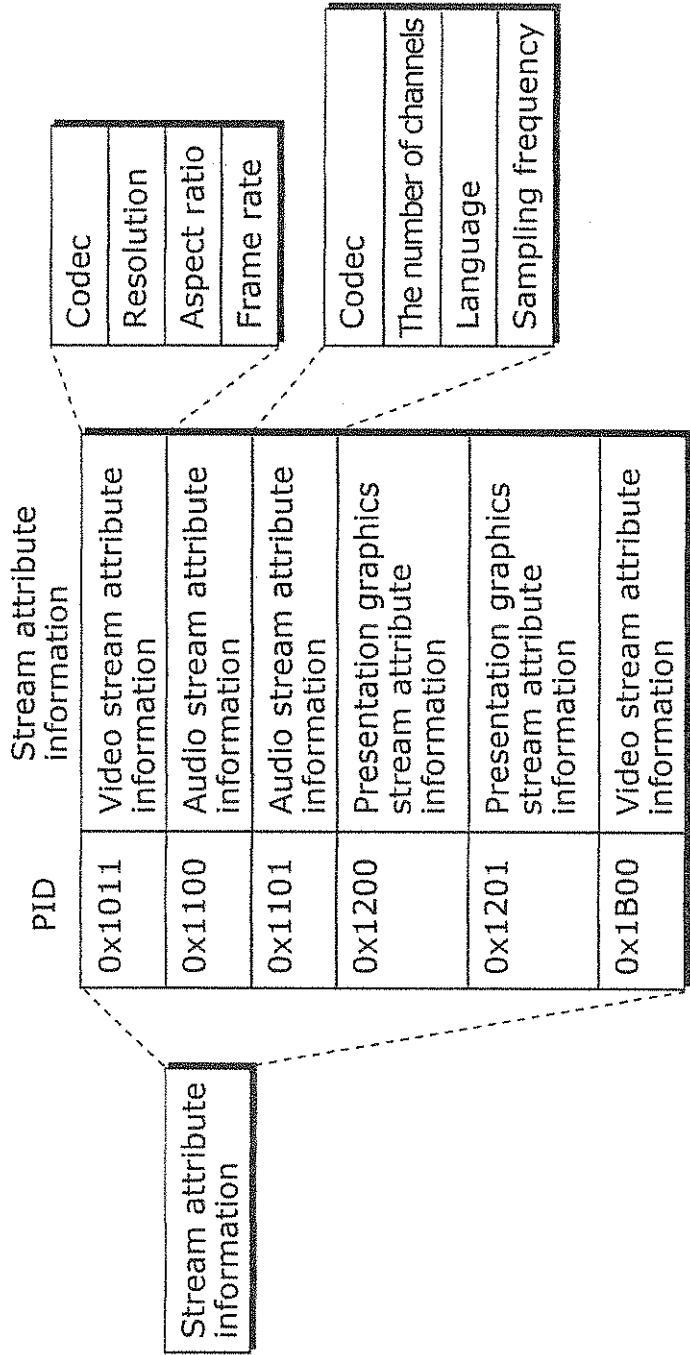


FIG. 50

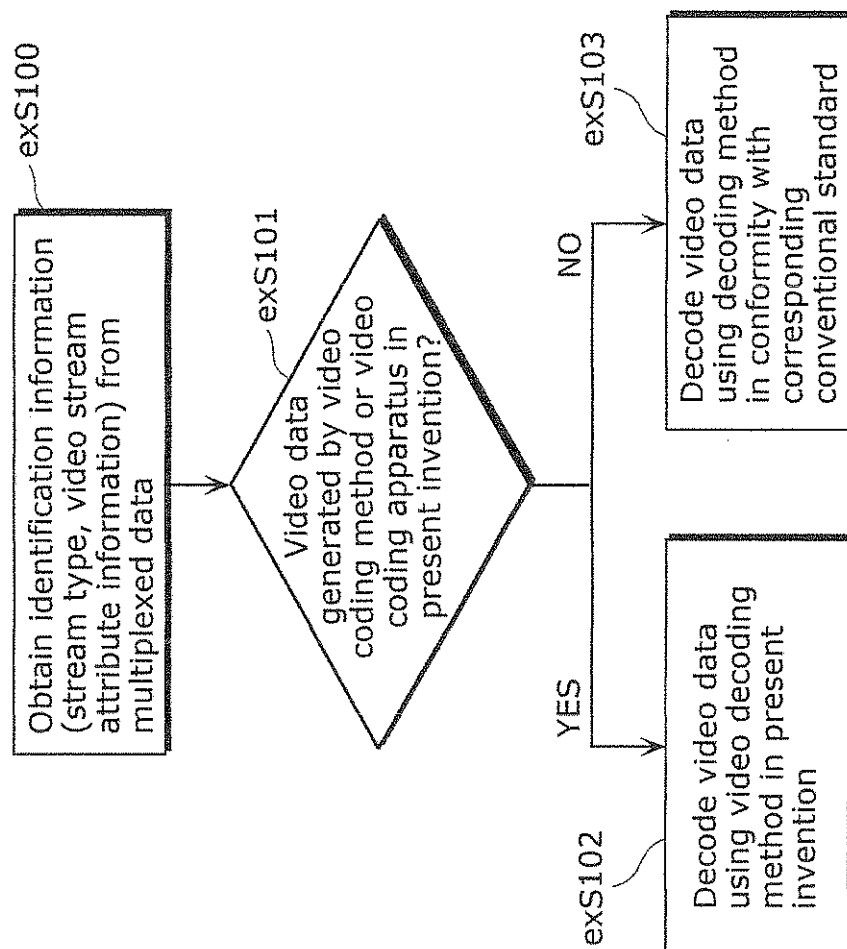


FIG. 51

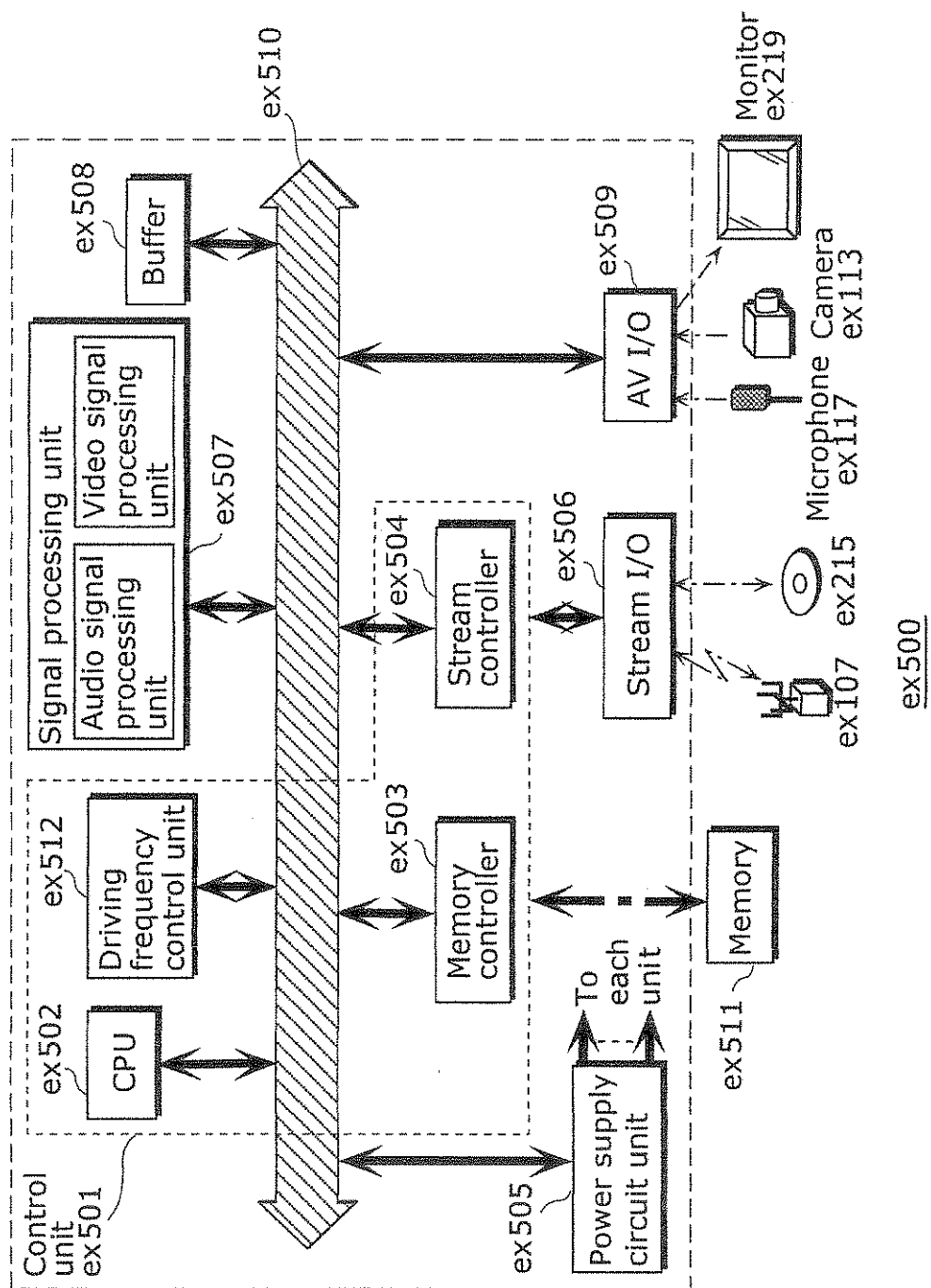


FIG. 52

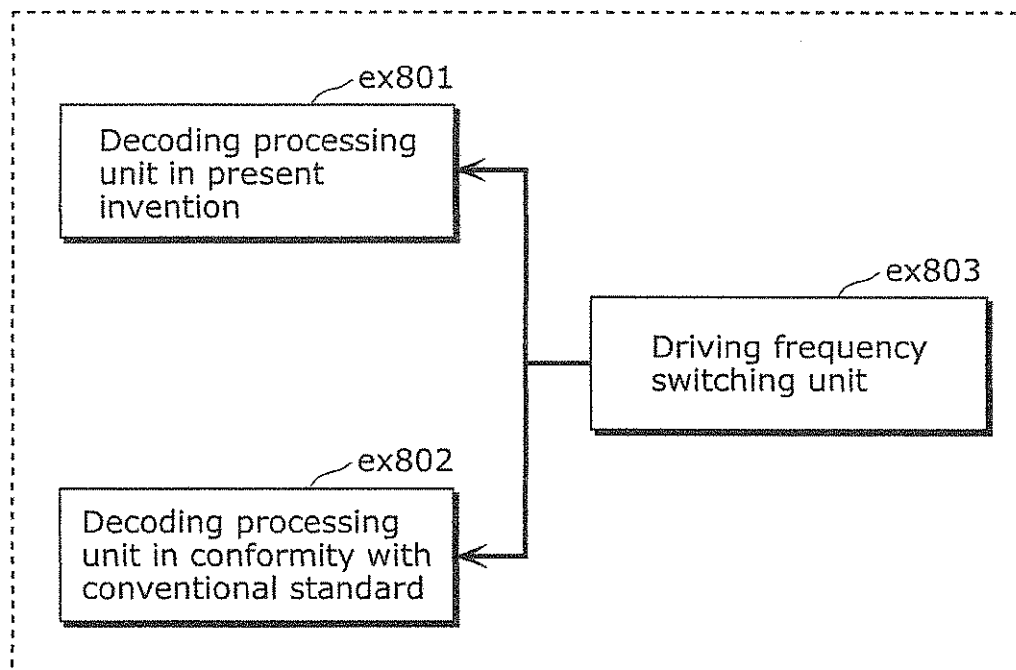


FIG. 53

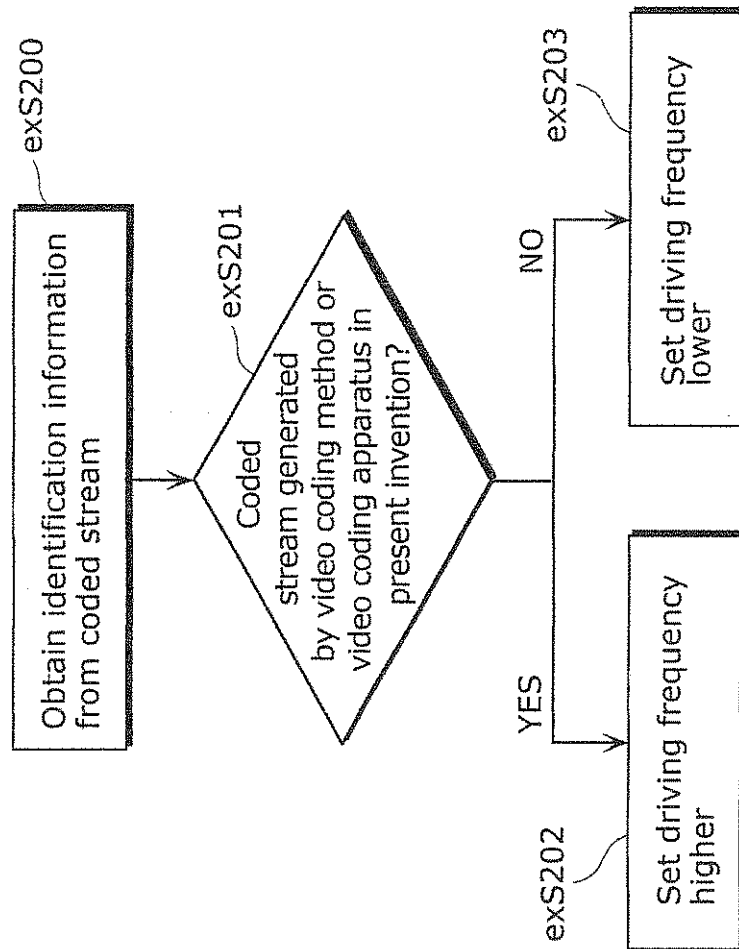


FIG. 54

Corresponding standard	Driving frequency
MPEG-4 AVC	500 MHz
MPEG-2	350 MHz
⋮	⋮

FIG. 55A

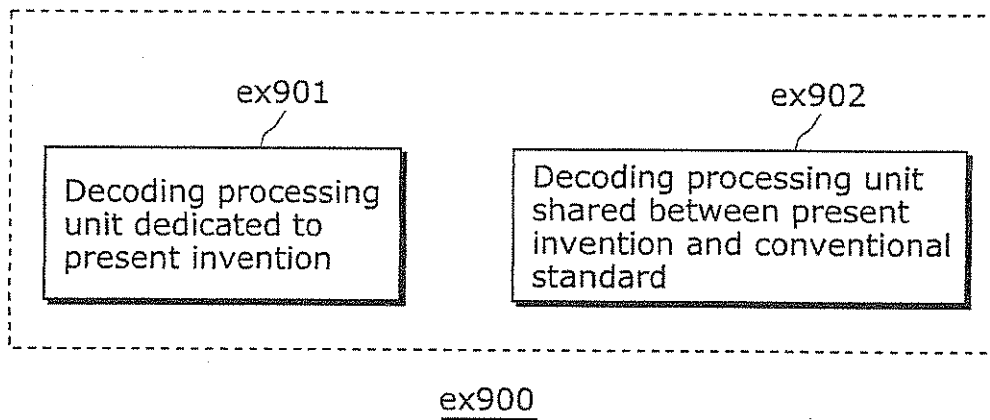


FIG. 55B

