

"A POWER CONVERTER WITH CURRENT-TYPE INVERTER"

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The present invention relates to a power
converter, with a current-type inverter.

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There has recently been suggested a PWM
current-type inverter having an advantage in that the
control circuit thereof is simple in configuration and
that the noises of the motor driven by use of it are
15 reduced, as disclosed in JP-A-62-163579. Also, an
application of this PWM current-type inverter to the
elevator control requiring high reliability and quietude
is reported in Article No. 15 at 1987 National
Conference of the Institute of Electrical Engineers of
20 Japan.

The power converter of this type comprises a
converter unit and an inverter unit with a DC reactor
interposed therebetween. The converter unit is
subjected to PWM current control by a control unit

1 including a one-chip microcomputer, and the inverter
unit is subjected to frequency control also by PWM
control of a control unit including a microcomputer.
The microcomputer of the converter unit receives a zero-
5 cross signal from a power supply for effecting synchro-
nization using the same. Methods of synchronizaiton
with a power supply are suggested in JP-A-62-171470,
JP-A-62-290359, JP-A-63-7165 and JP-A-63-7166.

The disadvantages of the conventional methods,
10 however, are that in the case where the power synchro-
nization fails to be effected with high accuracy, the DC
output current of the converter unit develops a ripple
about 6 or 12 times as large as the power frequency, and
that if the inductance of the DC reactor is small, the
15 particular ripple is applied to an induction motor
constituting a load through the inverter unit, thereby
undesirably causing a torque ripple in the motor. A
torque ripple, which is a rotational pulsation, causes a
vibration or noise in a mechanical system and may damage
20 a joint or the like parts. Also, an elevator which is
driven by an induction motor may become uncomfortable to
ride in. This problem is apparently avoided in the
conventional methods by setting the inductance of the DC
reactor at a sufficiently high level. In spite of this,
25 when the whole system is large in capacity, the volume
and cost of the DC reactor are increased unavoidably.
In a large-capacity system, therefore, it is necessary
to reduce both the volume and cost of the DC reactor

1 thereof.

A technique for improving this point has been suggested in Article No. 1483 at the 1988 National Conference of the Institute of Electrical Engineers of Japan. This suggestion was to switch the inverter pulse distribution in accordance with the DC power ripple in controlling a current-type inverter system. The output current of the inverter, however, is not necessarily in sinusoidal form but contains many high harmonic components therein. The torque ripple is thus not reduced sufficiently.

JP-A-62-163577, on the other hand, proposes a system for matching the sinusoidal characteristic of the output of a current-type inverter system with the effective utilization of the output current, wherein a predetermined time interval divided proportionately to the instant values of the sinusoidal waves of three phases, respectively, at each sampling. This prior art method has yet to solve the problems of which high harmonics contained in the output current are to be removed selectively and, for this purpose, how the width of the PWM pulse is to be calculated.

As described above, the conventional methods fail to pay sufficient attention to reducing the inductance of a DC reactor or high harmonic components of the output of a current-type inverter system in full consideration of the control of the inverter unit thereof. It is, therefore, difficult to reduce the size

of the DC reactor for a reduced cost or the high harmonic output components.

According to a first aspect of the present invention there is provided a power converter comprising a converter unit for converting an AC power into a DC output power, a current-type inverter unit for inverting the DC output of the converter unit into an AC output, a DC reactor inserted into a DC circuit connected between the converter unit and the inverter unit and a control unit for controlling each of the converter unit and the inverter unit according to pulse width modulation (PWM) control, wherein said control unit includes means for controlling a modulation rate of the inverter unit according to an instruction applied to said control unit.

According to a second aspect of the invention there is provided a power converter comprising:

- a) a converter unit for converting an AC power into a DC output power;
- b) a current-type inverter unit connected through a DC circuit for converting the DC output power of the inverter unit into an AC output power;
- c) a DC reactor connected into the DC circuit connecting said converter unit to said inverter unit;
- d) a first control unit for controlling said converter unit according to pulse width modulation control; and
- e) a second control unit for controlling an

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output frequency of the inverter unit according to pulse width modulation control, said second control unit including means for controlling a modulation rate
5 of said inverter unit according to an instruction applied to said second control unit.

The introduction of control of the modulation rate in PWM control of the PWM control system of an inverter unit permits the output current of the
10 inverter unit to be controlled accurately in accordance with a predetermined instruction, so that the effect of the ripple superimposed on the direct current supplied to

1 the inverter and that of the high harmonic components of
the output current are transmitted less to an induction
motor making up a load, thus making the induction motor
or load controllable faithfully to an instruction.

5 The present invention will now be described in greater
detail by way of examples with reference to the accompanying drawings,
wherein:-

Fig. 1 is a block diagram showing a basic
circuit configuration of a current-type inverter
according to an embodiment of the present invention.

10 Fig. 2 is a flowchart of the event computation
processing according to an embodiment of the present
invention.

Fig. 3 is a timing chart showing an example of
pulse pattern given to each transistor of the inverter
unit in the embodiment shown in Fig. 1.

15 Fig. 4 is a diagram for explaining the
operation of step F1400 in the flowchart of Fig. 2.

Fig. 5 is a flowchart of the event setting
processing for a pulse pattern effected in a
microcomputer 10 according to an embodiment of the
20 present invention.

Fig. 6 is a block diagram showing a basic
circuit configuration of a current-type ,inverter
according to a second embodiment of the present
invention.

25 Fig. 7 is a flowchart of the event computation
processing in the embodiment shown in Fig. 6.

Figs. 8A and 8B are diagrams showing the

1 relationship between the ripple component of the DC
current and the correction of the modulation rate data
effected according to the embodiment shown in Fig. 6.

Fig. 9 is a block diagram showing a basic
5 circuit configuration of a current-type inverter
according to a third embodiment of the present
invention.

Fig. 10 is a flowchart showing the event
computation processing in the embodiment shown in Fig.
10 9.

Fig. 11 is a block diagram showing a basic
circuit configuration of a current-type inverter
according to a fourth embodiment of the present
invention.

15 Fig. 12 is a flowchart of the event computa-
tion processing in the embodiment of Fig. 11.

Fig. 13 is a diagram showing a modulation
rate instruction used in the embodiment of Fig. 1.

Fig. 14 is a block diagram showing a
20 configuration of a modification of the fourth embodiment
shown in Fig. 11.

Fig. 15 is a block diagram showing a basic
circuit configuration of a current-type inverter for
driving an elevator according to a fifth embodiment of
25 the present invention.

Fig. 16 is a block diagram showing a
configuration of a current-type inverter according to a
sixth embodiment of the present invention.

1 Fig. 17 is a flowchart of the event computation processing in the embodiment shown in Fig. 16.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

 In a first embodiment of the present invention
5 shown in Fig. 1, reference numeral 1 designates a three-phase AC power supply, numeral 2 an overvoltage-controlling capacitor, numeral 3 a current-type converter unit, numerals 31 to 36 transistors making up main switching elements thereof, numeral 4 a DC reactor,
10 numeral 5 a current-type inverter unit, numerals 51 to 56 transistors making up main switching elements thereof, numeral 6 an overvoltage-controlling capacitor, numeral 7 an induction motor illustrated as an example of load, numeral 8 a DC current detector, numeral 9 a
15 comparator for comparing the primary current instruction i_1 with a feedback value i_1 , and numerals 10, 11 one-chip microcomputers forming the nucleus of a control section for supplying a pulse pattern (control signal) to the transistors 31 to 36 and 51 to 56 (These one-
20 chip microcomputers 10 and 11 are constructed of the same hardware and therefore the one-chip microcomputer 10 will be mainly referred to in the following explanation). Incidentally, the microcomputer 11 of the converter unit 3 performs the processings for (1) power
25 synchronization, (2) issuing a frequency instruction coincident with the power frequency, and (3) preparing a phase instruction from a current error. Also, the

1 current is controlled by PWM control.

The one-chip microcomputer 10 which is for controlling the frequency of the inverter unit 5 by PWM control, includes an input port 101, an internal bus 102, a ROM 103 for storing a program, a pulse width data table, etc., a RAM 104 used for temporary storage or as a register, an ALU 105 for executing computations and the like, an event setting register 107 (The "event" means indicating whether an output signal is high or low in level) for applying a control signal including a predetermined pulse pattern to the output port 106, a time setting register 108 for setting the time when the particular event is enabled, a holding register 109 for connecting and holding the contents of the setting registers 107, 108, an associative memory 110 in which several sets of data set in the holding register 109 are stored in cycles sequentially, a timer 111 for producing an actual time data, a comparator 112 for comparing the time on the timer 111 with the set time data in the associative memory 110 and producing an output therefrom when they coincide with each other, and an execution controller 113 for applying to the output port 106 and controlling the event set triggered by the comparator 112.

25 Numeral 12 designates a terminal supplied with a primary current instruction i_1^* applied to the converter control system, numerals 13, 14 terminals supplied with a frequency instruction ω_1^* and a phase

1 instruction θ^* applied to the inverter control system,
 and numeral 15 a signal line for supplying a signal for
 power synchronization. The primary current instruction
 signal i_1^* is adapted to be applied to the comparator 17
 5 through a delay element 16 for causing a delay corre-
 sponding to the response delay in a current control
 system, that is, in such a feedback control loop that
 the primary current instruction signal i_1^* and a DC
 current detected by the detector 8 are compared and an
 10 error therebetween Δi_1 is detected by the comparator 9
 and is reduced to zero. The DC current i_1 detected by
 the DC current detector 8, on the other hand, is also
 applied to the comparator 17, and the current ripple
 component Δi^* produced from the comparator 17 is applied
 15 to the one-chip microcomputer 10 for controlling the
 inverter unit 5.

Now, with regard to an event caused at the
 output port 106 according to a first embodiment of the
 present invention, the processing flow of an event
 20 computation processing program F1000 for determining a
 pulse pattern applied to the transistors 51 to 56 (S51
 to S56) making up main switching devices of the inverter
 unit 5 in the one-chip microcomputer will be explained
 with reference to Fig. 2.

25 (1) First, step F1100 reads from the input port
 101 the ripple component Δi^* providing an adjustment
 term in controlling the frequency instruction ω_1^* , the
 phase instruction θ^* and the modulation rate. In the

- 1 case where the frequency instruction ω_1^* and the phase instruction θ^* are computed in the one-chip microcomputer 10, the input port may be read only for the ripple component but not for any others.
- 5 (2) Step F1200 integrates the frequency instruction $\omega_1^*(\text{Hz})$ at every predetermined time interval Δt_1 , and the phase instruction θ^* is added to the result of integration to determine a general phase θ_T .
- (3) Step F1300 determines one of the six modes of
 10 pulse pattern into which the electrical angle of 360° is divided for each 60° , to be produced for the present general phase θ_T that is, an output event defined in accordance with the general phase θ_T . The relationship between the general phase θ_T and the six modes, which is
 15 not directly connected with the substance of the present invention and will not be described in detail, is explained in JP-A-62-163577, for example.
- (4) Finally, step F1400 determines the times T_A and $T_A + T_B$ at which the binary level, 0 or 1, of the
 20 pulse is changed, respectively, during the interrupt interval Δt_1 (As shown in Fig. 3, T_A is a turn-on period of S53, T_B a turn-on period of S51, and $\Delta t_1 - (T_A + T_B)$ a turn-on period of S52 when $0 \leq \theta_T \leq 60^\circ$) with reference to a data table based on the general phase θ_T .
- 25 Further, on the basis of a modulation rate ($\gamma - \Delta_i^*$) determined from the current ripple Δ_i^* taken in and a reference modulation rate γ for determining the degree to which the output of the converter unit 3 is changed

- 1 by the inverter unit 5 in the microcomputer, the time data T_A and $T_A + T_B$ searched for above are corrected in the manner mentioned below.

$$T_A' \leftarrow (\gamma - \Delta_i^*) \cdot T_A \quad (1)$$

$$(T_A' + T_B') \leftarrow (\gamma - \Delta_i^*) \cdot (T_A + T_B) \quad (2)$$

- This correction is effected by rewriting the time data T_A and $T_A + T_B$ searched for into $\gamma \cdot T_A$ and $\gamma \cdot (T_A + T_B)$ respectively in accordance with the reference modulation rate data γ , if the ripple component Δ_i^* is zero, for example. In the case where the ripple component Δ_i^* is positive, that is, in the case where the DC current i_1 detected by the DC current detector 8 is slightly larger than the current instruction i_1^* , the modulation rate instruction taking the ripple component Δ_i^* , that is, the adjustment term into consideration is $(\gamma - \Delta_i^*)$, which is a value smaller than the reference value γ by Δ_i^* . Thus, when the ripple component Δ_i^* is negative, the modulation rate instruction is $(\gamma - (-\Delta_i^*))$ which is larger than the reference value γ by Δ_i^* . If the time data T_A and $T_A + T_B$ searched for are modified by use of this value, the time data T_A' and $T_A' + T_B'$ after correction have a time width thereof shorter than the time data T_A and $T_A + T_B$ by a value equivalent to the ripple component Δ_i^* . The above-mentioned reference modulation rate γ which may be corrected in either positive or negative direction according to the ripple

1 component is set to a value smaller than unity such as
0.9 or 0.95. This is also the case with the other
embodiments described below.

Fig. 3 shows an example of the pulse patterns
5 S51 to S56 applied to the switching elements 51 to 56,
respectively, for one switching period Δt_1 of the
transistors, that is, a part of the on and off pulse
patterns applied to the transistors 51 to 56 of the
inverter unit 5. In Fig. 3, the solid lines indicate
10 the lack of ripple, and the dashed lines the presence of
ripple.

The pulse width data is corrected by a value
corresponding to Δi^* in the pulse width for the
transistor S52 providing a shorting phase thereby to
15 increase or decrease the shortcircuiting current. In
other words, in the case where Δi^* is positive, the
ripple component thereof fails to be produced as an
output of the inverter unit 5 but flows through the
transistor S52 that is a shortcircuiting phase arm.
20 When Δi^* is negative, by contrast, $T_A + T_B < T_A' + T_B'$,
and therefore, the pulse width applied to the transistor
S52 is shortened, so that the current flowing in the
transistor S52 by shortcircuiting is reduced by the
amount of the ripple, thereby increasing the the output
25 of the inverter unit 5. As a result, even if the input
DC current to the inverter unit 5 is larger or smaller
by the ripple component Δi^* than the current instruction
 i_1^* , the output current of the inverter unit 5 is

- 1 controlled to coincide with the current instruction i_1^* ,
and the output current is produced in sinusoidal form.

The reason why step F1400 determines the
reference modulation rate γ and controls the modulation
5 rate of the inverter unit 5 around the reference
modulation rate γ is because the ripple component Δi^*
detected has both positive and negative characteristics
and therefore the modulation rate may be required to be
corrected upward unlike in the aforementioned case.

- 10 Assuming that the reference modulation rate γ is 0.95,
for instance, the current utilization rate at the
inverter unit 5 falls by an average of 5%.

The delay element 16 for determining the
ripple component Δi^* is inserted against the current
15 instruction i_1^* by reason of the fact that simple
comparison between the current instruction i_1^* and the
detected current i_1 would cause a detected ripple
component to mix with a transient error under an abrupt
change in the current instruction i_1^* with the result
20 that the control system of the converter unit 3 would
undesirably interfere with that of the inverter unit 5.
The delay element according to the embodiment of the
present invention is based on a simulation of the
operation delay of the current control system. If means
25 for limiting the adjustment term $(\gamma - \Delta i^*)$ for the
modulation rate against the current ripple component Δi^*
is attached to the comparator 17, or is incorporated in
step F1400 in Fig. 2 for software processing of the

1 microcomputer 10, however, the phenomenon of interference mentioned above is prevented. In that case, the delay element 16 may be done.

In processing the aforementioned step F1400,
5 in order to determine the pulse widths T_A and T_B in accordance with the general phase θ_T , a table is searched for. Specifically, this search is made by checking a look-up table showing the values of a pair of sinusoidal curves at each of predetermined electrical
10 angles or phases θ_T in a range of electrical angles of 0° to 60° , as shown in Fig. 4. The pulse width for the shortcircuiting phase is determined as $(\Delta t_1 - T_A - T_B)$ as described above, and therefore no specific table is required. A method of calculating the pulse width by
15 distribution of crest values of sinusoidal wave is described in detail in JP-A-62-163577 referred to above.

The process mentioned above determines two data items including the contents of an event and the time of event change set in the event setting register
20 107 and the time setting register 108. These items are required to be set in the associative memory 110 for output port control in order to control the transistors 51 to 56 of the inverter unit 5 through the output port 106.

25 A flow of the process F2000 for setting these items is shown in Fig. 5, with reference to which explanation will be made below. This process F2000 is effected in the microcomputer 10.

- 1 (1) First, step F2100 determines whether an event and the time are set completely as required in the six transistors of the inverter unit 5. If the answer is "Yes", the process is finished.
- 5 (2) If the decision at step F2100 is "No", on the other hand, step F2200 sets a corresponding event in the event setting register 107, followed by step F2300 for setting the time of event change in the time setting register 108 thereby to complete the process.

10 The above-mentioned event setting process F2000 and the time computation process F1000 may be energized for each switching interval time Δt_1 of the transistors 51 to 56 making up main switching elements of the inverter unit 5 respectively, that is to say, for
15 each time providing a reciprocal of the switching frequency. In other words, as far as the event computation and event setting are effected for each time of Δt_1 , the latest pulse pattern is always produced from the output port 106 of the microcomputer 10 for
20 controlling the inverter unit 5.

According to the first embodiment of the present invention mentioned above, the modulation rate is controlled for the inverter unit in such a way as to offset the ripple component of the DC current applied to
25 the inverter unit, and therefore the DC reactor is reduced greatly, even in the presence of a ripple component, that is, even if the inductance of the DC reactor inserted between the converter unit and the

1 inverter unit is small.

The absence of a ripple component in the output current of the inverter unit 5 assures smooth revolutions of the motor 7, reduces the noises or
5 vibrations of the mechanical system, and greatly improves the riding quality of an elevator which may be driven by the motor 7.

The allowability to contain a ripple component in the output current of the converter unit 3 eliminates
10 the process of minimizing the ripple component on the part of the microcomputer 11 of the converter unit 3, and accordingly a sophisticated device is not required as the microcomputer 11.

Fig. 6 shows a second embodiment of the
15 present invention, in which a rectification ripple of the converter unit 3 supplied with a three-phase AC power from a power supply 1 is estimated and this ripple component is cancelled by controlling the modulation rate on the side of the inverter unit 5. This embodi-
20 ment is different from the first embodiment shown in Fig. 1 in that in the embodiment under consideration, a power sync signal 15 for detecting the starting point of a ripple is applied to a micro-computer for controlling the inverter unit 5. The parts in Fig. 6 are configured
25 in the same way as in the first embodiment. In Fig. 6, the component parts designated by the same reference numerals as in Fig. 1 designate corresponding or identical parts respectively.

1 The operation of this second embodiment of the
present invention will be explained with reference to
step F1000 representing the event computation process
shown in Fig. 7 and the current waveform shown in Fig.
5 8. The event computation processing F1000 is effected
in the microcomputer 10.

(1) As in the processing according to the first
embodiment explained with reference to Fig. 2, steps
F1100 to F1300 read the frequency instruction ω_1^* , phase
10 instruction θ^* and the power sync signal 15, calculate
the general phase θ_T and thus determine the pulse
pattern (event) to be given to the six transistors.

(2) Then, step F1500 searches the modulation rate
data r' in accordance with the lapse of time from the
15 input of the power sync signal 15.

Generally, the DC output I_d of the converter
unit 3 has a waveform shown in Fig. 8A due to the ripple
component superimposed thereon. The above-mentioned
modulation rate data r' for correction is such as to
20 offset the ripple of the DC current I_d as an example
thereof is shown in Fig. 8B, or in average, such a data
as to alternate vertically above and below the reference
modulation rate data r' . If a data as shown in Fig. 8B
is offered as a table to which reference is made by the
25 time lapse from the input time (A) of the sync signal
from the signal porch 15, it is possible to obtain a
modulation rate data r' for correction.

1 (3) Step F1600 then determines from Fig. 4 the
time data T_A and $T_A + T_B$ taken before the pulse pattern
is changed in accordance with the general phase θ_T
computed at step F1200. Further, the modulation rate γ'
5 for correction determined at step F1500 is multiplied by
these time data thereby to calculate the corrected time
data T_A' and $T_A' + T_B'$ ($T_A' = T_A \cdot \gamma'$, $T_A' + T_B' = T_A' \cdot \gamma' +$
 $T_B \cdot \gamma'$). These values are used as a pulse pattern-
setting data.

10 According to the second embodiment described
above, it is possible to offset the ripple of a DC
current by control at the inverter unit simply by taking
in the power sync signal, and therefore as in the first
embodiment, the DC reactor is reduced in size and a
15 special comparator circuit and the like are eliminated
outside of the control unit, thus simplifying the
circuit configuration.

Also in this embodiment, as in the first
embodiment, the ripple current component Δi^* may be
20 taken into consideration by applying the same component
to the microcomputer 10.

Fig. 9 shows a third embodiment of the present
invention, in which the microcomputer 10 for controlling
the inverter 5 is supplied with and a current instruc-
25 tion i_1^* and a DC current i_1 detected at a DC current
detector 8.

In the embodiment of Fig. 9, the component
elements designated by the same reference numerals as

- 1 those in Fig. 1 designate the same or equivalent
component parts respectively.

Step F1000 for event computation processing in
the microcomputer 10 according to the third embodiment
5 is effected according to the flow shown in Fig. 10.

(1) First, step F1100 takes in the frequency
instruction ω_1^* , phase instruction θ^* and also a DC
current i_1 and a current instruction i_1^* .

(2) Then, step F1700 compensates the current
10 instruction i_1^* thus taken in at step F1100 for a delay
corresponding to that of the current control system to
compute a compensation value I_1^* . Further, step 1800
subtracts the compensation value I_1^* from the DC current
 i_1 to determine a current error Δi^* , that is, an
15 adjustment term of the modulation rate.

(3) As in the case of Fig. 2 mentioned above, step
F1200 determines the general phase θ_T , and step F1300
determines a pulse pattern (event) to be given to the
six transistors in accordance with the general phase θ_T .

20 (4) Finally, step 1400 determines from Fig. 4 the
time data T_A and $T_A + T_B$ taken before the pulse pattern
is changed in accordance with the general phase θ_T
calculated at step F1200, and further, taking the
adjustment term Δi^* determined at step F1800 into
25 consideration, the above-mentioned time data, that is,
the pulse width data is corrected and computed, thus
preparing a pulse pattern used for event setting.

1 According to the third embodiment described
above, as in the first and second embodiments, not only
the DC reactor is reduced in size but also there is no
need of an external comparator circuit or a delay
5 element. The size of the control section is also
reduced.

A fourth embodiment of the present invention
is shown in Fig. 11. According to this embodiment,
which minimizes the high harmonic components contained
10 in the inverter output, the control microcomputer 10 of
the inverter unit 5 is supplied with a frequency
instruction ω_1^* , a phase instruction θ^* and also a
modulation instruction γ^* for the inverter output
current from a terminal 18. The processing for event
15 computation in the microcomputer 10 in this configura-
tion is effected according to the flow shown in Fig. 12.

In Fig. 11, the component parts designated by
the same reference numerals as in Fig. 1 designate the
same or equivalent component parts respectively.

20 (1) First, steps F1100 to F1300 take in the
frequency instruction ω_1^* , the phase instruction θ^* and
the modulation rate instruction γ^* , and as in other
embodiments mentioned above, determine the general phase
 θ_T , in accordance with which a pulse pattern (event)
25 given to the six transistors is determined.

(2) Then, the time T_A and $T_A + T_B$ taken before a
pulse pattern change is determined with reference to a
table as in the other embodiments. Further, in

- 1 accordance with the modulation rate instruction r^* taken
in at step F1100, the time data T_A and $T_A + T_B$ are
corrected to $r^* \cdot T_A$ and $r^* \cdot (T_A + T_B)$ thereby to prepare a
pulse pattern for the transistors 51 to 55 of the
5 inverter unit 5.

A fourth embodiment of the present invention has a primary feature in the manner of determining the modulation rate instruction value r^* given to the microcomputer 10.

- 10 An example of experiment conducted with various high harmonics is shown in Fig. 13, in which the abscissa represents the value of the modulation rate instruction r^* and the ordinate the magnitude of the high harmonic component contained in the output of the
15 inverter unit 5 in the construction of the fourth embodiment of the present invention.

- It is seen from this experiment result that if main emphasis is placed on removing the fifth-power high harmonic component from the output of the inverter unit
20 5, the modulation rate instruction r^* applied to the microcomputer 10 providing an inverter control should be set at point C in Fig. 13. In similar fashion, in the case where it is desired to remove only a specific high harmonic component other than above from the output of
25 the inverter unit 5, a modulation rate instruction should be set that minimizes the magnitude of the high harmonic component corresponding to the characteristics thereof. Also, if it is desired to reduce the high

1 harmonic components in general fashion with a view to
the general value of the high harmonic components of the
output of the inverter unit 5, on the other hand, the
modulation rate instruction γ^* should be set at a point
5 in the neighborhood of point B in Fig. 13 where the high
harmonic components are generally reduced. In setting
the modulation rate instruction, a given modulation rate
instruction γ^* may be stored in the ROM 103 in the case
of a fixed control for removing a specific high harmonic
10 component. If the high harmonic to be removed changes
depending on the situation, however, instructions may be
applied by way of port from a terminal 18 as shown in
Fig. 11. In such a case, the value γ^* may be determined
by a host microcomputer not shown as in the case of each
15 instruction of ω_1^* , θ^* and i_1^* .

As explained above, according to the fourth
embodiment of the present invention, a modulation rate
instruction at point B or C is set, and the modulation
rate of the inverter unit 5 is controlled in accordance
20 with the procedure shown in Fig. 12 to remove a specific
high harmonic or reduce high harmonic components in
general from the output of the inverter unit 5.

In the case of the fourth embodiment described
above, however, the modulation rate is set at a level
25 lower than a setting normally designated at point A,
such as the above-mentioned reference rate or unity
permitting the maximum output operation of the inverter,
thereby causing a problem of a transiently small current

1 value supplied to the motor or the like making up the
load 7. This problem may be solved to some degree by
the operation of speed feedback control constituted by a
major loop control circuitry not shown. Also, in order
5 to improve this problem more positively, a cooperative
control may be introduced in such a manner that the
modulation rate instruction γ^* is transmitted to the
control microcomputer 11 of the converter unit 3 and the
current decreasing on the inverter side is compensated
10 incrementally by a converter.

Fig. 14 is a block diagram showing a
configuration of a modification of the fourth embodiment
of the present invention incorporating the last-
mentioned functions.

15 In this example, the modulation rate instruc-
tion γ^* is applied also to the control microcomputer 11
of the converter unit 3, and according to this modula-
tion rate instruction γ^* , the microcomputer 11 controls
the inverter unit 3 in such a way that the decreasing
20 current on the inverter side is compensated upward on
the converter side in advance.

In the fourth embodiment and a modification
thereof explained above with reference to Figs. 11 and
14, the modulation rate instruction γ^* is applied to the
25 inverter control microcomputer 10 from outside thereof.
This modulation rate instruction γ^* , however, may be set
in advance in the program of the ROM 103 of the
microcomputer 10 with equal effect.

1 According to the fourth embodiment shown in
Figs. 11 and 14, like in the first embodiment of the
present invention, the ripple component Δi^* may be
applied to the microcomputer 10 for compensating for the
5 ripple component.

Fig. 15 is a block diagram showing a configuration of a fifth embodiment of the present invention to which the first embodiment shown in Fig. 1 is applied.

The fifth embodiment of the present invention
10 is so constructed that in the first embodiment of the invention explained with reference to Fig. 1, the motor making up the load 7 drives an elevator cage 60 and a counterweight 61 through a rope 63 and a sheave 62. This system is thus configured with the inductance of
15 the DC reactor set below 6 mH.

Generally, an elevator system comprises a control board incorporating a power converter including a converter unit 3, a DC reactor 4 and an inverter unit 5 and control microcomputers 10, 11, which control board
20 is in turn installed in a machine room at the top floor of the building together with a winching motor or the like making up a load 7 of the power converter. The machine room is desirably small in space for effective utilization of indoor space.

25 Among the units installed in the control board, the DC reactor weighs several hundred kilograms for about 10 mH in the prior art. The weight and bulkiness of the DC reactor occupying a large proportion

1 of the machine room space has been a problem specific to
an elevator system.

A fifth embodiment of the present invention
shown in Fig. 15 is an application of the first embodi-
5 ment shown in Fig. 1 to driving a winching motor for the
elevator system, in which the inverter unit 3 is appro-
priately controlled to assure optimum control of the
output thereof without being affected by the current
ripple superimposed on the direct current applied to the
10 same inverter unit 3. As a result, according to this
embodiment, it has been confirmed that the inductance of
the DC reactor is sufficiently reduced to less than 6 mH
as compared with the prior art.

If the DC reactor 4 is reduced below 6 mH, the
15 weight thereof is also saved by about one half as small
as the conventional DC reactor of about 10 mH (as shown
in Fig. 1). This reduction in size of the DC reactor
(1) reduces the machine room space, (2) facilitates
delivery into the machine room, (3) makes it possible to
20 reduce the floor strength of the machine room, (4) saves
the power loss at the DC reactor 4, and (5) lessens the
size of the processing circuit to cope with an over
voltage.

A sixth embodiment of the present invention
25 shown in Fig. 16 is so configured that the control
microcomputer 11 for the converter unit 3 and the
control microcomputer 10 for the inverter unit 5 are
supplied with a power demand instruction P^* anew from a

1 terminal 29 in addition to the modulation rate instruc-
 tion γ^* for the inverter unit 3. The power demand
 instruction P^* is issued to designate "1" for full-load
 upward drive or no-load downward drive (under heavy
 5 load) and "0" for other cases (under light load) in an
 application of the present embodiment to elevator
 control or the like case requiring various inverter
 outputs. The modulation rate instruction γ^* is for
 controlling the inverter modulation rate in a manner to
 10 minimize the high harmonic component of the inverter
 output as described above. Incidentally, the power
 demand instruction P^* , like the instructions ω_1^* and θ^* ,
 are supplied automatically from the host (not shown) of
 the microcomputers 10, 11. Also, the ripple component
 15 tends to assume a large value in a low output region and
 a small value in a high output region. In a high output
 region involving a full-load upward operation,
 therefore, it is more important to supply power securely
 to the motor for assuring the upward movement of the
 20 elevator at a specified speed than to remove high
 harmonics.

The operation of step F1000 for even
 computation processing according to the sixth embodiment
 satisfying the above-mentioned requirements will be
 25 explained with reference to Fig. 17.

(1) First, steps F1100 to F1300 take in the
 frequency instruction ω_1^* , phase instruction θ^* , power
 demand instruction P^* and the modulation rate instruc-

1 tion r^* , determine the general phase θ_T in the same
 manner as in other embodiments described above, and thus
 determine a pulse pattern (event) to be applied to the
 six transistors in accordance with the value of the
 5 general phase θ_T .

(2) Step F1400 then determines the time T_A and T_A
 + T_B taken before a change in pulse pattern with
 reference to a table as in other embodiments. The time
 data thus determined has such a value that the modula-
 10 tion rate of unity, that is, the output peak power of
 the inverter is retrieved most readily as an inverter
 control system.

(3) Step F3000 decides whether full power is to be
 produced at present, on the basis of the value of the
 15 power demand instruction P^* .

(4) If the decision at step F3000 is "Yes", the
 process proceeds to step F3200 where the modulation rate
 instruction supplied is ignored, and while placing most
 emphasis on the power output, the time data T_A and T_A +
 20 T_B providing the pulse width data mentioned above are
 left uncorrected. Since the control microcomputer 10
 for the inverter unit 5 is not controlled specifically
 against the modulation rate, the control microcomputer
 11 for the converter 3 is not subjected to cooperative
 25 control in recognition of such fact from the power
 demand instruction P^* .

(5) If the decision at step F3000 is "No", that
 is, when full power output is not required, on the other

1 hand, in order to secure control placing emphasis on
ripple compensation, the process proceeds to step F3100
where the time data T_A and $T_A + T_B$ are corrected in
accordance with the modulation rate instruction γ^* with
5 reference to the table and the corrected data $\gamma^* \cdot T_A$ and
 $\gamma^* \cdot (T_A + T_B)$ are computed.

In the sixth embodiment described above, if
the load demands full power, the modulation rate
instruction may be ignored for preferring power control.
10 When full power output is not required, by contrast, the
modulation rate instruction is taken into consideration
with primary emphasis placed on the index of performance
for control, so that a reduced gain on the inverter side
is recognized by the control microcomputer 11 of the
15 converter unit 3 from the power demand instruction P^*
thereby to correct the modulation rate of the converter
unit 3.

According to the sixth embodiment of the
present invention, as explained above, a predetermined
20 index of performance is usable for control even in the
case where the capacity of the power converter is
limited.

Although the sixth embodiment of the invention
has been explained above with the power demand
25 instruction P^* in binary form, this instruction may be
divided in multiple stages and the modulation rate
instruction γ^* may be presented in successive forms
including "80% satisfactory control", "60% satisfactory

1 control" and the like.

In each of the aforementioned embodiments, the transistors 31 to 36 and 51 to 56 of the converter unit 3 and the inverter unit 5 may be replaced by a gate 5 turn-off thyristor GTO, field effect transistor FET, insulation gate bipolar transistor IGBT, thyristor with commutation circuit or the like with equal effect.

It will thus be understood from the foregoing description that according to the present invention a 10 power converter may be controlled with a modulation rate based on a factor other than for normal modulation rate control, resulting in a smaller size of the DC reactor making up a DC-AC coupler, a smaller high harmonic component of the inverter output, and a reduced high 15 harmonic component leaking out to the power supply side providing converter input. As additional effects, the reduced leak of the high harmonic component toward the power supply side prevents flicker of a fluorescent lamp which may be connected to the power supply on one hand 20 and the overheating of a lagging capacitor on the other hand.

**CLAIMS**

1. A power converter comprising a converter unit for converting an AC power into a DC output power, a current-type inverter unit for inverting the DC output
5 of the converter unit into an AC output, a DC reactor inserted into a DC circuit connected between the converter unit and the inverter unit and a control unit for controlling each of the converter unit and the inverter unit according to pulse width modulation
10 (PWM) control, wherein said control unit includes means for controlling a modulation rate of the inverter unit according to an instruction applied to said control unit.
2. A power converter according to claim 1, wherein
15 said instruction includes a signal indicative of a DC ripple component applied to the current-type inverter unit.
3. A power converter according to claim 2, wherein
20 said ripple component is obtained from a DC input current of said current-type inverter unit.
4. A power converter according to claim 2, wherein
said ripple component is obtained by calculation from a DC input current of said current-type inverter unit.
5. A power converter according to claim 2, wherein
25 said control unit corrects gate pulses for determining timings of turning on and off of switching elements of the inverter unit based on a modified modulation rate determined by the DC ripple component applied to the



inverter unit and a predetermined reference modulation rate and applies the corrected gate pulses to the switching elements of the inverter unit.

6. A power converter according to claim 5, wherein
5 said modified modulation rate is obtained by decreasing the reference modulation rate by a value corresponding to a difference Δi_1^* between a DC current i_1 applied to the inverter unit and a primary electric current command i_1^* for an output of the converter unit
10 when the former is larger than the latter.

7. A power converter according to claim 2, wherein said DC ripple component is the difference between a DC current detected at an input of the inverter unit and an electric current command for the converter unit
15 which is issued at a predetermined delay time from a time of detection of the DC current.

8. A power converter according to claim 2, wherein said control unit controls the modulation rate of the inverter unit based on the DC ripple component so that
20 the pulse width modulation control of switching elements of the inverter unit is carried out so as to cause the inverter unit to produce an output of sinusoidal waveform.

9. A power converter according to claim 1, wherein
25 said pulse width modulation control of the inverter unit is carried out by said control unit based on a difference between an input current of the inverter unit and an electric current command for an output of



the converter unit so as to cause the inverter unit to produce an output of sinusoidal waveform.

10. A power converter according to claim 1, wherein said control unit controls said inverter unit based on
5 a frequency command ω_1^* , a phase command θ^* , and a current difference Δi_1^* between a DC current i_1 applied to the inverter unit and an electric current command i_1^* for an output of the converter unit.

11. A power converter according to claim 10, wherein
10 said current difference is a difference between an instant value of the DC current detected at an input of said inverter unit and a value of the electric current command issued at a predetermined delay time from a time when the instant value of the DC current
15 is detected.

12. A power converter according to any one of the preceding claims, wherein said instruction includes a signal indicative of a DC ripple component predicted to be applied to the inverter unit.

20 13. A power converter according to claim 12, wherein said DC ripple component is predicted by determining a phase of a predetermined waveform of the ripple component based on a synchronous signal obtained from an AC power supplied to an input of the converter
25 unit.

14. A power converter according to any one of the preceding claims, wherein said control unit further includes means for controlling the output of said



34.

converter unit according to the control of the modulation rate of said inverter unit.

15. A power converter according to any one of the preceding claims, wherein said instruction includes a
5 signal indicative of a modulation rate for minimizing harmonic components of an output of said current-type inverter unit.

16. A power converter according to any one of the preceding claims, wherein said instruction includes a
10 signal indicative of a modulation rate for minimizing a specific harmonic component of an output of said current-type inverter unit.

17. A power converter according to any one of the preceding claims, wherein said instruction includes a
15 signal indicative of a modulation rate for minimizing the general value of harmonic components of an output of said current-type inverter unit.

18. A power converter according to any one of the preceding claims, wherein said instruction includes a
20 signal indicative of a condition of a load of said inverter unit.

19 A power converter according to claim 18, wherein said condition is an electric power required for the load and whether the modulation rate of the inverter
25 unit is to be controlled or not is determined depending on a magnitude of the electric power required for the load.

20. A power converter comprising:



35.

a) a converter unit for converting an AC power into a DC output power;

b) a current-type inverter unit connected through a DC circuit for converting the DC output
5 power of the inverter unit into an AC output power;

c) a DC reactor connected into the DC circuit connecting said converter unit to said inverter unit;

d) a first control unit for controlling said converter unit according to pulse width modulation
10 control; and

e) a second control unit for controlling an output frequency of the inverter unit according to pulse width modulation control, said second control unit including means for controlling a modulation rate
15 of said inverter unit according to an instruction applied to said second control unit.

21. A power converter according to claim 20, wherein said instruction includes a signal indicative of a ripple component of the DC output power applied to
20 said inverter unit from said converter unit.

22. A power converter substantially as herein described with reference to and as illustrated in Figs 1 to 5, or Figs 6 to 8, or Fig 15, or Figs 16 and 17 of the accompanying drawings.
