(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 August 2005 (18.08.2005)

PCT

(10) International Publication Number
WO 2005/076349 A1

(51) International Patent Classification[7]: H01L 21/768

(21) International Application Number:
PCT/US2004/043912

(22) International Filing Date:
30 December 2004 (30.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/769,522 30 January 2004 (30.01.2004) US

(71) Applicant *(for all designated States except US)*: **LAM REASEARCH CORPORATION** [US/US]; 4650 Cushing Parkway, Fremont, CA 94538 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **BAILEY III, Andrew, D.** [US/US]; 5167 Northway Road, Peasanton, CA 94566 (US). **LOHOKARE, Shrikant, P.** [US/US]; 35141 Woodbridge Place, Fremont, CA 94536 (US).

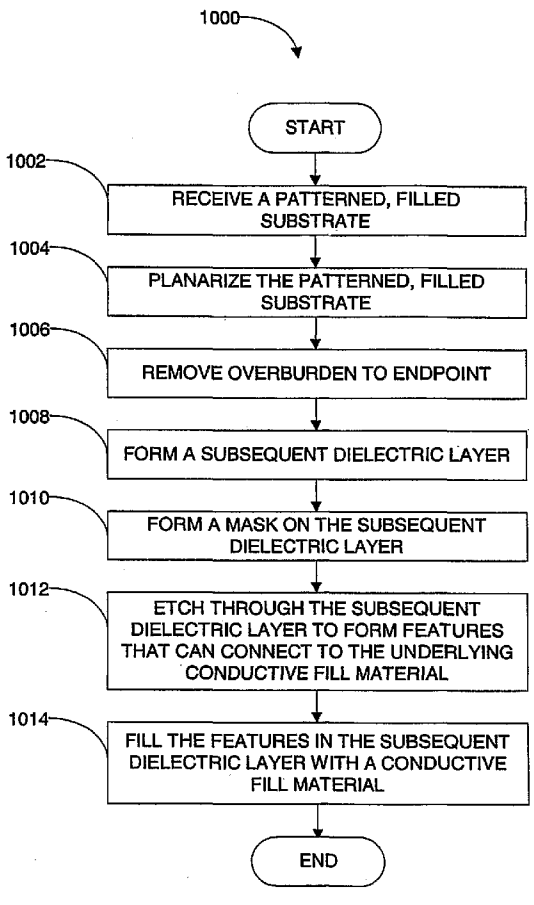
(74) Agent: **LEAVELL, George, B.**; Martine & Penilla & Gencarella, LLP, 710 Lakeway Drive, Suite 200, Sunnyvale, CA 94085 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR STRESS FREE CONDUCTOR REMOVAL



(57) Abstract: A system and method for forming a semiconductor in a dual damascene structure including receiving a patterned semiconductor substrate. The semiconductor substrate having a first conductive interconnect material filling multiple features (102,104,106) in the pattern. The first conductive interconnect material having an overburden portion (112). The over burden portion is planarized. The over burden portion is substantially entirely removed in the planarizing process. A mask layer is reduced and a subsequent dielectric layer (1130) is formed on the planarized over burden portion. A mask is formed on the subsequent dielectric layer. One or more features are formed in the subsequent dielectric layer and the features are filled with a second conductive interconnect material.

WO 2005/076349 A1

ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.