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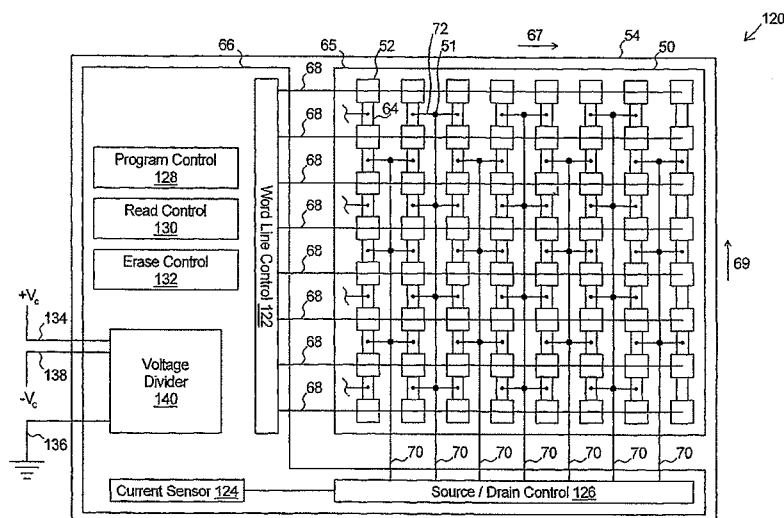
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(54) Title: MEMORY CELL ARRAY WITH STAGGERED LOCAL INTER-CONNECT STRUCTURE



(57) Abstract: A memory cell array (50) comprises a two dimensional array of memory cells (52) fabricated on a semiconductor substrate (54). The memory cells (52) are arranged in a plurality of rows defining a row direction (67) and a plurality columns defining a column direction (69). Each column of memory cells (52) comprising a plurality of alternating channel regions (58) and source/drain regions (64). A conductive interconnect (72) is positioned above each source/drain region (64) and coupled to only one other source/drain region (64). The one other source/drain region (64) is in a second column that is adjacent to the column. The conductive interconnects (64) are positioned such that every other conductive interconnect (64) connects to the adjacent column to a right side of the column and every other conductive interconnect connects to adjacent column to the left side of the column. A plurality of source/drain control lines (70) extends between adjacent columns of memory cells (52) and electrically couple to each conductive interconnect (72) that couples between the adjacent columns.

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