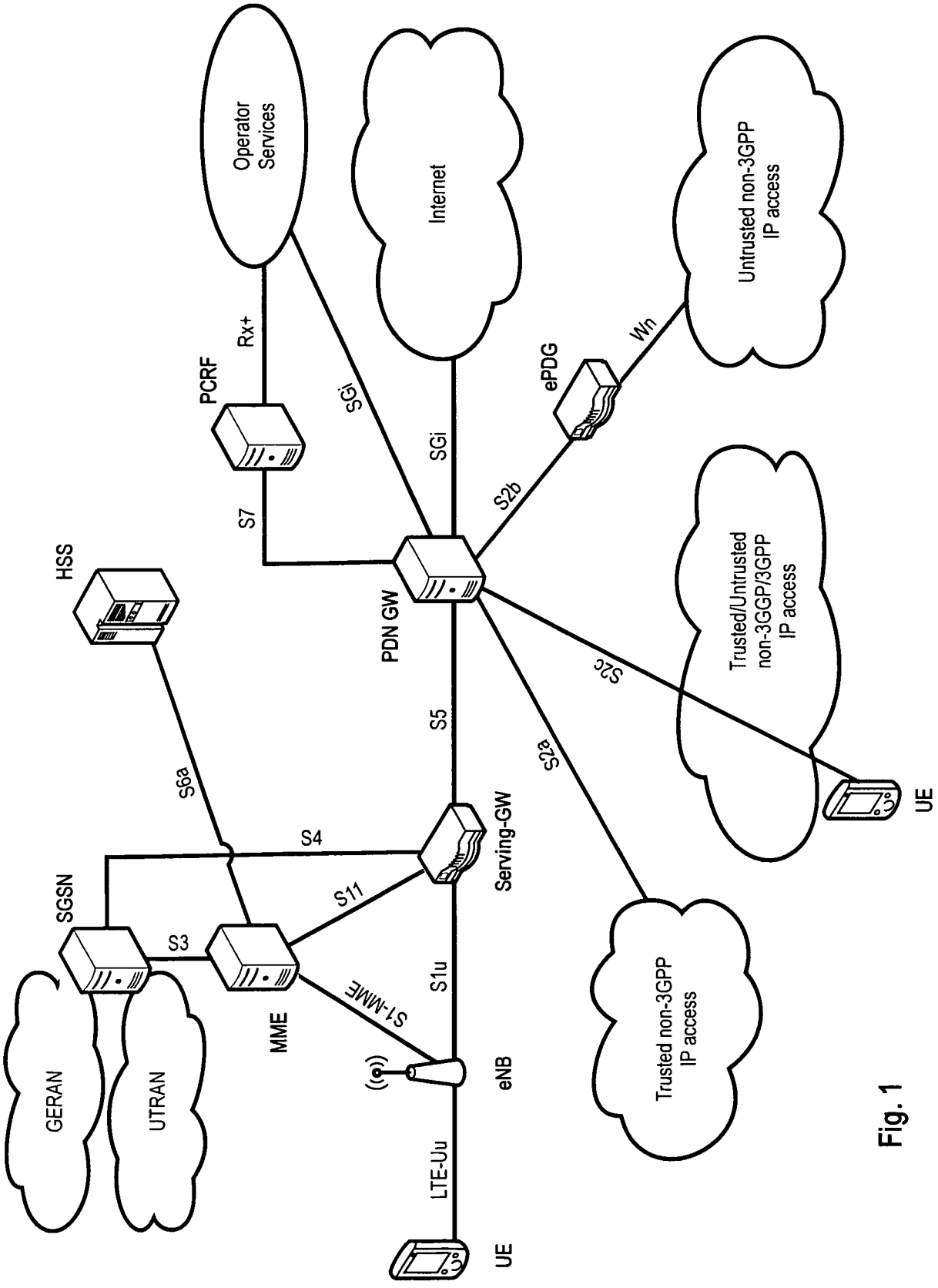

Operator Services
Internet
Untrusted non-3GPP IP access
PCRF
Rx+
SGi
SGi
ePDG
Wn
S7
S2b
HSS
PDN GW
Trusted/Untrusted non-3GGP/3GPP IP access
S2c
S5
S2a
S6a
UE
S4
Serving-GW
SGSN
S11
S3
S1u
S1-MME
MME
GERAN
UTRAN
eNB
Trusted non-3GPP IP access
LTE-Uu
UE

Fig. 1

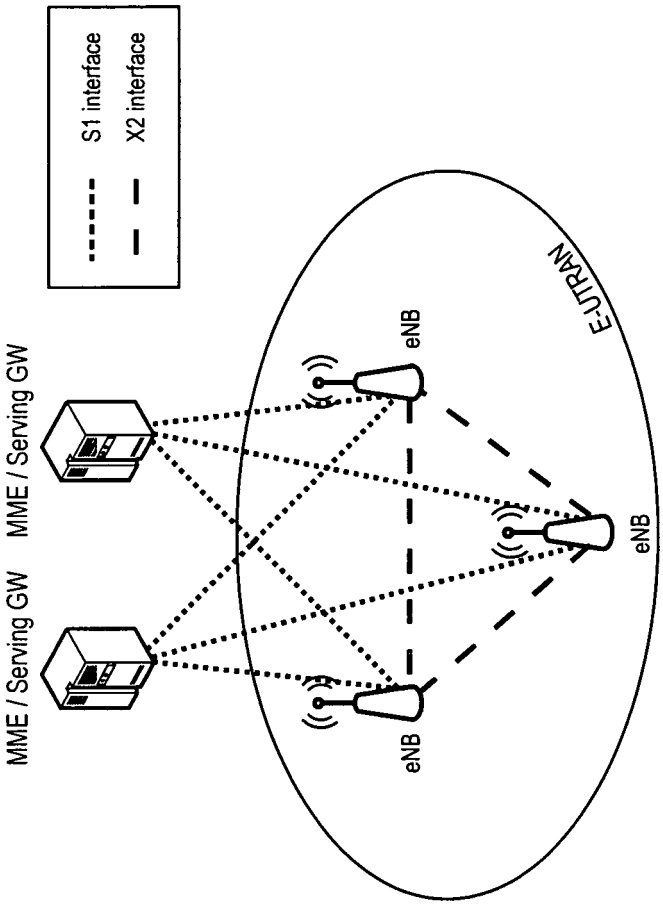

S1 interface
X2 interface
MME / Serving GW
MME / Serving GW
eNB
eNB
eNB
E-UTRAN

Fig. 2

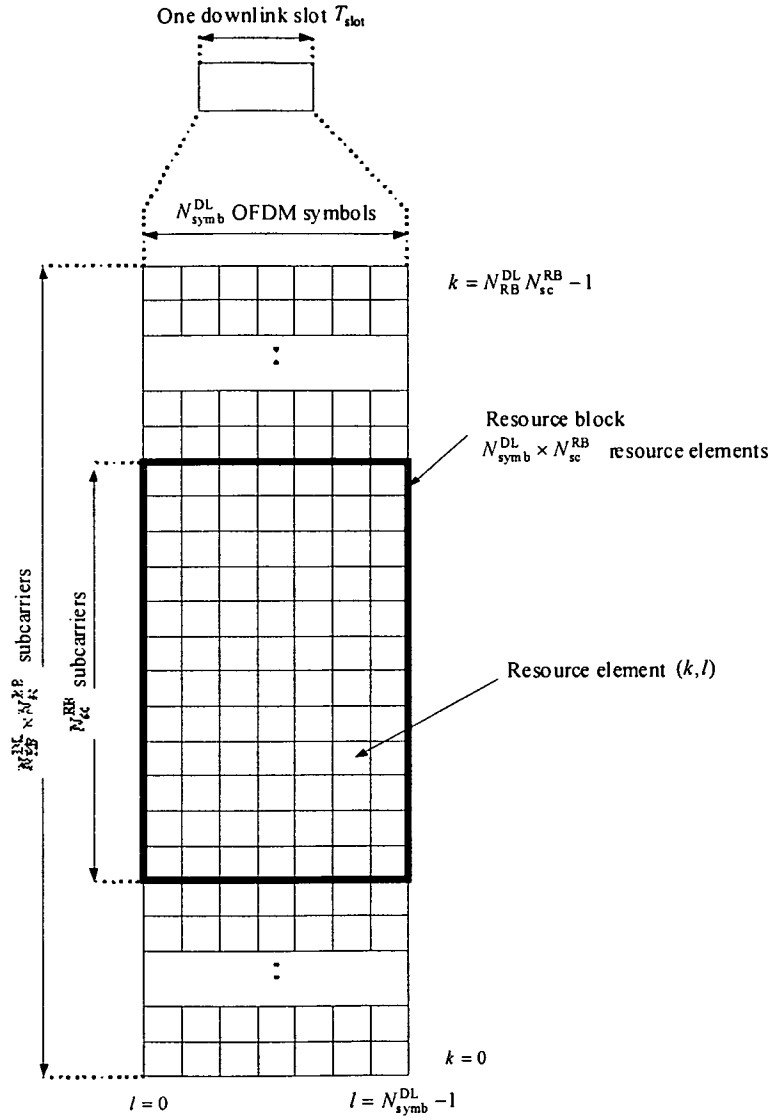

One downlink slot T_{slot}
N_{symb}^{DL} OFDM symbols
$k = N_{RB}^{DL} N_{sc}^{RB} - 1$
Resource block
$N_{symb}^{DL} \times N_{sc}^{RB}$ resource elements
Resource element (k,l)
$N_{RB}^{DL} \times N_{sc}^{RB}$ subcarriers
N_{sc}^{RB} subcarriers
$k = 0$
$l = 0$
$l = N_{symb}^{DL} - 1$

Fig. 3

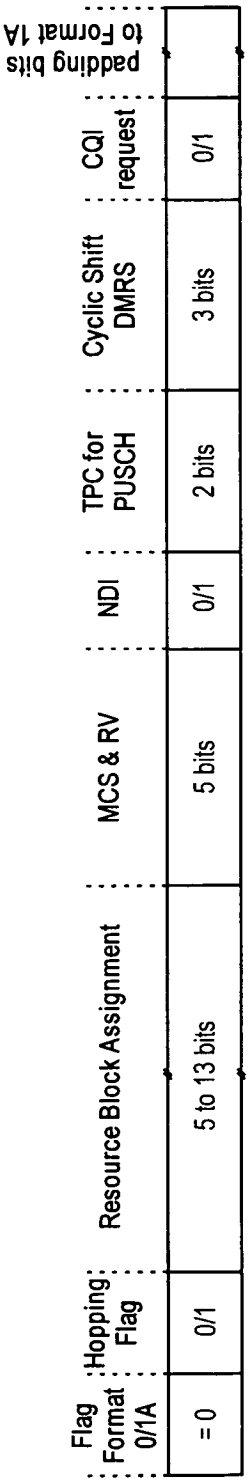

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
0/1

Fig. 4

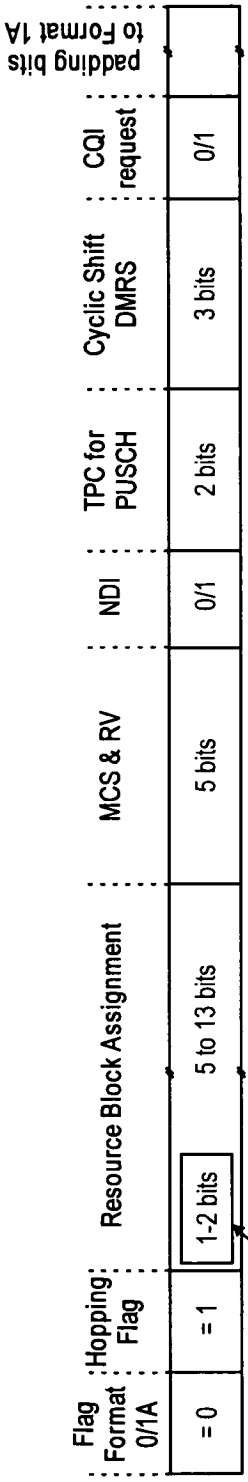

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
= 1
1-2 bits
5 to 13 bits
5 bits
0/1
2 bits
3 bits
0/1
Hopping Configuration Bits

Fig. 7

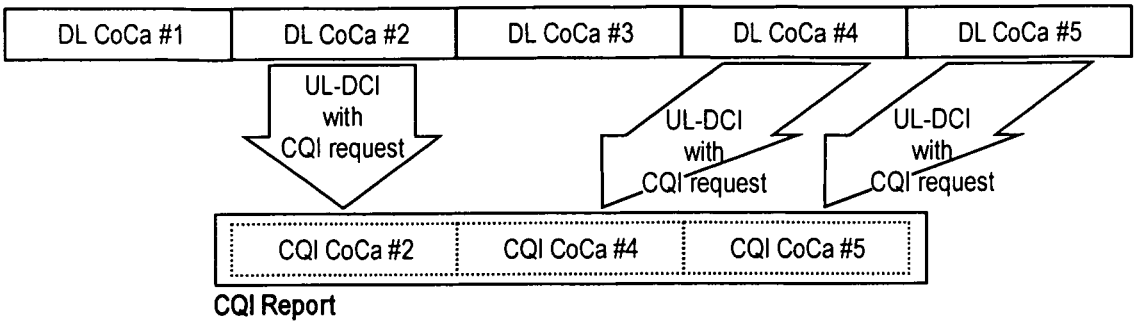

DL CoCa #1
DL CoCa #2
DL CoCa #3
DL CoCa #4
DL CoCa #5
UL-DCI with CQI request
UL-DCI with CQI request
UL-DCI with CQI request
CQI CoCa #2
CQI CoCa #4
CQI CoCa #5
CQI Report

Fig. 5

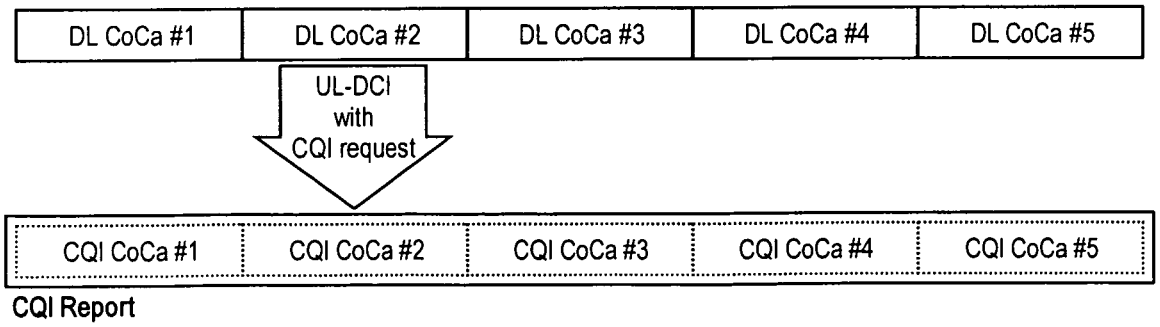

DL CoCa #1
DL CoCa #2
DL CoCa #3
DL CoCa #4
DL CoCa #5
UL-DCI with CQI request
CQI CoCa #1
CQI CoCa #2
CQI CoCa #3
CQI CoCa #4
CQI CoCa #5
CQI Report

Fig. 6

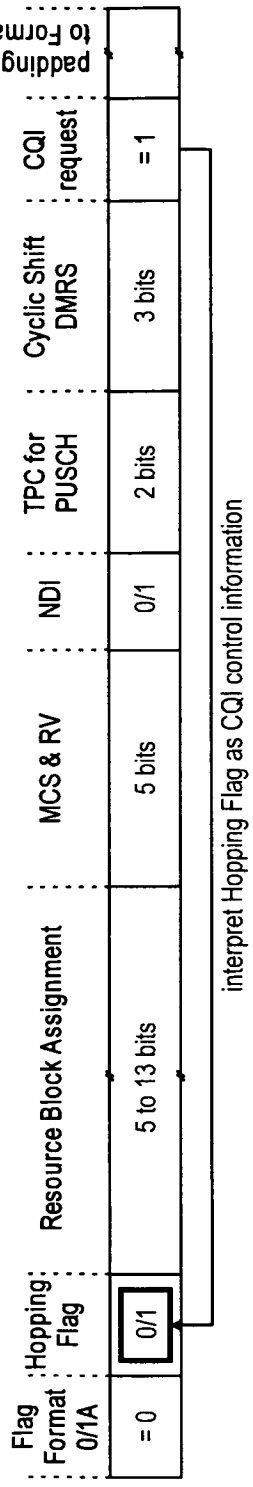

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1
interpret Hopping Flag as CQI control information

Fig. 8

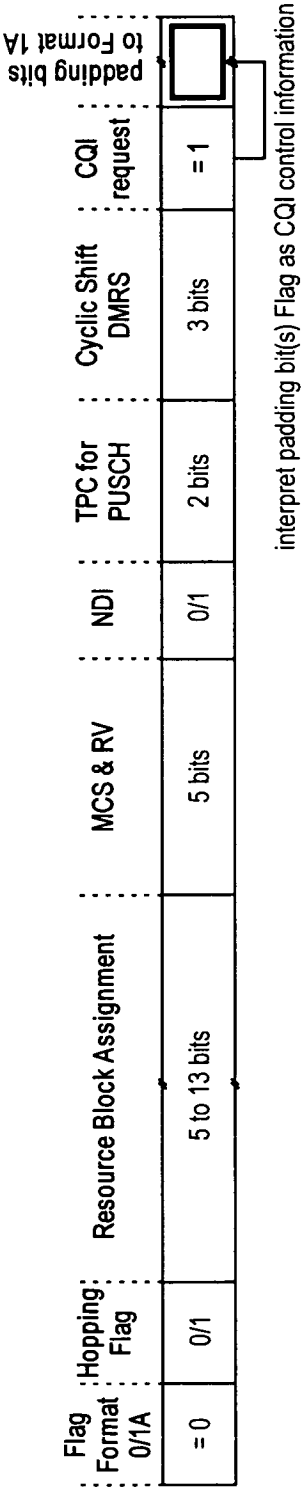

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1
interpret padding bit(s) Flag as CQI control information

Fig. 9

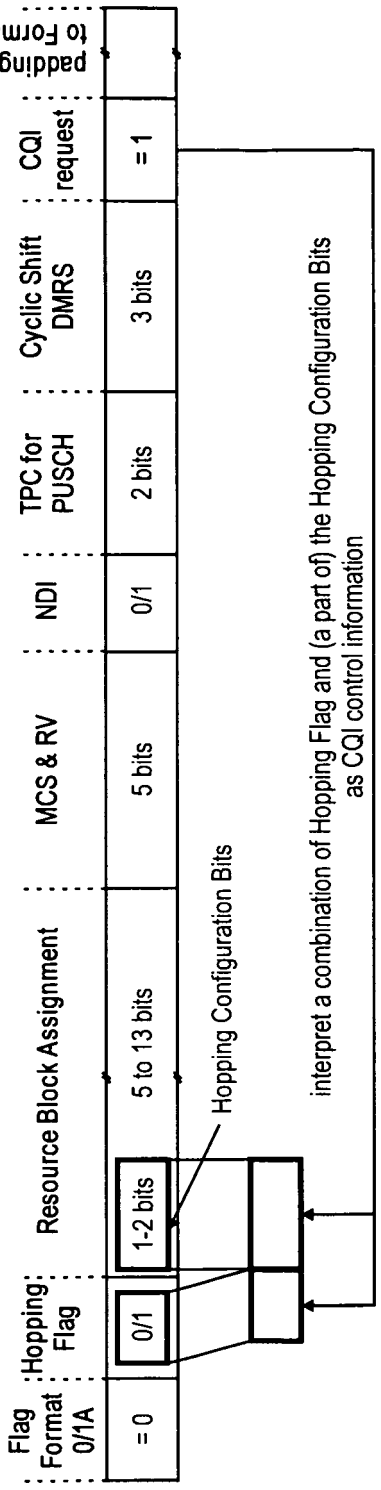

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
1-2 bits
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1
Hopping Configuration Bits
interpret a combination of Hopping Flag and (a part of) the Hopping Configuration Bits as CQI control information

Fig. 10

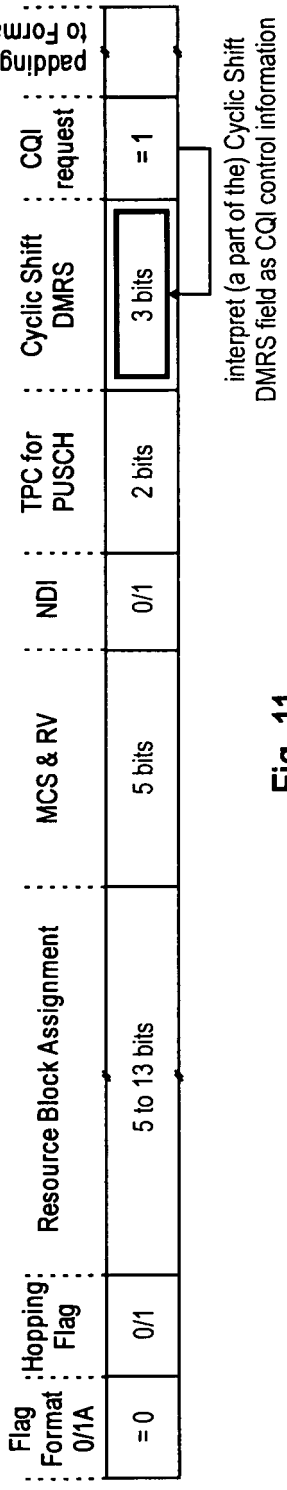

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1
interpret (a part of the) Cyclic Shift DMRS field as CQI control information

Fig. 11


Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1
interpret a combination of the Hopping Flag and (a part of the) Cyclic Shift DMRS field as CQI control information

Fig. 12

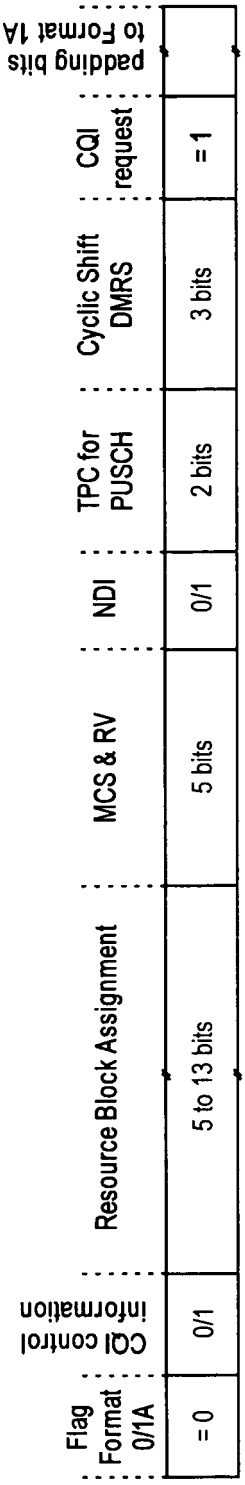

Flag Format 0/1A
CQI control information
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1

Fig. 13

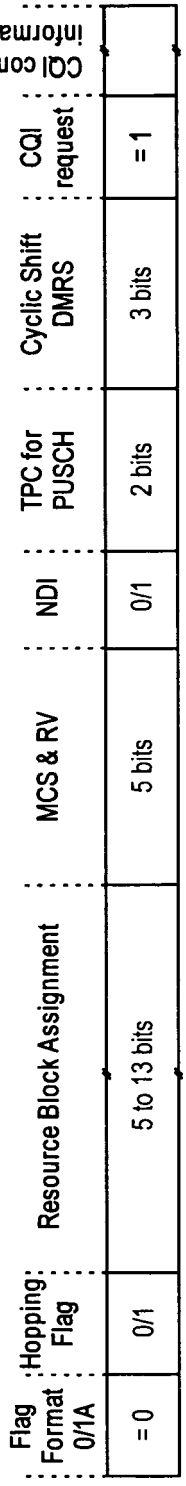

Flag Format 0/1A
Hopping: Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
CQI control information
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1

Fig. 14

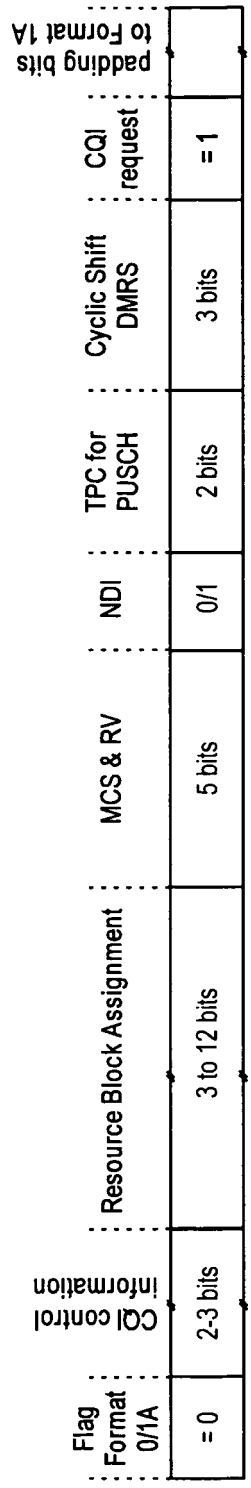

Flag Format 0/1A
CQI control information
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
2-3 bits
3 to 12 bits
5 bits
0/1
2 bits
3 bits
= 1

Fig. 15

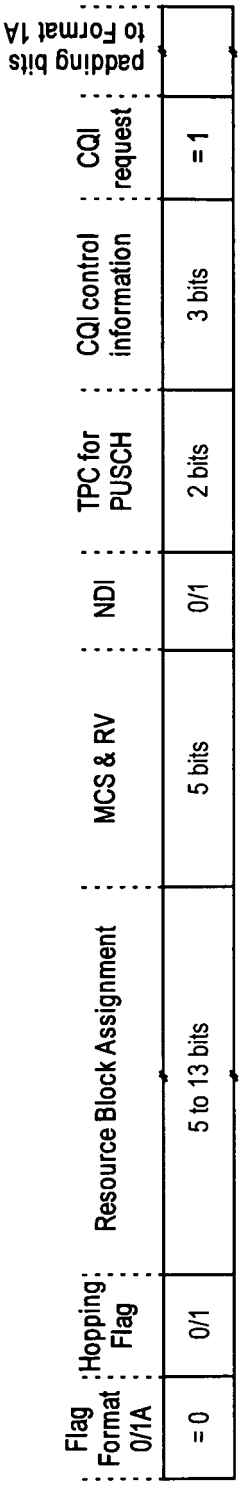

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
CQI control information
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1

Fig. 16

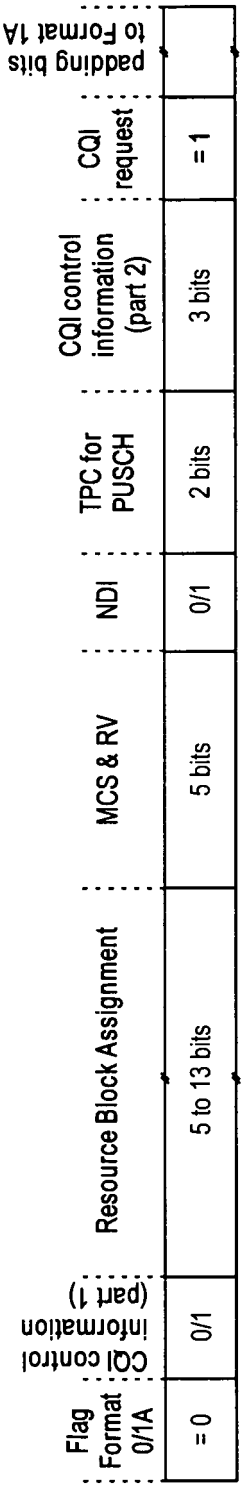

Flag Format 0/1A
CQI control information (part 1)
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
CQI control information (part 2)
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
= 1

Fig. 17

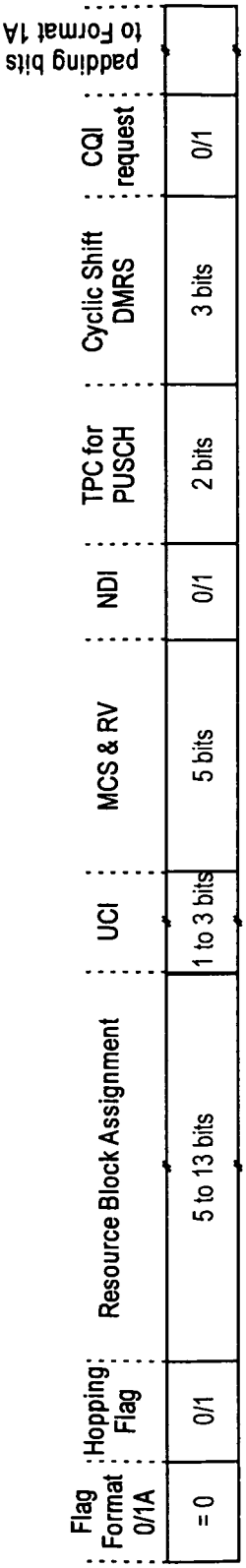

Flag Format 0/1A
Hopping Flag
Resource Block Assignment
UCI
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
= 0
0/1
5 to 13 bits
1 to 3 bits
5 bits
0/1
2 bits
3 bits
0/1

Fig. 19

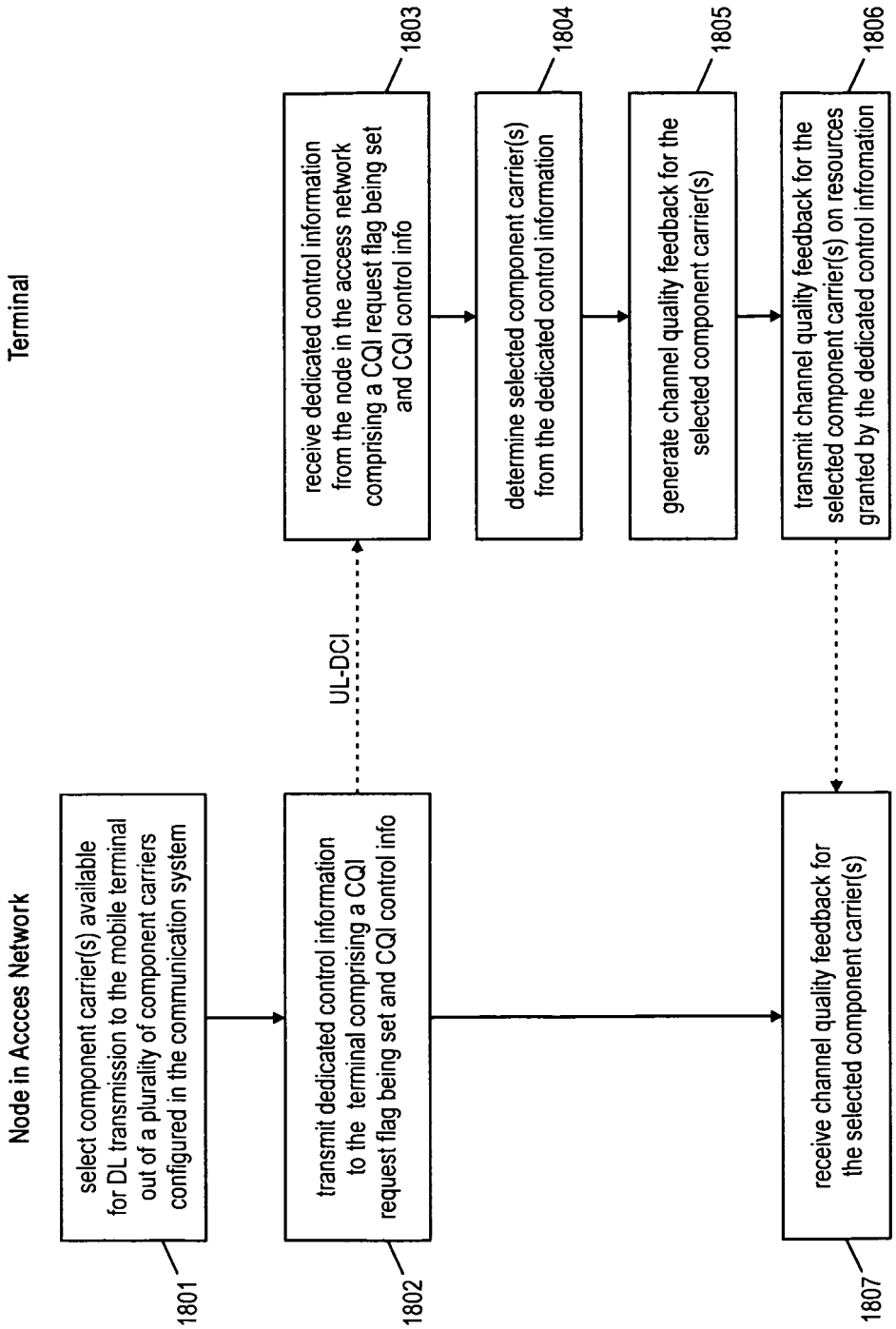

Node in Accces Network
Terminal
select component carrier(s) available for DL transmission to the mobile terminal out of a plurality of component carriers configured in the communication system
1801
transmit dedicated control information to the terminal comprising a CQI request flag being set and CQI control info
1802
UL-DCI
receive dedicated control information from the node in the access network comprising a CQI request flag being set and CQI control info
1803
determine selected component carrier(s) from the dedicated control information
1804
generate channel quality feedback for the selected component carrier(s)
1805
transmit channel quality feedback for the selected component carrier(s) on resources granted by the dedicated control infromation
1806
receive channel quality feedback for the selected component carrier(s)
1807

Fig. 18

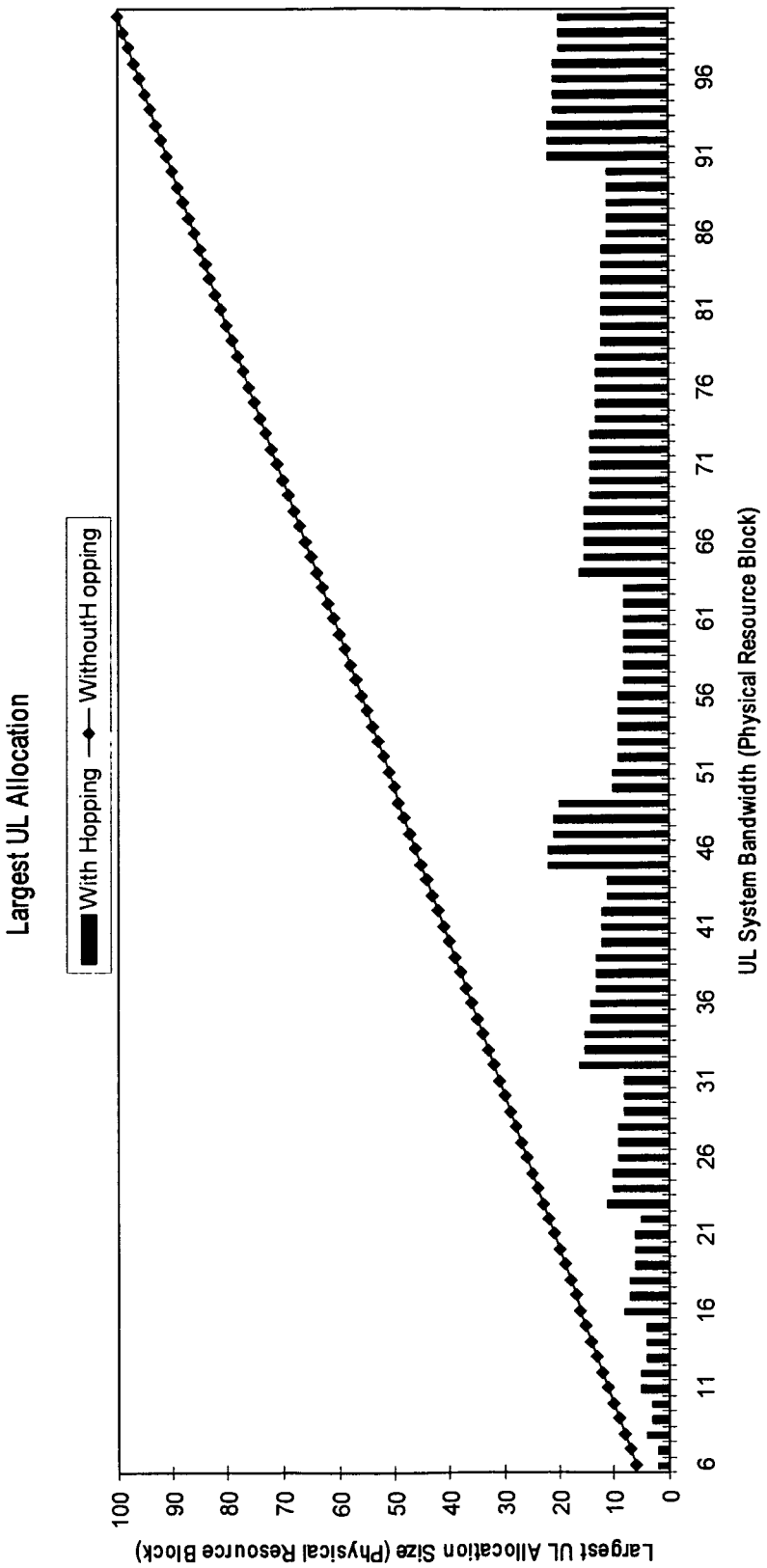

Largest UL Allocation
With Hopping
WithoutH opping
Largest UL Allocation Size (Physical Resource Block)
UL System Bandwidth (Physical Resource Block)
0
10
20
30
40
50
60
70
80
90
100
6
11
16
21
26
31
36
41
46
51
56
61
66
71
76
81
86
91
96

Fig. 20

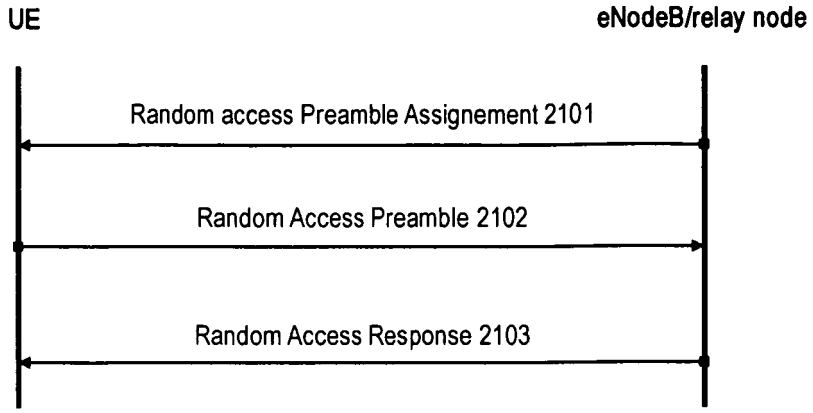

UE
eNodeB/relay node
Random access Preamble Assignement 2101
Random Access Preamble 2102
Random Access Response 2103

Fig. 21

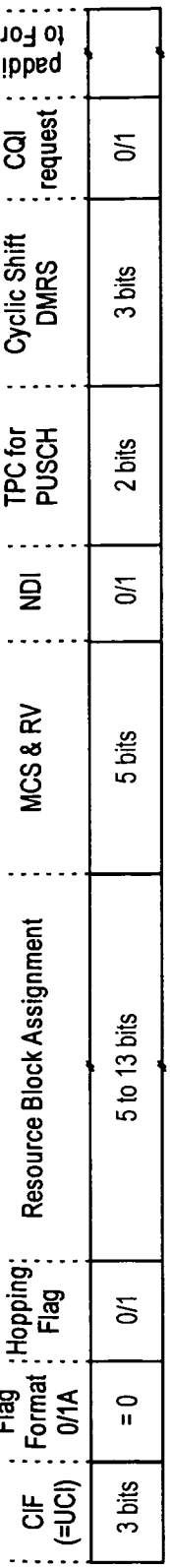

CIF (=UCI)
Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
CQI request
padding bits to Format 1A
3 bits
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits
0/1

Fig. 22

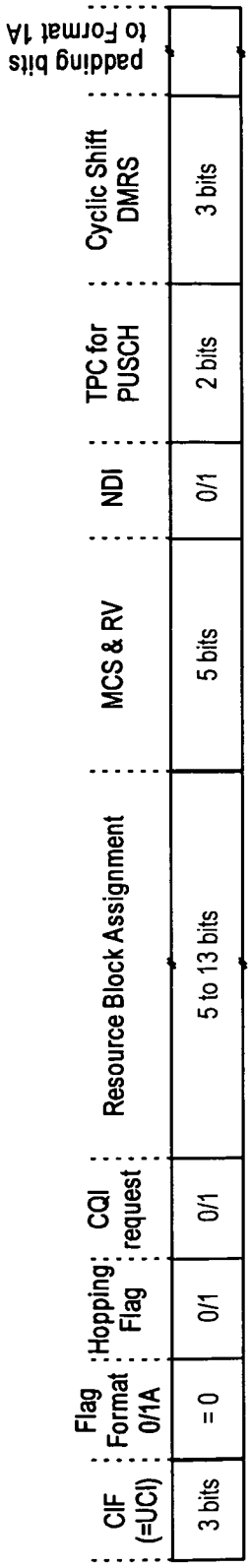

CIF (=UCI)
Flag Format 0/1A
Hopping Flag
Resource Block Assignment
MCS & RV
NDI
TPC for PUSCH
Cyclic Shift DMRS
padding bits to Format 1A
3 bits
= 0
0/1
5 to 13 bits
5 bits
0/1
2 bits
3 bits

Fig. 23