

CLAIMS

1. Method for directly depositing palladium onto a non-activated surface of a gallium nitride semiconductor, comprising in this order the steps:

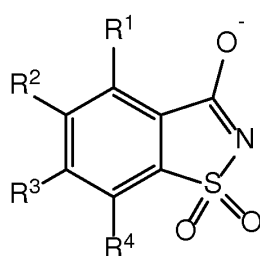
(i) providing a doped or non-doped gallium nitride semiconductor with a non-activated surface,

(ii) providing an aqueous, acidic palladium plating bath, comprising

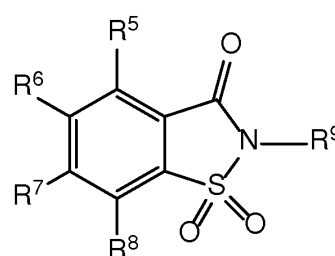
(a)  $\text{Pd}^{2+}$  ions,

(b) one or more than one reducing agent suitable to reduce  $\text{Pd}^{2+}$  ions to metallic  $\text{Pd}^0$ ,

(c) one or more than one compound selected from the group consisting of compounds of formulae (I) and (II)



(I)



(II),

wherein  $\text{R}^1$ ,  $\text{R}^2$ ,  $\text{R}^3$ ,  $\text{R}^4$ ,  $\text{R}^5$ ,  $\text{R}^6$ ,  $\text{R}^7$ , and  $\text{R}^8$  are independently H, alkyl, aryl, hetero aryl,  $\text{NH}_2$ ,  $\text{SO}_3\text{H}$ , or OH, and

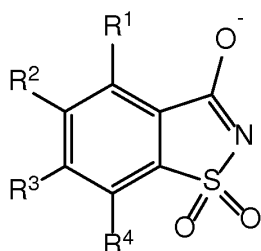
$\text{R}^9$  is independently H, alkyl, aryl, or hetero aryl,

(iii) contacting the semiconductor with the plating bath such that metallic palladium or a palladium alloy is electrolessly deposited onto the non-activated surface of the semiconductor, the plating bath temperature being in the range of from 70°C to 99°C.

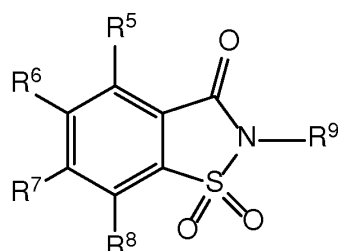
2. Method according to claim 1, wherein the surface of the semiconductor is not contacted with or does not comprise  $\text{Sn}^{2+}$  ions prior to step (iii) or when step (iii) is carried out, preferably is not contacted with or does not comprise tin ions or tin atoms prior to step (iii) or when step (iii) is carried out, more preferably is not contacted with or does not comprise activation metal ions or activation metal atoms prior to step (iii) or when step (iii) is carried out.

3. Method according to any of the aforementioned claims comprising the additional step prior to step (iii)
- cleaning the non-activated surface with a cleaning solution, the cleaning solution preferably comprising one or more than one ingredient selected from the group consisting of acids, bases, oxidizing agents, halogen ions, and organic solvents.
4. Method according to any of the aforementioned claims, wherein the pH of the acidic palladium plating bath is in the range of from 4.0 to 6.5, preferably from 5.3 to 6.3.
5. Method according to any of the aforementioned claims, wherein (c) is one or more than one compound of formula (I), preferably is a compound of formula (I), wherein  $R^1$ ,  $R^2$ ,  $R^3$ , and  $R^4$  is H.
6. Method according to any of the aforementioned claims, wherein the palladium plating bath additionally contains
- (d) one or more than one complexing compound selected from the group consisting of amines,
- preferably selected from the group consisting of primary amines, and secondary amines,
- more preferably selected from the group consisting of ethylenediamine, 1,3-diaminopropane, 1,2-bis(3-aminopropylamino)ethane, 2-diethylaminoethylamine, diethylenetriamine, diethylenetriaminepentacetic acid, nitroacetic acid, N-(2-hydroxyethyl)ethylenediamine, ethylenediamine-N,N-diacetic acid, 2-(dimethylamino)ethylamine, 1,2-diamino-propylamine, 1,3-diaminopropylamine, 3-(methylamino)-propylamine, 3-(dimethylamino)propylamine, 3-(diethylamino)propylamine, bis-(3-aminopropyl)amine, 1,2-bis-(3-aminopropyl)alkylamine, diethylenetriamine, triethylenetetramine, tetraethylenepentamine, and pentaethylenhexamine.
7. Method according to any of the aforementioned claims, wherein in step (iii) the semiconductor and the plating bath are in contact for 10 to 1200 seconds, preferably for 30 to 800 seconds, more preferably for 60 to 400 seconds.
8. Method according to any of the aforementioned claims, wherein the plating bath temperature in step (iii) is in the range of from 70°C to 95°C, preferably in the range of from 75°C to 95°C, more preferably in the range of from 79°C to 91°C.

9. Method according to any of the aforementioned claims, wherein the deposited palladium and palladium alloy has a total layer thickness in the range of from 10 nm to 1000 nm, more preferably 50 nm to 400 nm, most preferably 100 nm to 300 nm.
10. Method according to any of the aforementioned claims, wherein the metallic palladium or palladium alloy is selectively deposited onto the non-activated surface such that a palladium pattern or palladium alloy pattern is obtained on the surface of the semiconductor.
11. Method according to any of the aforementioned claims comprising after step (iii) the additional step
  - (iv) depositing an additional metal layer or metal alloy layer onto the electrolessly deposited metallic palladium/palladium alloy obtained after step (iii), preferably by electroless deposition.
12. Use of an aqueous, acidic palladium plating bath, comprising
  - (a)  $\text{Pd}^{2+}$  ions,
  - (b) one or more than one reducing agent suitable to reduce  $\text{Pd}^{2+}$  ions to metallic  $\text{Pd}^0$ ,
  - (c) one or more than one compound selected from the group consisting of compounds of formulae (I) and (II)



(I)



(II),

wherein  $\text{R}^1$ ,  $\text{R}^2$ ,  $\text{R}^3$ ,  $\text{R}^4$ ,  $\text{R}^5$ ,  $\text{R}^6$ ,  $\text{R}^7$ , and  $\text{R}^8$  are independently H, alkyl, aryl, hetero aryl,  $\text{NH}_2$ ,  $\text{SO}_3\text{H}$ , or OH, and

$\text{R}^9$  is independently H, alkyl, aryl, or hetero aryl,

for directly and electrolessly depositing metallic palladium or a palladium alloy onto a non-activated surface of a doped or non-doped gallium nitride semiconductor.

13. Palladium or palladium alloy coated, doped or non-doped gallium nitride semiconductor obtained through the method defined in any of claims 1 to 11.

14. Palladium or palladium alloy coated, doped or non-doped gallium nitride semiconductor with an interface between the coated palladium or palladium alloy and the doped or non-doped gallium nitride semiconductor, wherein
- the palladium and palladium alloy is wet chemically deposited, and
  - 5       - the interface does not contain tin ions, tin atoms, or tin containing compounds, preferably does not contain activation metal ions, activation metal atoms, or activation metal containing compounds.
15. Semiconductor according to claim 14, wherein the deposited palladium and palladium alloy has a total layer thickness in the range of from 10 nm to 1000 nm, more
- 10       preferably 50 nm to 400 nm, most preferably 100 nm to 300 nm.