

**BOARD-ON-CHIP TYPE SUBSTRATES WITH CONDUCTIVE TRACES
IN MULTIPLE PLANES, SEMICONDUCTOR DEVICE PACKAGES
INCLUDING SUCH SUBSTRATES, AND ASSOCIATED METHODS**

ABSTRACT OF THE DISCLOSURE

A method for fabricating a chip-scale board-on-chip substrate, or redistribution element, includes forming conductive planes on opposite sides of a substrate. A first of the conductive planes includes two sets of bond fingers, conductive traces that extend
5 from a first set of the bond fingers, and two sets of redistributed bond pads, including a first set to which the conductive traces lead. The second conductive plane includes conductive traces that extend from locations that are opposite from the second set of bond fingers toward locations that are opposite from the locations of the second set of redistributed bond pads. Conductive vias are formed through the second set of bond
10 fingers to the conductive traces of the second conductive plane. In addition, conductive vias are also formed to electrically connect the conductive vias of the second conductive plane to their corresponding redistributed bond pads in the first conductive plane. Redistribution elements including these features, as well as semiconductor device assemblies including the redistribution elements and assembly methods, are also
15 disclosed.

Figure 3