

## **METHOD APPLIED TO PLASMA SYSTEM AND RELATED PLASMA SYSTEM**

### **TECHNICAL FIELD**

5           The present disclosure relates to an operation method, and more particularly, to a method applied to a plasma system and a related plasma system.

### **BACKGROUND**

10           With continuously reduced sizes of features in the integrated circuit, more and more strict processing technologies are required. One of the important requirements is the consistency in product etching. During the technological process, strict requirements are put on the consistency in the technological results from all chambers of machine tables of the same type, as to avoid technological risks caused by the consistency problem among the chambers. Therefore, the consistency in the  
15           technological results among different chambers needs to be achieved through strict process control. In the actual controlling process, differences in etching results caused by differences in uncontrollable distribution parameters such as the lower electrode routing form still exist, and are further enlarged particularly in an advanced process.

### **SUMMARY**

20           Therefore, the present disclosure discloses a method applied to a plasma system and a related plasma system for solving at least one of the problems mentioned in the background part.

          According to an embodiment of the disclosure, there is provided a method  
25           applied to a plasma system. The plasma system has a chamber, a lower electrode disposed in the chamber, and a radio frequency source coupled to the lower electrode via a matching circuit. The plasma system is configured to process a workpiece placed on the lower electrode. The method includes: starting the radio frequency source; increasing a radio frequency power of the radio frequency source, and generating an  
30           output power at the lower electrode through the matching circuit that is at a default

position; and adjusting, when a first condition is met, the radio frequency power with a first trend, and adjusting, with a second trend involving increasing a ratio of the output power to the radio frequency power, the matching circuit to meet a second condition.

5        According to an embodiment of the disclosure, there is provided a method applied to a plasma system. The plasma system has a chamber, a lower electrode disposed in the chamber, and a radio frequency source coupled to the lower electrode via a matching circuit. The plasma system is configured to process a workpiece placed on the lower electrode. The method includes: starting the radio frequency source to  
10    generate a radio frequency power; increasing the radio frequency power of the radio frequency source, the radio frequency power generating an output power at the lower electrode through the matching circuit that is at a default position; and adjusting, when a DC voltage detected by a sensor coupled to the workpiece reaches a default voltage or the radio frequency power reaches a maximum radio frequency power, the  
15    matching circuit to increase a ratio of the output power to the radio frequency power.

      According to an embodiment of the disclosure, there is provided a plasma system configured to process a workpiece placed in a chamber. The plasma system includes a lower electrode, a radio frequency source, a matching circuit and a control circuit. The lower electrode is disposed in the chamber; the radio frequency source is coupled to  
20    the lower electrode; and the matching circuit is coupled between the radio frequency source and the lower electrode. When the radio frequency source is started to generate a radio frequency power, an output power is generated at the lower electrode through the matching circuit that is at a default position. The control circuit is coupled to the radio frequency source and the matching circuit. The control circuit is configured to  
25    control the radio frequency source to increase the radio frequency power until a first condition is met, and then adjust the radio frequency power with a first trend, and adjust, with a second trend involving increasing a ratio of the output power to the radio frequency power, the matching circuit to meet a second condition.

## 30    **BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a schematic diagram of a plasma system according to an embodiment of the disclosure.

FIG. 2 is a schematic diagram of a matching circuit according to an embodiment of the disclosure.

5        FIG. 3 is a first partial flowchart of a method applied to a plasma system according to an embodiment of the disclosure.

FIG. 4A is a waveform diagram according to the first partial flowchart of the method shown in FIG. 3.

10       FIG. 4B is another waveform diagram according to the first partial flowchart of the method shown in FIG. 3.

FIG. 5 is a second partial flowchart of a method applied to a plasma system according to an embodiment of the disclosure.

FIG. 6A is a waveform diagram according to the second partial flowchart of the method shown in FIG. 5.

15       FIG. 6B is another waveform diagram according to the second partial flowchart of the method shown in FIG. 5.

FIG. 7A is a waveform diagram according to the embodiment of FIG. 4A.

FIG. 7B is a waveform diagram according to the embodiment of FIG. 4B.

FIG. 7C is another waveform diagram according to the embodiment of FIG. 4B.

20       FIG. 8 is a flowchart of a method applied to a plasma system according to another embodiment of the disclosure.

FIG. 9A is a waveform diagram according to the flowchart of the method shown in FIG. 8.

25       FIG. 9B is another waveform diagram according to the flowchart of the method shown in FIG. 8.

## **DETAILED DESCRIPTION**

The following disclosure provides various implementations or examples that can be used to implement various features of the disclosure. The specific embodiments of components and configurations described below are provided to simplify the present

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disclosure. It is to be understood that such descriptions are merely illustrative and are not intended to limit the present disclosure. For example, in the following description, forming a first feature on or over a second feature in certain embodiments may include that the first and second features are in direct contact with each other; and in  
5 other certain embodiments may also include that an additional component is formed between the first and second features so that the first and second features may not be in direct contact. In addition, the present disclosure may use the same reference signs and/or numbers in various embodiments for brevity and clarity purposes, which do not represent a relationship between the various embodiments and /or configurations  
10 discussed.

Furthermore, spatially relative terms, such as "under", "below", "over", "above", and the like, may be used herein for convenience in describing the relationship of one element or feature to another element or feature illustrated in the figures. These spatially relative terms are intended to encompass a variety of different orientations of  
15 the device in use or operation in addition to the orientation depicted in the figures. The device may be otherwise oriented (e.g., rotated 90 degrees or at other orientations) and the spatially relative terms should be interpreted accordingly.

Although numerical ranges and parameters setting forth the broad scope of the application are approximations, the numerical values set forth in the specific  
20 embodiments are reported as precisely as possible. Any numerical value, however, inherently contains certain errors necessarily resulting from the individual testing methods. As used herein, "about" generally refers to actual values within 10%, 5%, 1%, or 0.5% of a particular value or range. Alternatively, the term "about" indicates that the actual value falls within the acceptable standard error of the mean, subject to  
25 consideration by those of ordinary skill in the art to which this application pertains. It should be understood that all ranges, amounts, values and percentages herein used (e.g., to describe amounts of materials, length of time, temperature, operating conditions, ratio of amounts, and the like) are modified by "about" in addition to the experimental examples, or unless otherwise expressly stated. Accordingly, unless  
30 indicated to the contrary, the numerical parameters set forth in the specification and

attached claims are approximations that may vary depending upon the desired properties sought to be obtained. At the very least, these numerical parameters are to be understood as meaning the number of significant digits and the number resulting from applying ordinary rounding techniques. Herein, numerical ranges are expressed from one end to the other or between the two ends; unless otherwise indicated, all numerical ranges recited herein are inclusive of the endpoints.

When a plasma system processes, for example, etches a workpiece (e.g., a wafer), a voltage bias on the workpiece (e.g., the wafer) is required to be detected in real time, and in order to achieve consistency in the process results on the workpiece (e.g., the wafer), the voltage bias on the workpiece (e.g., the wafer) is required to be controlled to remain constant during the processing. If the voltage bias on the workpiece (e.g., the wafer) takes a very long time to reach the default voltage bias, the unstable voltage bias may cause a processing result of the workpiece (e.g., the wafer) less than the expected, thereby greatly reducing the yield. Therefore, how to quickly adjust the voltage bias on the workpiece (e.g., the wafer) to the default voltage bias and maintain it constant is a major challenge to achieve the consistency in process results. The present disclosure provides a method applied to a plasma system and a related plasma system, which can quickly adjust a voltage bias on a workpiece (e.g., a wafer) to a default voltage bias and avoid the situation where the voltage bias on the workpiece (e.g., the wafer) takes a very long time to reach the default voltage bias. The method and the plasma system provided by the disclosure can effectively improve the production yield of workpieces (e.g., wafers) and reduce energy loss.

FIG. 1 is a schematic diagram of a plasma system 1 according to an embodiment of the disclosure. In the embodiment, the plasma system 1 is configured to process a workpiece (e.g., a wafer). The plasma system 1, for example, may be an etching device that etches the workpiece (e.g., the wafer) using plasma. As shown in FIG. 1, the plasma system 1 includes a chamber 10, a lower electrode 11 disposed in the chamber 10, a radio frequency power supply 12, a matching circuit 13, a sensor 14, and a control circuit 15. The workpiece (e.g., the wafer) is placed on the lower electrode 11 for processing. The radio frequency power supply 12 is coupled to the

lower electrode 11 via the matching circuit 13. The radio frequency power supply 12 is configured to provide a radio frequency power RFp that forms an output power OUTp at the lower electrode 11 after passing through a matcher in the matching circuit 13.

5 By adjusting a position of the matcher in the matching circuit 13, the matching circuit 13 may have different impedances. When the impedance of the matching circuit 13 is impedance-matched with the output impedance (e.g., 50  $\Omega$ ) of the radio frequency power supply 12, the impedance of the transmission line between the radio frequency power supply 12 and the matching circuit 13, the impedance of the lower  
10 electrode 11, and the impedance formed by the plasma in the chamber 10, a minimum reflected power of the matching circuit 13 to the radio frequency power RFp is obtained, and in this case, the ratio of the output power OUTp to the radio frequency power RFp is at the maximum.

As will be understood by those ordinary skilled in the art, in order to realize  
15 precise impedance-matching, an amplitude/phase detection circuit (not shown) may be provided between the radio frequency power supply 12 and the matching circuit 13. The amplitude/phase detection circuit is configured to obtain a modulus and a phase of the impedance as viewed from an input end of the matching circuit 13 to the chamber 10, and to provide an input amount required by a matching control algorithm  
20 to the control circuit 15, where the control circuit 15 adjusts the matching circuit 13 to finally match the total impedance of the matching circuit 13 and the chamber 10 to the output impedance (e.g., 50  $\Omega$ ) of the radio frequency power supply 12, thereby achieving impedance matching.

The sensor 14 is coupled to the lower electrode 11 to detect a radio frequency  
25 voltage above the workpiece (e.g., the wafer) in real time, convert the radio frequency voltage into a DC bias voltage (BIAS), and output the DC bias voltage (BIAS). The control circuit 15 receives the DC bias voltage (BIAS), and adjusts the radio frequency power RFp of the radio frequency power supply 12 or the position of the matcher in the matching circuit 13 in real time according to the DC bias voltage  
30 (BIAS) and a default voltage. The default voltage may be pre-stored in a storage

device (not shown) in the plasma system 1, such as a memory. After reading the default voltage from the storage device, the control circuit 15 compares the default voltage with the DC bias voltage (BIAS) to adjust the radio frequency power RFp of the radio frequency power supply 12 or the position of the matcher in the matching circuit 13 in real time. In detail, the control circuit 15 may read data and/or parameters in the radio frequency power supply 12 and the matching circuit 13 in real time, and determine how to adjust the radio frequency power supply 12 and the matching circuit 13 according to the radio frequency power RFp and the position of the matcher in the matching circuit at the same time point in the data.

As will be understood by those ordinary skilled in the art, the plasma system 1 may further include other devices and components necessary to accomplish the processing of a workpiece (e.g., a wafer). For example, the plasma system 1 includes an upper radio frequency power supply, a matching circuit corresponding to the upper radio frequency power supply, and a coil, and further includes a pipeline for introducing a reactant gas, etc. However, for simplicity of illustration, FIG. 1 only depicts the devices and components related to the inventive spirit of the present disclosure.

FIG. 2 is a schematic diagram of a matching circuit 13 according to an embodiment of the disclosure. As shown in FIG. 2, the matching circuit 13 includes variable capacitors C1 and C2 and inductors L1 and L2. The variable capacitor C1 and the inductor L1 are connected in series to form a tuning circuit, while the variable capacitor C2 and the inductor L2 are connected in series to form another tuning circuit. In detail, one end of the inductor L1 is connected to the radio frequency power supply 12 and the other end thereof is connected to one end of the variable capacitor C1, while the other end of the variable capacitor C1 is connected to the lower electrode 11; and one end of the variable capacitor C2 is connected to the radio frequency power supply 12 and the other end thereof is connected to one end of the inductor L2, while the other end of the inductor L2 is connected to a reference power supply terminal (e.g., a ground terminal). As will be understood by those ordinary skilled in the art, the positions of the capacitor and the inductor in the tuning circuit are not limited, as

long as the function and purpose of the tuning circuit can be achieved by connecting the capacitor and the inductor in series. The position of the matcher mentioned in the above and following paragraphs represents the impedance of the variable capacitors C1 and C2. It should be noted that the present disclosure does not limit to the case that only the capacitors in the matching circuit 13 are variable; similarly, impedance matching can also be achieved by variable inductors. As described above, upon receiving the DC bias voltage (BIAS), and determining to adjust the matcher in the matching circuit 13 according to the DC bias voltage (BIAS) and the default voltage, the control circuit 15 may adjust the variable capacitor C1 or C2 of the matching circuit 13 through a stepping motor (not shown) included therein to achieve impedance matching.

FIG. 3 is a first partial flowchart of method 2 according to an embodiment of the present disclosure. The present disclosure is not limited to being performed solely according to the flow steps shown in FIG. 3, provided that substantially the same results can be obtained.

At step 201: a radio frequency power supply is started to generate a radio frequency power.

At step 202: the radio frequency power is increased, and the radio frequency power generates an output power at the lower electrode through a matcher of the matching circuit that is at a default position.

At step 203: a control circuit judges whether the radio frequency power or a DC bias voltage meets a first condition, and if so, the flow proceeds to the flowchart of FIG. 5; otherwise, the flow returns to step 202.

In detail, when the DC bias voltage (BIAS) output from the sensor 14 reaches the default voltage, the control circuit 15 determines that the first condition is met, or when the radio frequency power RFp of the radio frequency power supply 12 reaches the maximum radio frequency power  $RFp_{max}$ , the control circuit 15 determines that the first condition is met.

Referring to FIG. 4A, a waveform diagram according to the first partial flowchart of the method 2 shown in FIG. 3 is depicted. At time point t0, the radio frequency

power supply 12 is started (step 201). Next, the control circuit 15 increases the radio frequency power RFp, which generates the output power OUTp at the lower electrode 11 through a matcher of the matching circuit 13 that is at the default position (step 202). The default position corresponds to the impedance of the matching circuit 13 before the matcher of the matching circuit 13 is adjusted. The output power OUTp is increased due to the increase in the radio frequency power RFp, and thus the radio frequency voltage above the workpiece (e.g., the wafer) is also increased, resulting in an increase in the DC bias voltage (BIAS) output from the sensor 14. It should be noted that the position of the matcher in the matching circuit 13 remains at the default position during the increase of the radio frequency power RFp. At time point t1, the DC bias voltage (BIAS) rises to the default voltage due to the increase of the radio frequency power RFp, and at this time, the control circuit 15 determines that the first condition is met.

Referring to FIG. 4B, another waveform diagram according to the first partial flowchart of the method 2 shown in FIG. 3 is depicted. At time point t0, the radio frequency power supply 12 is started (step 201). Next, the radio frequency power RFp is increased, and generates the output power OUTp at the lower electrode 11 through a matcher of the matching circuit 13 that is at the default position (step 202). Likewise, the output power OUTp is increased due to the increase in the radio frequency power RFp, and thus the radio frequency voltage above the workpiece (e.g., the wafer) is also increased, resulting in an increase in the DC bias voltage (BIAS) output from the sensor 14. Also likewise, the position of the matcher in the matching circuit 13 remains at the default position during the increase of the radio frequency power RFp. At time point t1, although the DC bias voltage (BIAS) has not reached the default voltage, the radio frequency power RFp has reached the maximum radio frequency power  $RFp_{max}$ , so the control circuit 15 determines that the first condition is met.

Referring to FIG. 5, a following second partial flowchart of the method 2 shown in FIG. 3 is depicted. The present disclosure is not limited to being performed solely according to the flow steps shown in FIG. 5, provided that substantially the same results can be obtained.

At step 204: the control circuit adjusts the radio frequency power with a first trend.

At step 205: the control circuit adjusts the position of the matcher in the matching circuit with a second trend.

5       At step 206: the control circuit judges whether the position of the matcher in the matching circuit or the DC bias voltage meets a second condition, and if so, the flow proceeds to step 207; otherwise, the flow returns to steps 204 and 205.

At step 207: the process is ended.

In detail, the control circuit 15 adjusts the radio frequency power RFp with a  
10       decreasing first trend, and adjusts, with a second trend involving increasing the ratio  
of the output power OUTp to the radio frequency power RFp, the position of the  
matcher in the matching circuit 13. In other words, the control circuit 15 controls the  
position of the matcher in the matching circuit 13 such that the impedance of the  
matching circuit 13 is impedance-matched with the output impedance (e.g., 50  $\Omega$ ) of  
15       the radio frequency power supply 12, the impedance of the transmission line between  
the radio frequency power supply 12 and the matching circuit 13, the impedance of  
the lower electrode 11, and the impedance formed by the plasma in the chamber 10. In  
addition, when the DC bias voltage (BIAS) reaches the default voltage and the ratio of  
the output power OUTp to the radio frequency power RFp is at the maximum (i.e.,  
20       impedance matching), the control circuit 15 determines that the second condition is  
met.

Referring to FIG. 6A, a waveform diagram according to the second partial  
flowchart of the method 2 shown in FIG. 5 is depicted. Continuing with the  
embodiment of FIG. 4A, at time point t1, when the DC bias voltage (BIAS) reaches  
25       the default voltage and the control circuit 15 determines that the first condition is met,  
the control circuit 15 adjusts the position of the matcher in the matching circuit 13  
with the second trend involving increasing the ratio of the output power OUTp to the  
radio frequency power RFp (step 205). With the adjustments by the control circuit 15,  
the position of the matcher in the matching circuit 13 gets closer and closer to the  
30       matching position corresponding to impedance matching. That is, the output power

OUTp, and thus the DC bias voltage (BIAS), will increase. Since the DC bias voltage (BIAS) has already reached the default voltage at time point t1, and will deviate from the default voltage if the DC bias voltage (BIAS) continues to increase, the control circuit 15 will adjust the radio frequency power RFp with the decreasing first trend (step 204), so as to ensure that the DC bias voltage (BIAS) will not deviate too much from the default voltage, and thus get stabilized around the default voltage more quickly.

In FIG. 6A, the trend is indicated by a dotted arrow. For example, the control circuit 15 adjusts the radio frequency power RFp with the decreasing first trend, so the radio frequency power RFp shown in FIG. 6A shows a downward trend after the time point t1. For another example, the control circuit 15 adjusts, with the second trend involving increasing the ratio of the output power OUTp to the radio frequency power RFp, the position of the matcher in the matching circuit 13, so the position of the matcher shown in FIG. 6A shows a trend toward the matching position after time point t1. For another example, the DC bias voltage (BIAS) shown in FIG. 6A tends to remain at the default voltage after time point t1. It should be noted that the dotted arrows in FIG. 6A only indicate a trend, in other words, the radio frequency power RFp is not limited to decrease with linear changes as shown in FIG. 6A, but may decrease with curved changes or gradually decrease after remaining constant for a period of time. Likewise, the DC bias voltage (BIAS) is not limited to be fixed at the default voltage, but may oscillate within a certain range of the default voltage.

In addition, it should be noted that the matching position in FIG. 6A represents a position when the matcher in the matching circuit 13 is adjusted to the so-called "matching position", where the ratio of the output power OUTp to the radio frequency power RFp is at the maximum, that is, impedance matching is achieved. The impedance represented by the matcher at the default position and the impedance represented by the matcher at the matching position are not limited to linear changes from each other. Meanwhile, although FIG. 6A depicts an upward trend for the position of the matcher, it does not mean that the impedance represented by the matching position of the matcher is greater than the impedance represented by the

default position of the matcher. The position of the matcher depicted in FIG. 6A should only be interpreted as the position of the matcher adjusted from the default position with the second trend involving increasing the ratio of the output power OUTp to the radio frequency power RFp. When the position of the matcher reaches the "matching position", the ratio of the output power OUTp to the radio frequency power RFp is at the maximum.

At time point t2, the ratio of the output power OUTp to the radio frequency power RFp is at the maximum and the DC bias voltage (BIAS) is the default voltage. At this time, the control circuit 15 determines that the second condition is met, and stops the adjustments to the radio frequency power RFp and the position of the matcher in the matching circuit 13. Thereby, the process of method 2 is ended.

By firstly increasing the radio frequency power RFp until the DC bias voltage (BIAS) reaches the default voltage, and then starting to adjust the position of the matcher in the matching circuit 13, the DC bias voltage (BIAS) can reach the default voltage in an effectively shortened time, and since the matcher of the matching circuit 13 reaches the matching position, the reflected power is at the minimum, thereby effectively reducing energy loss.

Referring to FIG. 6B, another waveform diagram according to the second partial flowchart of the method 2 shown in FIG. 5 is depicted. Continuing with the embodiment of FIG. 4B, at time point t1, although the DC bias voltage (BIAS) has not reached the default voltage, the radio frequency power RFp has reached the maximum radio frequency power  $RFp_{max}$ , so the control circuit 15 determines that the first condition is met. Next, the control circuit 15 adjusts the position of the matcher in the matching circuit 13 with the second trend involving increasing the ratio of the output power OUTp to the radio frequency power RFp (step 205). With the adjustments by the control circuit 15, the position of the matcher in the matching circuit 13 gets closer and closer to the matching position corresponding to impedance matching. That is, the output power OUTp, and thus the DC bias voltage (BIAS), will increase. Meanwhile, the control circuit 15 adjusts the radio frequency power RFp with the decreasing first trend (step 204). Even though the decrease of the radio frequency power RFp will

cause a decrease trend of the DC bias voltage (BIAS), the DC bias voltage (BIAS) can still increase continuously until the default voltage is reached under the condition that the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is larger than the  
5 decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power RFp.

However, the present disclosure is not limited thereto. As described above, since the radio frequency power RFp has already reached the maximum radio frequency power  $RFp_{max}$  although the DC bias voltage (BIAS) has not yet reached the default  
10 voltage at time point t1, if the radio frequency power RFp is then immediately decreased, the DC bias voltage (BIAS) will tend to decrease before reaching the default voltage, and thus further deviate from the default voltage. Accordingly, in another embodiment, the control circuit 15 may control the radio frequency power RFp to remain constant for a period of time after time point t1. At this time, since the  
15 position of the matcher in the matching circuit 13 gets closer and closer to the matching position corresponding to impedance matching, the DC bias voltage (BIAS) is thus increased. After the DC bias voltage (BIAS) reaches the default voltage, the control circuit 15 adjusts the radio frequency power RFp with the decreasing first trend (step 204), so as to ensure that the DC bias voltage (BIAS) will not deviate too  
20 much from the default voltage, and thus reach the default voltage more quickly.

Likewise, in FIG. 6B, the trend is indicated by a dotted arrow. For example, at time point t1, the control circuit 15 may adjust the radio frequency power RFp with the decreasing first trend, or may adjust the radio frequency power RFp with the decreasing first trend after the radio frequency power RFp remains constant for a  
25 certain period of time. Therefore, the radio frequency power RFp shown in FIG. 6B shows a downward trend after time point t1. For another example, the control circuit 15 adjusts, with the second trend involving increasing the ratio of the output power OUTp to the radio frequency power RFp, the position of the matcher in the matching circuit 13, so the position of the matcher shown in FIG. 6B shows a trend toward the  
30 matching position after time point t1. For another example, the DC bias voltage

(BIAS) shown in FIG. 6B tends to be adjusted toward the default voltage after time point t1. The dotted arrows in FIG. 6B only indicate a trend, in other words, the radio frequency power RFp is not limited to decrease with linear changes as shown in FIG. 6B, but as described above, the radio frequency power RFp may gradually decrease after remaining constant for a period of time. Likewise, without limitation, the DC bias voltage (BIAS) is adjusted to the default voltage with linear changes, or the DC bias voltage (BIAS) may be adjusted toward the default voltage with curved changes.

Likewise, the position of the matcher depicted in FIG. 6B should only be interpreted as the position of the matcher adjusted from the default position with the second trend involving increasing the ratio of the output power OUTp to the radio frequency power RFp. When the position of the matcher reaches the "matching position", the ratio of the output power OUTp to the radio frequency power RFp is at the maximum.

At time point t2, the ratio of the output power OUTp to the radio frequency power RFp is at the maximum and the DC bias voltage (BIAS) is the default voltage. At this time, the control circuit 15 determines that the second condition is met, and stops the adjustments to the radio frequency power RFp and the position of the matcher in the matching circuit 13. Thereby, the process of method 2 is ended.

By firstly increasing the radio frequency power RFp until the radio frequency power RFp reaches the maximum radio frequency power  $RFp_{max}$ , and then starting to adjust the position of the matcher in the matching circuit 13, the DC bias voltage (BIAS) can reach the default voltage in an effectively shortened time, and since the matcher of the matching circuit 13 reaches the matching position, the reflected power is at the minimum, thereby effectively reducing energy loss.

Referring to FIG. 7A, a waveform diagram illustrating adjusting the radio frequency power RFp with the first trend and adjusting the position of the matcher in the matching circuit 13 with the second trend according to an embodiment of the disclosure is depicted. Continuing with the embodiment of FIG. 4A, at time point t1, when the DC bias voltage (BIAS) reaches the default voltage and the control circuit 15 determines that the first condition is met, the control circuit 15 adjusts, with the

second trend involving increasing the ratio of the output power OUTp to the radio frequency power RFp, the position of the matcher in the matching circuit 13. Meanwhile, the control circuit 15 adjusts the radio frequency power RFp with the decreasing first trend. The decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power RFp changes in a non-linear manner, and similarly, the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" changes in a non-linear manner. In addition, the impedance of the plasma also changes in a non-linear manner. Therefore, considering the above factors comprehensively, the DC bias voltage (BIAS) cannot be increased or decreased stably. Accordingly, in FIG. 7A, during the time period from time points t1 to t3, where the position of the matcher in the matching circuit 13 and the radio frequency power RFp are adjusted at the same time, the DC bias voltage (BIAS) oscillates within a certain range around the default voltage.

In this embodiment, during the time period from time points t1 to t3, the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is greater than the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power RFp. Therefore, at time point t3, the DC bias voltage (BIAS) will be greater than the default voltage, and if the position of the matcher in the matching circuit 13 is continuously controlled to be adjusted toward the "matching position", the DC bias voltage (BIAS) will deviate from the default voltage. Accordingly, the control circuit 15 stops adjustments to the position of the matcher in the matching circuit 13 while continuously decreasing the radio frequency power RFp. In this manner, the DC bias voltage (BIAS) exhibits a decreasing trend during the time period from time points t3 to t4.

As will be understood by those ordinary skilled in the art, if, during the time period from time points t1 to t3, the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is less than the decrease of the DC bias voltage (BIAS) caused by the

decrease of the radio frequency power RFp, the DC bias voltage (BIAS) will be lower than the default voltage at time point t3. If the radio frequency power RFp is continuously controlled to be decreased, the DC bias voltage (BIAS) will be further deviated from the default voltage. Accordingly, the control circuit 15 may stop decreasing the radio frequency power RFp and continuously control the position of the matcher in the matching circuit 13 to be adjusted toward the "matching position". In this manner, the DC bias voltage (BIAS) exhibits an increasing trend during the time period from time points t3 to t4.

With continued reference to FIG. 7A, at time point t4, the DC bias voltage (BIAS) returns to the default voltage. During the time period from time points t4 to t5, the control circuit 15 again controls the position of the matcher in the matching circuit 13 to be adjusted toward the "matching position", and decreases the radio frequency power RFp. Since at this time, the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is less than the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power RFp, the DC bias voltage (BIAS) will be lower than the default voltage at time point t5. At this time, if the radio frequency power RFp is continuously controlled to be decreased, the DC bias voltage (BIAS) will be further deviated from the default voltage. Accordingly, the control circuit 15 stops decreasing the radio frequency power RFp, and continuously adjusts the position of the matcher in the matching circuit 13. In this manner, the DC bias voltage (BIAS) exhibits an increasing trend during the time period from time points t5 to t2.

As will be understood by those ordinary skilled in the art, if, during the time period from time points t4 to t5, the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is greater than the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power RFp, the DC bias voltage (BIAS) will be greater than the default voltage at time point t5. If the position of the matcher in the matching circuit 13 is continuously controlled to be adjusted toward the "matching position", the DC bias voltage (BIAS) will be further deviated from the default

voltage. Accordingly, the control circuit 15 may stop controlling the position of the matcher in the matching circuit 13 to be adjusted toward the "matching position", and continuously decrease the radio frequency power RFp. In this manner, the DC bias voltage (BIAS) exhibits a decreasing trend during the time period from time points t5 to t2.

At time point t2, the ratio of the output power OUTp to the radio frequency power RFp is at the maximum and the DC bias voltage (BIAS) is the default voltage. At this time, the control circuit 15 determines that the second condition is met, and stops the adjustments to the radio frequency power RFp and the position of the matcher in the matching circuit 13.

It should be noted that the variation of the DC bias voltage (BIAS) in FIG. 7A is only illustrated as an example, but not a limitation to the disclosure. The spirit of the disclosure lies in that the DC bias voltage (BIAS) can reach the default voltage quickly, and after reading the above embodiments, a person skilled in the art should easily understand that the DC bias voltage (BIAS) can be increased by controlling the position of the matcher in the matching circuit 13 to be adjusted toward the "matching position", and conversely, the DC bias voltage (BIAS) can be decreased by decreasing the radio frequency power RFp. Moreover, the control circuit 15 can adjust the position of the matcher in the matching circuit 13 and the radio frequency power RFp according to the actual condition of the DC bias voltage (BIAS), so as to achieve the spirit of the present disclosure.

Referring to FIG. 7B, another waveform diagram illustrating adjusting the radio frequency power RFp with the first trend and adjusting the position of the matcher in the matching circuit 13 with the second trend according to an embodiment of the disclosure is depicted. Continuing with the embodiment of FIG. 4B, at time point t1, although the DC bias voltage (BIAS) has not reached the default voltage, the radio frequency power RFp has reached the maximum radio frequency power RFp<sub>max</sub>, so the control circuit 15 determines that the first condition is met. Next, as described in the embodiment of FIG. 6B, the control circuit 15 adjusts the radio frequency power RFp with the decreasing first trend, while controlling the position of the matcher in

the matching circuit 13 to be closer to the matching position in impedance matching.

During the time period from time points  $t_1$  to  $t_3$ , since the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is less than the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power  $RF_p$ , the DC bias voltage (BIAS) exhibits a decreasing trend. Starting from time point  $t_3$ , the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" begins to exceed the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power  $RF_p$ , the DC bias voltage (BIAS) exhibits an increasing trend. As will be understood by those ordinary skilled in the art, if, during the time period from time points  $t_1$  to  $t_3$ , the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" is greater than the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power  $RF_p$ , the DC bias voltage (BIAS) will not exhibit a decreasing trend during the time period from time points  $t_1$  to  $t_3$ , but instead, the DC bias voltage (BIAS) will continuously increase.

At the time point  $t_2$ , the ratio of the output power  $OUT_p$  to the radio frequency power  $RF_p$  is at the maximum and the DC bias voltage (BIAS) is the default voltage, the control circuit 15 determines that the second condition is met and stops the adjustments to the radio frequency power  $RF_p$  and the position of the matcher in the matching circuit 13.

Referring to FIG. 7C, yet another waveform diagram illustrating adjusting the radio frequency power  $RF_p$  with the first trend and adjusting the position of the matcher in the matching circuit 13 with the second trend according to an embodiment of the disclosure is depicted. Continuing with the embodiment of FIG. 4B, at time point  $t_1$ , although the DC bias voltage (BIAS) has not reached the default voltage, the radio frequency power  $RF_p$  has reached the maximum radio frequency power  $RF_{p_{max}}$ , so the control circuit 15 determines that the first condition is met. Next, as described in the embodiment of FIG. 6B, the control circuit 15 firstly controls the radio

frequency power RFp to remain constant, while controlling the position of the matcher in the matching circuit 13 to be adjusted toward the "matching position". The DC bias voltage (BIAS) is thus increased. At the time point t3, the DC bias voltage (BIAS) reaches the default voltage and the control circuit 15 begins to adjust the radio frequency power RFp with the decreasing first trend and continuously control the position of the matcher in the matching circuit 13 to be closer to the matching position in impedance matching.

As described in the embodiment of FIG. 7A, since the decrease of the DC bias voltage (BIAS) caused by the decrease of the radio frequency power RFp changes in a non-linear manner, and similarly, the increase of the DC bias voltage (BIAS) caused by the position of the matcher in the matching circuit 13 adjusted toward the "matching position" changes in a non-linear manner, it is not guaranteed that the DC bias voltage (BIAS) will be steadily increased or decreased. Accordingly, in FIG. 7C, during the time period from time points t3 to t2, the DC bias voltage (BIAS) oscillates within a certain range around the default voltage. After reading the above embodiments, a person skilled in the art should understand that for brevity purposes, detailed description about the decrease of the DC bias voltage (BIAS) with respect to the radio frequency power RFp and changes in the position of the matcher in the matching circuit 13 adjusted toward the "matching position" during the time period from time points t3 to t2 in the embodiment of FIG. 7C are omitted.

At time point t2, the ratio of the output power OUTp to the radio frequency power RFp is at the maximum and the DC bias voltage (BIAS) is the default voltage. At this time, the control circuit 15 determines that the second condition is met, and stops the adjustments to the radio frequency power RFp and the position of the matcher in the matching circuit 13.

In the above embodiment, by firstly increasing the radio frequency power RFp until the first condition is met, i.e., until the DC bias voltage (BIAS) reaches the default voltage or, until the radio frequency power RFp reaches the maximum radio frequency power  $RFp_{max}$ , and then starting to adjust the position of the matcher in the matching circuit 13, the DC bias voltage (BIAS) can reach the default voltage in an

effectively shortened time, and since the matcher of the matching circuit 13 reaches the matching position, the reflected power is at the minimum, thereby effectively reducing energy loss. However, the present disclosure is not limited thereto. The purpose of making the matcher of the matching circuit 13 reach the matching position is to obtain the minimum reflected power and thus reduce energy loss. However, in the case of not considering energy loss, the control circuit 15 may choose not to adjust the position of the matcher in the matching circuit 13 to the "matching position".

FIG. 8 is a flowchart of a method applied to a plasma system according to another embodiment of the disclosure. The present disclosure is not limited to being performed solely according to the flow steps shown in FIG. 8, provided that substantially the same results can be obtained.

At step 701: a radio frequency power supply is started to generate a radio frequency power.

At step 702: the radio frequency power is increased, and the radio frequency power generates an output power at the lower electrode through a matcher of the matching circuit that is at a default position.

At step 703: a control circuit judges whether the radio frequency power or the DC bias voltage meets a first condition, and if so, the flow proceeds to step 704; otherwise, the flow proceeds to step 702.

As described in the embodiment of FIG. 3, when the DC bias voltage (BIAS) output from the sensor 14 reaches the default voltage, the control circuit 15 determines that the first condition is met, or when the radio frequency power RFp of the radio frequency power supply 12 reaches the maximum radio frequency power  $RFp_{max}$ , the control circuit 15 determines that the first condition is met.

At step 704: the position of the matcher in the matching circuit 13 is selectively adjusted.

In detail, if the DC bias voltage (BIAS) output from the sensor 14 reaches the default voltage, the control circuit will not adjust the position of the matcher in the matching circuit 13; if the radio frequency power RFp of the radio frequency power supply 12 reaches the maximum radio frequency power  $RFp_{max}$ , but the DC bias

voltage (BIAS) has not reached the default voltage, the control circuit will adjust the position of the matcher in the matching circuit 13 toward the "matching position".

Referring to FIG. 9A, at time point t0, the radio frequency power supply 12 is started (step 701). Next, the radio frequency power RFp is increased, and generates the output power OUTp at the lower electrode 11 through a matcher of the matching circuit 13 that is at the default position (step 702). The output power OUTp is increased due to the increase in the radio frequency power RFp, and thus the radio frequency voltage above the workpiece (e.g., the wafer) is also increased accordingly, resulting in an increase in the DC bias voltage (BIAS) output from the sensor 14. The control circuit 15 keeps the position of the matcher in the matching circuit 13 at the default position throughout the increase of the radio frequency power RFp. At time point t1, the DC bias voltage (BIAS) rises to the default voltage due to the increase of the radio frequency power RFp, and at this time, the control circuit 15 determines that the first condition is met (step 703). Since the DC bias voltage (BIAS) has reached the default voltage, the control circuit 15 stops adjusting the radio frequency power RFp. Since the control circuit 15 does not adjust the position of the matcher in the matching circuit 13 (step 704), the position of the matcher in the matching circuit 13 is not at the "matching position". However, the DC bias voltage (BIAS) can still quickly reach the default voltage without considering the magnitude of the reflected power of the matching circuit 13 to the radio frequency power RFp.

Referring to FIG. 9B, at time point t0, the radio frequency power supply 12 is started (step 701). Next, the control circuit 15 increases the radio frequency power RFp, which generates the output power OUTp at the lower electrode 11 through a matcher of the matching circuit that is at the default position (step 702). The output power OUTp is increased due to the increase in the radio frequency power RFp, and thus the radio frequency voltage above the workpiece (e.g., the wafer) is also increased, resulting in an increase in the DC bias voltage (BIAS) output from the sensor 14. Likewise, the position of the matcher in the matching circuit 13 remains at the default position during the increase of the radio frequency power RFp. At time point t1, although the DC bias voltage (BIAS) has not reached the default voltage, the

radio frequency power RFp has reached the maximum radio frequency power  $RFp_{max}$ , and at this time, the control circuit 15 determines that the first condition is met (step 703). Next, the control circuit 15 controls the radio frequency power RFp to remain constant, and begins to control the position of the matcher in the matching circuit 13 to be adjusted toward the "matching position" (step 704), so that the DC bias voltage (BIAS) is continuously increased. At time point t3, although the position of the matcher in the matching circuit 13 has not reached the "matching position". the DC bias voltage (BIAS) has reached the default voltage, and thus the control circuit 15 stops adjustments to the position of the matcher in the matching circuit 13. In this manner, the DC bias voltage (BIAS) can still quickly reach the default voltage without considering the magnitude of the radio frequency power RFp (remaining at the maximum radio frequency power  $RFp_{max}$ ) and the magnitude of the reflected power of the matching circuit 13 to the radio frequency power RFp.

In summary, by firstly increasing the radio frequency power RFp until the first condition is met, i.e., until the DC bias voltage (BIAS) reaches the default voltage or the radio frequency power RFp reaches the maximum radio frequency power  $RFp_{max}$ , and then starting to adjust the position of the matcher in the matching circuit 13, the present disclosure can make the DC bias voltage (BIAS) reach the default voltage in an effectively shortened time, and since the matcher of the matching circuit 13 reaches the matching position, make the reflected power at the minimum, thereby effectively reducing energy loss. However, in the case of not considering energy loss, the control circuit 15 may choose not to adjust the matcher of the matching circuit 13 to the "matching position", but can still make the DC bias voltage (BIAS) reach the default voltage in an effectively shortened time.

25

What is claimed is:

1. A method applied to a plasma system, the plasma system having a chamber, a lower electrode disposed in the chamber, and a radio frequency source coupled to the lower electrode via a matching circuit, and the plasma system being configured to process a workpiece placed on the lower electrode, wherein the method comprises:

starting the radio frequency source;

increasing a radio frequency power of the radio frequency source, and generating an output power at the lower electrode through a matcher of the matching circuit that is at a default position; and

adjusting, when a first condition is met, the radio frequency power with a first trend, and adjusting, with a second trend involving increasing a ratio of the output power to the radio frequency power, the matching circuit to meet a second condition.

2. The method according to claim 1, wherein the first condition comprises a direct current (DC) voltage detected by a sensor coupled to the workpiece reaching a default voltage.

3. The method according to claim 1, wherein the first condition comprises the radio frequency power reaching a maximum radio frequency power.

4. The method of any one of claims 2-3, wherein the second condition is met when the ratio of the output power to the radio frequency power is at the maximum and the DC voltage detected by the sensor coupled to the workpiece reaches the default voltage.

5. The method according to claim 1, wherein the first trend comprises adjusting the radio frequency power in a decreasing manner.

6. A method applied to a plasma system, the plasma system having a chamber, a

lower electrode disposed in the chamber, and a radio frequency source coupled to the lower electrode via a matching circuit, and the plasma system being configured to process a workpiece placed on the lower electrode, wherein the method comprises:

starting a radio frequency source;

5        increasing a radio frequency power of the radio frequency source, the radio frequency power generating an output power at the lower electrode through a matcher of the matching circuit that is at a default position; and

adjusting, when a DC voltage detected by a sensor coupled to the workpiece reaches a default voltage or the radio frequency power reaches a maximum radio  
10       frequency power, the matcher of the matching circuit to increase a ratio of the output power to the radio frequency power.

7. The method according to claim 6, further comprising:

decreasing the radio frequency power of the radio frequency source when the DC  
15       voltage reaches the default voltage or the radio frequency power reaches the maximum radio frequency power.

8. The method according to claim 6, further comprising:

maintaining the radio frequency power until the DC voltage is greater than the  
20       default voltage, and then decreasing the radio frequency power of the radio frequency source.

9. The method according to any one of claims 7-8, further comprising:

stopping adjustment of the matcher of the matching circuit when the ratio of the  
25       output power to the radio frequency power is at the maximum and the DC voltage reaches the default voltage.

10. A plasma system having a chamber and configured to process a workpiece placed in the chamber, comprising:

30        a lower electrode disposed in the chamber;

a radio frequency source coupled to the lower electrode;

a matching circuit coupled between the radio frequency source and the lower electrode, wherein when the radio frequency source is started to generate a radio frequency power, an output power is generated at the lower electrode through a matcher  
5 of the matching circuit that is at a default position; and

a control circuit coupled to the radio frequency source and the matching circuit, wherein the control circuit is configured to control the radio frequency source to increase the radio frequency power until a first condition is met, and then adjust the radio frequency power with a first trend, and adjust, with a second trend involving  
10 increasing a ratio of the output power to the radio frequency power, the matching circuit to meet a second condition.