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(54) CIRCUIT ARRANGEMENT FOR GENERATING A CONTROL SIGNAL FOR THE FIELD OUTPUT STAGE IN A TELEVISION RECEIVER

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a circuit arrangement for generating a control signal for the field timebase stage in a television receiver for a system in which a number of fields constitutes an image, the arrangement comprising a generator for generating a signal whose frequency is the line frequency or an integral multiple of the line frequency, a frequency divider circuit for dividing the signal output of the generator, means for applying received field synchronising pulses to a comparator stage for comparing the phase between the synchronising pulses and pulses produced by the frequency divider circuit, the comparator stage being capable of supplying a signal to a gate which signal is dependent on the phase difference between the compared pulses.

A circuit arrangement of this kind is described in United States Patent Specification 3,708,621. Since in this known circuit arrangement, the control signal is derived by frequency division from the line synchronising signal, its frequency is correct as soon as the line synchronising circuit has pulled in in frequency which is usually effected at a comparatively fast rate. The comparator stage which may be formed as a coincidence stage and an integrator ensure the correct phase of the received field control signal relative to the field synchronising pulses originating from the transmitter and received by the television receiver. In the off-phase condition the comparator stage provides a pulse during the occurrence of a pulse originating from the frequency divider circuit. When the integrator, which may be a counter, has received a given number of these pulses, it in turn applies a signal

which enables the gate. The frequency divider circuit, which consists of a plurality of bistable elements, is then reset in that one of the received field synchronising pulses is passed by the gate. The phase is then correct, the comparator stage no longer supplies a pulse and the received synchronising pulses can in principle no longer reach the divider circuit, at least not as long as the signal generated by the circuit arrangement maintains the same frequency and the same phase as the received pulses.

The known circuit arrangement is considered to have the following drawbacks. Firstly, at the instant when the frequency divider circuit is reset, vertical deflection discontinues and subsequently commences again which means that one vertically directed deflection period becomes shorter than the others. When this deflection period is very short or when, in contrast, it is almost as long as a normal deflection, i.e. 20 ms in a television system using 50 fields per second, this is not a very great drawback. When, however, the shorter deflection period lasts, for example, 10 ms, the mean level of the sawtooth current flowing through the field deflection coil is shifted considerably which may result in the transistors of the field output stage providing the said current being cut off for a given period. A brightly lit horizontal line then appears on the display screen of the receiver which is disturbing for the observer and which may be harmful for the screen.

Secondly, in the case when the received signal is weak, the coincidence stage not only receives the useful field synchronising pulses originating from the transmitter but also noise and interference. It may then occur that the coincidence stage receives too little information during the occurrence of the synchronising pulses which may be observed as the off-phase condition. The gate may therefore be enabled at any arbitrary instant so that interference can directly influence the frequency divider circuit and cause an incorrect phase. The divider circuit may also at any instant be reset so

that the vertical deflection can commence and end at any instant. The height of the image displayed then continuously varies and may be very small if interference continues at a fast rate. This has the same disturbing effect as that described above.

It is an object of the invention to provide an improved arrangement of the type described above.

10 From one aspect the invention provides a circuit arrangement for generating a control signal for the field time base stage in a television receiver for a system in which a plurality of fields constitutes an image, said
15 arrangement comprising a generator for generating a signal whose frequency is the line frequency or an integral multiple of the line frequency, a frequency divider circuit for dividing the signal output of said generator,
20 means for applying received field synchronising pulses to a comparator stage for comparing the phase between said synchronising pulses and the pulses produced by said frequency divider circuit, said comparator
25 stage being capable of applying a signal to a gate which signal is dependent on the phase difference between said compared pulses, said frequency divider circuit, dependent on an output signal from said gate,
30 being switchable under the control of a memory element between first and second states, respectively having first and second divisors.

35 From a further aspect the invention provides a circuit arrangement for generating a control signal for the field time base stage in a television receiver for a system in which a plurality of fields constitutes an image, said arrangement comprising a generator for
40 generating a signal whose frequency is the line frequency or an integral multiple of the line frequency, said multiple being equal to the number of fields in an image, a frequency divider circuit for dividing the signal
45 output of said generator, means for applying received field synchronising pulses to a comparator stage for comparing the phase between said synchronising pulses and pulses produced by said frequency divider circuit,
50 said comparator stage being capable of applying a signal to a gate which signal is dependent on the phase difference between said compared pulses, said frequency divider circuit dependent on an output signal from
55 said gate being switchable under the control of a memory element between first and second states, respectively having first and second divisors, said first divisor being numerically equal to the number of lines per image, whilst said second divisor differs from
60 said first divisor, said memory element bringing and maintaining said frequency divider circuit in its first state when said compared pulses at least partly coincide but brings
65 said frequency divider to its second state

when said compared pulses have not coincided for a given period.

The drawbacks of the known circuit arrangement have been recognised by being caused by the received field synchronising pulses being directly applied to the frequency divider circuit. With the present invention, no received signal and hence no interference can directly reach the divider circuit. This may be compared with the known circuit arrangements in which a field oscillator to be synchronised is used instead of a divider circuit (or a counter). In these circuit arrangements, the oscillator initially receives the received field synchronising pulses (direct synchronisation) until the frequency and the phase of the generated signal are correct. Subsequently, the direct path is completely or partly cut off while the frequency and the phase are always recontrolled (indirect synchronisation) unless the off-phase condition occurs again for some reason or other. In the known circuit arrangement referred to in the abovementioned United States Patent Specification, direct synchronisation is used only once for resetting for the case where the off-phase condition (=non-coincidence) has taken longer than a given period whereafter the frequency divider circuit operating as a field generator does not receive anything anymore unless, as has been explained, the received signal is weak. In the circuit arrangement according to the invention which is also provided with a frequency divider circuit, this divider circuit is not adjusted by an external signal. This again is an indirect synchronisation, but one which is only active in the off-phase condition and is thereafter no longer active. The circuit arrangement according to the invention therefore has the advantage of the circuit arrangements employing indirect synchronisation, i.e. the greater insensitivity to interference, as well as the advantage of generating the field frequency by means of frequency division, i.e. obtaining substantially immediately the exact frequency of the control signal applied to the field output stage.

Moreover, since the frequency divider circuit in the circuit arrangement according to the invention has two states with different divisors which are dependent on the output voltage of the gate, that is to say, on the fact whether the received and generated signals of field frequency are either in phase or not in phase (=coincidence), the above-described interfering phenomena cannot occur. In fact, the second divisor will in practice be chosen sufficiently closely to the first one in order that switching over from one to the other divider cannot result in an image having a small height and a strong brightness.

A further aspect of the invention is that

the relevant circuit arrangement is alternatively suitable for the reception of "non-standard signals", i.e. signals in which the number of lines per image deviates from the number prescribed for the relevant television system. Such signals are generated by some test signal generators or may be produced when using video recorders. An embodiment of the circuit arrangement according to the invention makes synchronisation in such a case possible as well, whereby direct synchronisation is used. To this end the memory element may comprise a bistable element receiving reset pulses when the compared pulses at least partly coincide and receiving set pulses when the compared pulses have not coincided for a given period, while the divisor in its second state may be larger than that in its first state, means being provided by which the bistable element in the memory element cannot receive reset pulses, with the frequency divider circuit being adjustable by means of received field synchronising pulses.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a block schematic diagram of a television receiver provided with a first embodiment circuit arrangement according to the invention,

Figure 2 shows in greater detail part of the circuit arrangement of Figure 1,

Figures 3, 4, 5, 6 and 7 show waveforms for describing the operation of Figures 1 and 2,

Figure 8 shows in greater detail a further part of the circuit arrangement, and

Figure 9 shows part of a second embodiment of the circuit arrangement according to the invention.

In Figure 1, 1 denotes an aerial by means of which a television signal can be received. This signal is applied to an RF and detection section 2. The detected signal is subsequently applied to the sound section 3 of the television receiver and to a video amplifier 4 at whose output a complete video signal, possibly with a chrominance signal in the case of colour television, is available. This signal is applied to a section 5 in which it is processed for a picture display tube 6 as well as to a synchronising separator 7. The output voltage of separator 7 comprises line synchronising pulses which are applied to a phase detector 8 whose output voltage can influence an oscillator 11 through a fly-wheel filter 9 and a reactance circuit 10. Oscillator 11 generates a voltage of double the line frequency $2f_H$, i.e. 31250 Hz in the case of reception of a signal in accordance with a television system employing 625 lines per complete image, 2 interlaced rasters per image and 50 fields per second. It is also

possible that oscillator 11 generates a voltage of the line frequency f_H and whose frequency is subsequently doubled. The voltage of the frequency $2f_H$ controls a frequency divider circuit 12 in which its frequency is divided by two and the signal thus obtained is applied through a pulse shaper 13 to the line output stage 14 which provides the line deflection current for the deflection coil (not shown) for the horizontal deflection of the electron beam(s) in tube 6.

The voltage available at the output of oscillator 11 also controls frequency divider circuit 15 in which its frequency is divided by the divisor 625 in a first state and by another divisor in a second state. When oscillator 11 has the correct frequency, i.e. after frequency pull-in of the circuits 8, 9, 10, 11 for the in direct line synchronisation, the frequency of the signal generated by the divider circuit 15 is correct, that is to say, it is equal to the field frequency, in case of the given standard of 50 Hz, if the divider circuit is in its first state. An adjusting gate 16 ensures that the divider has the correct value. A pulse shaper 17 receives the signal generated by the divider circuit 15 and controls the field output stage 18 which applies the field deflection current to the deflection coil (not shown) for the vertical deflection of the electron beam(s) in tube 6. The two pulse shapers 13 and 17 ensure that the line and the field control signal acquire the waveform required for output stages 14 and 18, respectively.

The output voltage from synchronising separator 7 also comprises field synchronising pulses which are separately obtained by means of a field synchronising separator 19 which separated pulses are applied to an input of a coincidence stage 20. The divided pulses originating from the output of pulse shaper 17 are present at a second input of the coincidence stage 20. In the on-phase state, that is to say, in the case where a field synchronising pulse originating from the separator 19 and a divider pulse from shaper 17 at least partly coincide, stage 20 does not provide a signal. In the off-phase state, it provides a signal, namely a divider pulse to an integrator 21 which is followed by a level detector 22. When this off-phase state lasts at least approximately 0.4 s, which corresponds to approximately 20 pulses, the detected level exceeds a given threshold level so that a gate 23 formed as control switch starts to conduct. The field synchronising pulses at the output of separator 19 are also applied to a trigger 24 which, for example, by means of differentiation, generates pulses whose leading edges coincide with those of the synchronising pulses. When switch 23 conducts, some of these pulses are passed and are applied to a memory element 25. Memory element 25 influences adjusting gate 16

through a gate 26 in a manner which will be described hereinafter with the result that the on-phase state occurs. Coincidence stage 20 then does not provide a pulse so that switch 23 is cut off. Element 25 influences also pulse shaper 17 as will be described hereinafter.

Figure 2 shows in greater detail the parts 15, 16, 25 and 26 of the circuit arrangement shown in Figure 1. In this embodiment, frequency divider circuit 15 consists of ten bi-stable elements, in this case flipflops 15₁, 15₂ . . . 15₁₀ which may be formed in known manner and each of which divides by two. In order that divider circuit 15 is reset after the 625th period of the signal with the frequency 2f₁₁ to the initial position, i.e. the position at the commencement of the first period, the outputs of oscillator 11 and of flipflops 15₅, 15₆, 15₇ and 15₁₀ are connected to five inputs of the adjusting gate 16 formed as a NAND gate, while gate 26 is connected to a sixth input 27 thereof.

Figure 3 shows the operation of divider circuit 15 and adjusting gate 16 in which input 27 is initially left out of consideration. Figure 3 shows the output signal S11 from oscillator 11 as well as the output signals Q15₁, Q15₂, . . . Q15₁₀ from flipflops 15₁, 15₂, . . . 15₁₀ and the signal S28 at the reset line 28 of the flipflops, which line connects the reset terminals (S₂) of all flipflops of divider circuit 15 and which is connected to the output of gate 16. The numbers T₁, T₂, . . . T₆₂₅, T₆₂₆, T₆₂₇ indicate the periods of signals S11, while H₁, H₂, . . . H₃₁₁, H₃₁₂ indicate the corresponding line periods. For the raster commencing after period T₆₂₅ the notations T'₁, T'₂, . . . H'₁ apply. Each flipflop reverses when a leading edge occurs in the output signal from the previous flipflop or from signal S11.

At the commencement of period T₁, signals S11, Q15₁, Q15₂, . . . Q15₁₀ are "high" which may be indicated by the binary number 0. At the commencement of period T₂, flipflop 15₁ reverses, signal Q15₁ becomes "low" which corresponds to the number 1. Figure 3 shows that for the first six periods the flipflops indicate the following:

T₁: 0000000000
T₂: 0000000001
T₃: 0000000010
T₄: 0000000011
T₅: 0000000100
and T₆: 0000000101

in which signals Q15₁, Q15₂, . . . Q15₁₀ are written from the right to the left. These are the numbers 0, 1, 2, 3, 4 and 5 in the decimal system, that is to say, the number of the corresponding period reduced by 1. For the periods T₆₂₂, T₆₂₃, T₆₂₄ and T₆₂₅ the flipflops indicate the following:

T₆₂₂: 1001101101
T₆₂₃: 1001101110
T₆₂₄: 1001101111
and T₆₂₅: 1001110000

These are the numbers 621, 622, 623 and 624.

It is evident that gate 16 has received at least one 0 at one of its inputs up to the first half of period T₆₂₅. Figure 3 shows that during the second half of period T₆₂₅ signals S11, Q15₅, Q15₆, Q15₇ and Q15₁₀ are simultaneously equal to 1 so that signal S28 becomes equal to 0. The pulse thus generated is applied as a reset pulse through line 28 to all flipflops of divider circuit 15. The flipflops which were not in the "high" state, i.e. flipflops 15₅, 15₆, 15₇ and 15₁₀ are brought to that state while the other flipflops do not change their state. At the commencement of the next period, period T'₁, all flipflops indicate 0 and a new raster commences.

Memory element 25 includes a flipflop 29, an output 30 of which is connected to an input of gate 26 while another input of gate 26 is connected to the output of flipflop 15₄. The outputs of an OR gate 32 and of an OR gate 33 are connected to the set (S₁) and the reset terminal (S₂), respectively, of flipflop 29. The output signal Q from flipflop 29 is present at output 30 and

the other output signal $\bar{Q}$ is present at the other output 31 thereof. The output signals from switch 23 and pulse shaper 17 are applied to gate 33 while the output signals from switch 23 and an inverter stage 34 are applied to gate 32, stage 34 reversing the output signal from pulse shaper 17 in its polarity.

In the off-phase state, received pulses are passed by switch 23 (Figure 4a) which do not coincide with the divider pulses (Figure 4b) originating from pulse shaper 17. Consequently, gate 33 does not provide a signal (Figure 4d). However, gate 32 receives the pulses of Figure 4b and the pulses of Figure 4c which are inverted relative thereto so that this gate is enabled. The first of the output pulses from gate 32 (Figure 4e) sets flipflops 29 whose output signals conse-

quently become Q=1 and $\bar{Q}$ =0. If flipflop 29 were already in this state, nothing would be changed.

When the on-phase state has been achieved after some time, one pulse from switch 23 (Figure 5a) and one divider pulse (Figure 5b) at least partly coincide. Gate 33 is enabled (Figure 5d) while gate 32 which receives the pulse of Figure 5a and the pulse of Figure 5c which is inverted relative to that of Figure 5b does not provide a signal (Figure 5e). Flipflop 29 is reset by the pulse

of Figure 5d, that is to say, the signals $Q=0$ and $Q=1$ are present at terminals 30 and 31, respectively. Gate 26 is a controlled switch and does not conduct under these circumstances. The operation of divider circuit 15 therefore remains the same as has been described hereinbefore. If due to the inertia of integrator 21 other pulses might be passed by switch 23, the state will not change.

In the off-phase state for which $Q=1$ gate 26 conducts so that the output signal $Q15_1$ from flipflop 15, is present at the input 27. Figure 3 shows that $Q15_1=0$ during period T_{625} . Signal S28 consequently remains equal to 1 and divider circuit 15 is not reset. Figure 6 shows the further variation. This Figure shows that only during the second half of period T_{633} , i.e. 8 periods later than in the on-phase state, the signals S11, $Q15_1$, $Q15_2$, $Q15_3$, $Q15_4$, and $Q15_5$, applied to gate 16 are all equal to 1 so that a reset pulse $S28=0$ is generated. The next period is thus the first period T_1 of a new raster.

The foregoing shows that memory element 25 ensures that, dependent on the fact whether the on-phase or off-phase state has occurred, the frequency divider circuit divides the frequency $2f_{11}$ from signal S11 by the divisors 625 and 633 respectively. The following cases may occur:

1. on-phase state, with $Q=0$: the previous divisor was 625, Q remains 0, the on-phase state is maintained and neither the memory element nor the divider circuit are influenced;
2. on-phase state with $Q=1$: the previous divisor was 633, Q becomes 0 and the divisor becomes 625, which is the case as under 1;
3. off-phase state (longer than approximately 0.4 s) with $Q=0$: the previous divisor was 625, Q becomes 1 so that the divisor becomes 633; the pulses in Figures 5a and 5b have different repetition frequencies and are displaced relative to each other; after a given pull-in period, the on-phase state is reached which is the case as under 2;
4. off-phase state (longer than approximately 0.4 s) with $Q=1$: the previous divisor was 633 and remains so because Q remains equal to 1 which is the case as under 3.

The case under item 1 above is thus always the final state in which neither any received signal nor any noise or interferences can reach the divider circuit. If the received field synchronising pulses drop out after this state has been reached the divider circuit continues to divide by 625 due to the action of the memory element so that the image displayed on the display screen of tube 6 remains in place. When the re-

ceived signal is so weak that substantially no distinction can be made between interferences and field synchronising pulses or when these pulses drop out before the on-phase state is reached, the divisor 633 is used for division. The image "rolls over" in the vertical direction which is less disturbing to the observer and is less harmful for the screen than the brightly lit narrow images which can be displayed with the known circuit arrangement.

Figure 7 shows how the pull-in process is effected, i.e. when $Q=1$. Figure 7a shows the output pulses from pulse shaper 17 and Figure 7b shows the pulses originating from trigger 24. Since the frequency of the latter pulses ($=2f_{H.1}/625$) is higher than that of the former pulses ($=2f_{H.1}/633$), they are displayed moving relative thereto to the left until coincidence takes place in gates 32 and 33: Q becomes 0; coincidence also takes place in the coincidence stage 20 and switch 23 is open. For each period of the frequency divider circuit, the relative time difference Δt between two received pulses 1 and 2 is equal to 8 times one period of signal S11, i.e., approximately $8 \times 32 \mu s = 256 \mu s$. One period of the frequency divider

circuit corresponds to $\frac{633 \times 32}{8 \times 32} = 79$ times

Δt . In the most unfavourable case in which the process commences with the pulse in the position 3 in Figure 7b, this process will therefore take approximately 75 field periods, i.e. 1.5 s. In this extreme case, which is very improbable, it takes consequently approximately $0.4 + 1.5 = 1.9$ s before the displayed images comes to a standstill.

It may occur that just before the end of the pull-in process the pulse of Figure 7b occupies such a position, indicated by 4, that at the next position 5 after a period of time Δt the leading edge of the pulse occurs just before the trailing edge of the pulse of Figure 7a. As a result, the divider circuit is brought to the state with the divisor 625. Since the coincidence period is then very short, it is however, evident that this situation is very sensitive to interference. This drawback is obviated according to a feature of the invention in that the duration of the pulse in Figure 7a is made longer at the instant when the 625-state occurs. Information therefore may be obtained from memory element 25 which thus fulfils a second function, which information is applied to pulse shaper 17.

Figure 8 shows pulse shaper 17 in greater detail. The outputs of flipflops 15, and flipflop 15, are connected to the inputs of controlled switches 35 and 36, respectively. The switches 35 and 36 are controlled by the signals at the outputs 30 and 31, respectively, of memory elements 25. The

outputs of switches 35 and 36 are connected to two inputs of an adder stage 37. The output signal thereof is applied to a keyed gate 38 which is keyed by the output signal $Q_{15,10}$ from flipflop 15.

A pulse shaper is required in any case. The output signal $Q_{15,10}$ from the frequency divider circuit has a natural frequency of $2f_{11} \cdot \frac{1}{2}^{10}$ which corresponds to a natural period of approximately 33 ms. Circuit 15 is reset approximately 20 ms after the commence-

ment of the period, i.e. $20 - \frac{33}{2} \approx 35$ ms after

reversal in the middle of the natural period. Signal $Q_{15,10}$ therefore has a flyback period of approximately 3.5 ms and is thus not usable as a field control signal. The pulse shaper therefore has also two states. In the state with divisor 633 of the divider circuit

for which $Q=1$ and $\bar{Q}=0$, switch 35 conducts while switch 36 is cut off. The output signal $Q_{15,10}$ from flipflop 15, whose natural period is equal to $2^4 \cdot \frac{1}{2} f_{11} \approx 512 \mu s$ is applied to gate 38. This gate is keyed in such a manner that only the first positive half period of signal $Q_{15,10}$ is passed, that is to say, its output signal lasts until the first trailing edge. This may be obtained in known manner with the aid of bistable elements. This is the pulse in Figure 7a, it lasts approximately $256 \mu s$ from the instant of resetting divider circuit 15. Since $\Delta t \approx 256 \mu s$, this is exactly the duration which is at least required. As soon as the state with divisor 625 is achieved, there applies

that $Q=0$ and $\bar{Q}=1$. Switch 36 then conducts while switch 35 is cut off so that the output signal from gate 38 is the first positive half period of signal $Q_{15,10}$. This is the pulse in Figure 7c and it lasts approximately $512 \mu s$ from the instant of resetting divider circuit 15. As a result, it is insured that the pulse in Figure 7b in any case completely coincides therewith while the output signal from gate 38, hence from pulse shaper 17, is always suitable for controlling the field output stage 18. The flyback period thereof is in fact shorter than approximately 1 ms.

Figure 7b shows that the largest possible time difference between the leading edges of the pulses is slightly shorter than approximately $256 \mu s$, i.e. $\frac{0.256}{20} \approx 1.3\%$ of a field

period. This slight deviation is maintained as long as the occurred on-phase state lasts and produces a deviation in the vertical position of the image. It may be noted that this value, as well as the maximum duration of the pull-in process, emanates from the difference between the two divi-

sors 633 and 625, i.e. $8=2^3$. A value different from 633 for the divisor in the off-phase state may, however, be chosen. Instead of applying signal $Q_{15,10}$ to adjusting gate 16, the supply of signal $Q_{15,10}$ to this gate may be interrupted so that the divisor becomes $625-2^4=609$. In this case, the time difference Δt in Figure 7b lasts approximately $16 \times 32 \mu s = 512 \mu s$, so that the pull-in time has been reduced by 50% relative to the described case with a divisor of 633 while the minimum duration of the pulse in Figure 7a must also be $512 \mu s$. The extended pulse of Figure 7c then lasts at least approximately $700 \mu s$ which is still just suitable as a field control signal. The largest possible vertical deviation is then, however, doubled.

Divisors other than 633 and 609 may be obtained by applying or not applying one or more output signals from the flipflops of divider circuit 15 to adjusting gate 16. For 633 the difference from the nominal divisor 625 is equal to $+2^3$ and for 609 it is -2^4 . The divisor 613, for example, corresponds to $-2^4+2^2=-12$ and may be realised by connecting for $Q=1$ the output of flipflop 15, to an input of gate 16 and by interrupting the connection between the output of flipflop 15, and the relevant input of gate 16. Divisors other than 625 are obtained in that the connection between at least one of the flipflops 15, 15a, 15b, 15c to gate 16 is interrupted and/or in that at least one of the other flipflops is connected to gate 16. The considerations regarding divisor 609 have, however, shown that the choice of the second divisor cannot be eliminated in practice, while it is evident that in practice the second divisor should not deviate too much from the nominal divisor 625. Moreover, divisors 633 and 609 can be obtained in the easiest manner.

It is to be noted that it may occur that coincidence takes place in stage 20 but not in memory element 25 due to the shorter duration of the pulse generated by trigger 24. However, in such a case, the divisor deviates from the value 625 so that the process described with reference to Figure 7 is effected.

Figure 9 shows another embodiment of the circuit arrangement according to the invention in which a higher value than the nominal value 625, namely 633, is chosen for the divisor in the off-phase state. This embodiment is based on the following recognition. There are some test signal generators in which the number of lines per image is not 625 but, for example, 624, so that the displayed image is not interlaced. They are used, for example, for adjusting the convergence in colour television receivers. When using video recorders, it may occur that, for example, when displaying a stationary

image, the number of line synchronising pulses per image slightly deviates from 625. Field synchronisation with the known circuit arrangement is impossible when such "non-standard signals" are received. The object of the embodiment of Figure 9 is to establish synchronisation in such a case and for this purpose the direct synchronisation is used while the frequency divider circuit is set to the state with divisor 633. Since this state corresponds to a lower frequency than the nominal one, the direct synchronisation is possible while the drawbacks thereof do not in most cases apply because the received signal often comprises little noise and interferences.

The embodiment of Figure 9 comprises parts which also occur in those of the previous Figures and which have the same reference numerals. In Figure 9, 39 denotes a switch which may be, for example, manually operated and which is closed when the above-mentioned non-standard signals are received. As a result, the delay introduced by integrator 21 is reduced, for example, by making a time constant associated with this integrator shorter or by switching off integrator 21 completely. Coincidence stage 20 thus does not have any effect any longer. Also, the closure of switch 39 renders the input voltage of an amplifier 40 "high" so that its output voltage likewise becomes "high" ($=0$). Under these circumstances, a controlled switch 41 which is connected to the output of a trigger 24 starts to conduct so that the pulses originating from the trigger are passed and reach an input of an AND gate 42. Another input thereof is connected to the output of gate 16 and the output thereof is connected to the reset line 28 of the ten flipflops of divider circuit 15. The output voltage from amplifier 40 is also applied to an inverter stage 43 whose output voltage is "low" ($=1$) when switch 39 is closed and is applied to an input of an OR gate 44. Another input of gate 44 is connected to the output of integrator 21 and its output is connected to the input of level detector 22. Furthermore, the output of inverter stage 43 is also connected to an extra input of OR gate 33.

Under the circumstances described, gates 44 and 33 do not provide any signal ($=1$). The output signal from level detector 22 becomes 0 so that the controlled switch 23 conducts. Synchronising pulses originating from trigger 24 are passed on to OR gate 32. If they do not already have the values

$Q=1$ and $\bar{Q}=0$, the output signals from flipflop 29 consequently become $Q=1$ and $\bar{Q}=0$. This is the state as described with reference to Figure 6 for which frequency divider circuit 15 should be reset after the

633rd period of oscillator 11. In fact, the output signal from gate 16 then is 0 so that signal S28 is likewise 0. Before the 633rd period, however, a received field synchronising pulse is present through switch 41 at the relevant input of gate 42 ($=0$) so that $S28=0$. Divider circuit 15 is thereby reset.

When standard signals are received (that is to say with 625 lines per image) switch 39 is open so that integrator 21 has the original time constant whilst switch 41 is cut off. Received field synchronising pulses can no longer reach gate 42. The output signal from inverter stage 43 is 0 so that those from OR gates 44 and 33 only depend on the signals from integrator 21 and switch 23, respectively. The circuit arrangement of Figure 9 operates in the same way as those of Figures 1 and 2. It may be noted that the extension of the duration of the divider pulse after the occurrence of the on-phase state in case of reception of non-standard signals is not effected in the embodiment of Figure 9 because signal Q remains equal to 1. This is no drawback because in the most cases little noise and interference are received.

Negative logic is employed in the foregoing. It is evident that this choice is not important for the essence of the invention. For positive logic only the denomination of the logic gates shown in the Figure would have to be changed in known manner.

Elements 10 to 13, 15 to 17, 20 to 26 and 39 to 44 of the described circuit arrangements, with the exception of a capacitor possibly associated with integrator 21, may be advantageously integrated in a semiconductor body. In view of the large number of components thereof, it is evident that a non-integrated embodiment would not be economical. It may be noted that the described frequency divider circuit and the memory element consist of binary elements. Embodiments of the same scope as described are, however, feasible, using elements of different types.

A television system employing 625 lines per image, two interlaced rasters per image and 50 fields per second has been taken as an example in the foregoing. It will be evident that modifications of the circuit arrangement according to the invention without an essential difference are possible for the reception of television signals in accordance with a different system.

WHAT WE CLAIM IS:—

1. A circuit arrangement for generating a control signal for the field time base stage in a television receiver for a system in which a plurality of fields constitutes an image, said arrangement comprising a generator for generating a signal whose frequency is the line frequency or an integral multiple of

image, the number of line synchronising pulses per image slightly deviates from 625. Field synchronisation with the known circuit arrangement is impossible when such "non-standard signals" are received. The object of the embodiment of Figure 9 is to establish synchronisation in such a case and for this purpose the direct synchronisation is used while the frequency divider circuit is set to the state with divisor 633. Since this state corresponds to a lower frequency than the nominal one, the direct synchronisation is possible while the drawbacks thereof do not in most cases apply because the received signal often comprises little noise and interferences.

The embodiment of Figure 9 comprises parts which also occur in those of the previous Figures and which have the same reference numerals. In Figure 9, 39 denotes a switch which may be, for example, manually operated and which is closed when the above-mentioned non-standard signals are received. As a result, the delay introduced by integrator 21 is reduced, for example, by making a time constant associated with this integrator shorter or by switching off integrator 21 completely. Coincidence stage 20 thus does not have any effect any longer. Also, the closure of switch 39 renders the input voltage of an amplifier 40 "high" so that its output voltage likewise becomes "high" (=0). Under these circumstances, a controlled switch 41 which is connected to the output of a trigger 24 starts to conduct so that the pulses originating from the trigger are passed and reach an input of an AND gate 42. Another input thereof is connected to the output of gate 16 and the output thereof is connected to the reset line 28 of the ten flipflops of divider circuit 15. The output voltage from amplifier 40 is also applied to an inverter stage 43 whose output voltage is "low" (=1) when switch 39 is closed and is applied to an input of an OR gate 44. Another input of gate 44 is connected to the output of integrator 21 and its output is connected to the input of level detector 22. Furthermore, the output of inverter stage 43 is also connected to an extra input of OR gate 33.

Under the circumstances described, gates 44 and 33 do not provide any signal (=1). The output signal from level detector 22 becomes 0 so that the controlled switch 23 conducts. Synchronising pulses originating from trigger 24 are passed on to OR gate 32. If they do not already have the values

$Q=1$ and $\overline{Q}=0$, the output signals from flipflop 29 consequently become $Q=1$ and

$\overline{Q}=0$. This is the state as described with reference to Figure 6 for which frequency divider circuit 15 should be reset after the

633rd period of oscillator 11. In fact, the output signal from gate 16 then is 0 so that signal S28 is likewise 0. Before the 633rd period, however, a received field synchronising pulse is present through switch 41 at the relevant input of gate 42 (=0) so that $S28=0$. Divider circuit 15 is thereby reset.

When standard signals are received (that is to say with 625 lines per image) switch 39 is open so that integrator 21 has the original time constant whilst switch 41 is cut off. Received field synchronising pulses can no longer reach gate 42. The output signal from inverter stage 43 is 0 so that those from OR gates 44 and 33 only depend on the signals from integrator 21 and switch 23, respectively. The circuit arrangement of Figure 9 operates in the same way as those of Figures 1 and 2. It may be noted that the extension of the duration of the divider pulse after the occurrence of the on-phase state in case of reception of non-standard signals is not effected in the embodiment of Figure 9 because signal Q remains equal to 1. This is no drawback because in the most cases little noise and interference are received.

Negative logic is employed in the foregoing. It is evident that this choice is not important for the essence of the invention. For positive logic only the denomination of the logic gates shown in the Figure would have to be changed in known manner.

Elements 10 to 13, 15 to 17, 20 to 26 and 39 to 44 of the described circuit arrangements, with the exception of a capacitor possibly associated with integrator 21, may be advantageously integrated in a semiconductor body. In view of the large number of components thereof, it is evident that a non-integrated embodiment would not be economical. It may be noted that the described frequency divider circuit and the memory element consist of binary elements. Embodiments of the same scope as described are, however, feasible, using elements of different types.

A television system employing 625 lines per image, two interlaced rasters per image and 50 fields per second has been taken as an example in the foregoing. It will be evident that modifications of the circuit arrangement according to the invention without an essential difference are possible for the reception of television signals in accordance with a different system.

WHAT WE CLAIM IS:—

1. A circuit arrangement for generating a control signal for the field time base stage in a television receiver for a system in which a plurality of fields constitutes an image, said arrangement comprising a generator for generating a signal whose frequency is the line frequency or an integral multiple of



the line frequency, a frequency divider circuit for dividing the signal output of said generator, means for applying received field synchronising pulses to a comparator stage for comparing the phase between said synchronising pulses and the pulses produced by said frequency divider circuit, said comparator stage being capable of applying a signal to a gate which signal is dependent on the phase difference between said compared pulses, said frequency divider circuit, dependent on an output signal from said gate, being switchable under the control of a memory element between first and second states, respectively having first and second divisors.

2. A circuit arrangement for generating a control signal for the field time base stage in a television receiver for a system in which a plurality of fields constitutes an image, said arrangement comprising a generator for generating a signal whose frequency is the line frequency or an integral multiple of the line frequency, said multiple being equal to the number of fields in an image, a frequency divider circuit for dividing the signal output of said generator, means for applying received field synchronising pulses to a comparator stage for comparing the phase between said synchronising pulses and pulses produced by said frequency divider circuit, said comparator stage being capable of applying a signal to a gate which signal is dependent on the phase difference between said compared pulses, said frequency divider circuit dependent on an output signal from said gate, being switchable under the control of a memory element between first and second states, respectively having first and second divisors, said first divisor being numerically equal to the number of lines per image whilst said second divisor differs from said first divisor, said memory element bringing and maintaining said frequency divider circuit in its first state when said compared pulses at least partly coincide but brings said frequency divider to its second state when said compared pulses have not coincided for a given period.

3. A circuit arrangement as claimed in Claim 1 or 2, in which an adjusting gate for adjusting the frequency divider circuit at the commencement of each field raster, has an input for controlling said frequency divider circuit by means of said memory element.

4. A circuit arrangement as claimed in Claim 1, 2 or 3, in which said memory element comprises a bistable element which receives reset pulses when said compared

pulses coincide at least partly and which receives set pulses when said compared pulses have not coincided for a given period.

5. A circuit arrangement as claimed in Claim 4, in which said second divisor is numerically larger than said first divisor, means being provided by which said bistable element in the memory element cannot receive reset pulses, said frequency divider circuit being adjustable by means of received field synchronising pulses.

6. A circuit arrangement as claimed in Claim 1, 2, 3, 4 or 5, in which a pulse shaper is provided whose pulsatory output signal is applied to said comparator stage, said memory element bringing said pulse shaper to a first state to bring said frequency divider circuit to its first state, the duration of the output pulse from the pulse shaper in its first state being longer than in a second state to which said pulse shaper is brought by said memory element when it brings said frequency divider circuit to its second state.

7. A circuit arrangement as claimed in Claim 6, in which said frequency divider circuit consists of bistable elements, said pulse shaper including a keyed gate which in its first state receives the output signal from a bistable element and in its second state receives the output signal from another bistable element, the period of the first-mentioned output signal being longer than the period of the latter-mentioned signal, the output signal from said keyed gate being the first half period of the relevant output signal after the instant of resetting the frequency divider circuit.

8. A circuit arrangement as claimed in Claim 1 or 2, in which said frequency divider circuit consists of bistable elements, the outputs of a plurality of said bistable elements being connected to inputs of an adjusting gate for adjusting the frequency divider circuit at the commencement of each field raster, a controllable switch being incorporated in at least one of the connections thus formed, which switch may be controlled by said memory element.

9. A circuit arrangement as claimed in Claim 8, in which said first divisor differs from said second divisor by 2^n , where n is an integer.

10. A circuit arrangement as claimed in any of the preceding Claims, in which at least the frequency divider circuit, the adjusting gate, the memory element and the pulse shaper are integrated in a semiconductor body.

11. A circuit arrangement for generating a control signal for the field time base stage



in a television receiver, substantially as here-
in described with reference to the accom-
panying drawings.

- 5 12. A television receiver comprising a
field control circuit as claimed in any of the
preceding Claims.

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