CLAIMS

1. An interposer-less multi-chip module, comprising:

a substrate;

a base film disposed on the substrate; and

chips pressed into the base film, wherein the chips have varying thicknesses, and wherein top surfaces of the chips are coplanar.

2. The interposer-less multi-chip module of claim 1, wherein the base film comprises a material selected from the group consisting of: spin-on-glass, a doped polymer, and combinations thereof.

3. The interposer-less multi-chip module of claim 1, wherein the base film is cross-linked.

4. The interposer-less multi-chip module of claim 1, wherein the substrate comprises a silicon (Si) wafer.

5. The interposer-less multi-chip module of claim 1, wherein the chips comprise upward facing metal landing pads.

6. An interposer-less multi-chip module, comprising:

a substrate;

a base film disposed on the substrate;

chips pressed into the base film, wherein the chips have varying thicknesses, and wherein the chips are pressed into the base film to different depths such that top surfaces of the chips are coplanar; and

an interconnect layer present on the substrate over the chips, wherein the interconnect layer comprises back-end-of line (BEOL) metal wiring.

7. The interposer-less multi-chip module of claim 6, wherein the base film comprises a material selected from the group consisting of: spin-on-glass, a doped polymer, and combinations thereof.

8. The interposer-less multi-chip module of claim 6, wherein the chips comprise upward facing metal landing pads, and wherein the BEOL metal wiring contacts the upward facing metal landing pads.

9. The interposer-less multi-chip module of claim 6, wherein the BEOL metal wiring provides bridge connections between the chips.

10. The interposer-less multi-chip module of claim 6, further comprising:
solder bumps present on the interconnect layer in contact with the metal wiring.

11. A method of forming an interposer-less multi-chip module, the method comprising:

depositing a base film onto a substrate;

placing chips on the substrate over the base film; pressing the chips into the base film using a presser such that top surfaces of the chips are coplanar; and

curing the base film to cross-link the base film.

12. The method of claim 11, wherein the base film comprises a material selected from the group consisting of: spin-on-glass, a doped polymer, and combinations thereof.

13. The method of claim 11, wherein the presser comprises a planar surface spanning all of the chips.

14. The method of claim 11, wherein the chips have varying thicknesses.

15. The method of claim 11, wherein the chips comprise upward facing metal landing pads.

16. The method of claim 11, wherein curing the base film comprises annealing the substrate at a temperature of from about 100º C. to about 500º C. and ranges therebetween, for a duration of from about 1 hour to about 5 hours and ranges therebetween.

17. A method of forming an interposer-less multi-chip module, the method comprising:

depositing a base film onto a substrate;

placing chips on the substrate over the base film, wherein the chips have varying thicknesses;

pressing the chips into the base film using a presser, wherein the presser presses the chips having the varying thickness into the base film to different depths such that top surfaces of the chips are coplanar;

curing the base film; and

forming an interconnect layer on the substrate over the chips, wherein the interconnect layer comprises BEOL metal wiring.

18. The method of claim 17, wherein the base film comprises a material selected from the group consisting of: spin-on-glass, a doped polymer, and combinations thereof.

19. The method of claim 17, wherein the presser comprises a planar surface spanning all of the chips.

20. The method of claim 17, wherein the chips comprise upward facing metal landing pads, and wherein the BEOL metal wiring contacts the upward facing metal landing pads.

21. The method of claim 17, wherein the BEOL metal wiring provides bridge connections between the chips.

22. The method of claim 17, further comprising:

forming solder bumps on the interconnect layer in contact with the metal wiring.

23. The method of claim 17, further comprising:

dicing the substrate into multiple segments, wherein each of the multiple segments comprises at least two of the chips.