zone 304 may be referred to as a curved bar profile deposition zone, and edge zones 302 may be referred to as a curved channel profile deposition zone.

[0053] The curved bar profile film 308 has a decreasing thickness along an x direction from center to edge of wafer 306 and a uniform, or substantially uniform, thickness along a y direction of the wafer. Conversely, the curved channel profile film 307 has an increasing thickness along the x direction from center to edge of wafer 306 and a uniform, or substantially uniform, thickness along a y direction of the wafer. Together, curved bar profile film 308 and curved channel profile film 307 may form a uniform thickness profile film or a complementary profile film stack. The complementary profile film stack has a thickness 309 based on the combined thickness of the curved channel profile film 307 and the curved bar profile film 308.

[0054] As film 307 and film 308 are deposited independently, each film may be deposited under conditions to have a different internal stress. For example, curved bar profile film 308 may have a compressive internal stress, while curved channel profile film 307 may have a tensile internal stress, or vice versa. As film stresses may be superimposed, the stacked film may have a compressive internal stress in areas of the film having a small x/large y coordinate, i.e., corresponding to center zone 304, while the stacked film also has a tensile internal stress in areas of the film having a large x/small y coordinate, i.e., coordinating to edge zones 302, or vice versa. As noted above, the center of the wafer may be considered the origin, e.g., x=0 and y=0.

[0055] While Figures 3B and 3C show a complementary profile film stack comprising one pair of curved channel profile film 307 and a curved bar profile film 308, a complementary profile film stack may comprise more than one pair of a curved channel profile film and a curved bar profile film. The curved channel profile film of a certain pair (e.g., a first pair) may have different properties such as a thickness, stress, stress ratio, materials, compositions, etc. from those of the curve channel profile film of the other pair (e.g., a second pair). Similarly, the curved bar profile film of a certain pair (e.g., the first pair) may have different properties such as a thickness, stress, stress ratio, materials, compositions, etc. from those of the curve bar profile film of the other pair (e.g., the second pair).

[0056] While films 307 and 308 are discussed herein as having opposite types of internal stress, e.g., one film has a compressive internal stress and the other film has a tensile internal stress, in some embodiments both films may have a tensile or compressive internal stress, but different magnitudes of internal stress. This may address wafers that have different magnitudes of x-bow and y-bow even if the both bows are positive or negative. In some embodiments depositing same type stress films may increase throughput.

comprise two or more sets of complementary profile films, e.g., two or more sets of a curved bar profile film 308 and a curved channel profile film 307.

[0060] In some embodiments, each of the curved bar profile films 308-1–N and curved channel profile films 307-1–M have the same profile, respectively. In other embodiments, the profiles of one or more non-uniform thickness profile film may be different from the other non-uniform thickness profile films. In some embodiments, a pair of complementary profile films may be defined by a thickness 350, which refers to the thickness of the pair of complementary profile films (e.g., a combination of a curved bar profile film and a curved channel profile film). A thickness 350 of the pair of complementary profile films may be less than about 1 μm or between about 0.5 μm and about 1 μm. In some embodiments, each pair of complementary profile films in an alternating film stack may have the same thickness, which for a four-bilayer stack shown in Figure 3D may have a total thickness between about 2 μm and about 4 μm. In some embodiments, each pair of complementary profile films in an alternating stack may have different thickness.

[0061] Figure 3D presents an illustration where a curved bar profile film 308 is deposited after a curved channel profile film 307 is deposited, which is then repeated four times to provide an alternating stack of 4 pairs of complementary profile films. Figure 3E presents a similar stack except that a curved bar profile film 308-1 is deposited before a curved channel profile film 307-1 is deposited, instead of after. As described above, the number of layers and the thickness profiles illustrated in these figures are exemplary only. More or less than four pairs of the complementary profile films are deposited to optimize the overall bow of the wafer. An additional tensile or compressive internal stress layer may also be added, in between the pair of the complementary films, or as the last layer, as illustrated in Figures 3F and 3G.

[0062] Figures 3F and 3G present illustrations of cap or filler layers that may be deposited. In Figure 3F, a cap layer 341 that has a uniform, or substantially uniform, thickness is deposited. As will be discussed further below, cap layer 341 may be a uniform thickness profile film having a tensile internal stress, a compressive internal stress, or zero or negligible internal stress. A uniform thickness profile film may be deposited after depositing one or more pairs of complementary profile films. In some embodiments, a uniform thickness profile film may be deposited between pairs of the alternating stack of complementary profile films. For example, complementary profile films as described herein may be used to compensate for saddle-shaped wafer bow, e.g., a positive x-bow and negative y-bow. While complementary profile films may reduce the difference in wafer bow between the x-direction and y-direction, the wafer bow from a reference plane (e.g., an xy plane intersecting the wafer) may still be relatively large, e.g., 200 μm or more. For example, a saddle-shaped wafer may have backside layers deposited thereon that change the shape to a bowl

or dome shaped wafer. The difference between x-bow and y-bow is reduced, but the wafer is still bowed. A uniform thickness profile cap layer may compensate for such a wafer bow by having a uniform tensile internal stress or compressive internal stress. As the x-bow and y-bow have been substantially equalized by the complementary profile films, the uniform thickness profile film may thus compensate the remaining wafer bow.

[0063] Figure 3G presents an illustration of a filler layer 345. During deposition of a curved bar profile film 308, a curved bar profile film may have a "center drop," where the thickness of the film has two maxima offset from a center position of the film at or near radius zero (i.e., at or near the wafer center), and at radius zero the thickness of the film is less than the maxima. This difference in thickness may be insubstantial for small thicknesses of complementary profile films, e.g., less than about 1μm. However, for larger thicknesses of a complementary profile film stack or an alternating stack of complementary profile films having a large overall thickness, e.g., greater than about 2 μm or greater than about 2.5 μm, the center drop may become noticeable and affect the flatness of the film. Thus, a filler layer 345 may be deposited to fill the gap formed in the curved bar profile film. In some embodiment, a filter layer 344 may be deposited to fill the gap formed in the curved channel profile film, for example, where the alternating stack film 340 is formed similarly to that of Figure 3D. Filler layer 345 may be deposited using similar techniques as curved bar profile 344 with a sharper taper in thickness as a function of radius.

[0064] In some embodiments, an alternating stack of complementary profile films may have pairs of complementary profile films having different properties such as thickness, stress, stress ratio, materials, compositions, etc., Figure 3H illustrates an alternating stack of complementary profile films where the order of deposition for pairs of complementary profile films changes. Curved channel profile film 327-1 is deposited first, followed by curved bar profile films 328-1 and 328-2. In some embodiments, curved bar profile film 328-1 and curved bar profile film 328-2 may have different properties as described herein or the same properties. Then, a curved channel profile film 327-2 may be deposited last and may, in some embodiments, have different properties as described herein or the same properties as curved channel profile film 327-1.

[0065] Figure 3I illustrates another alternating stack of complementary profile films where the order of deposition for pairs of complementary profile films changes. In Figure 3I, curved bar profile film 338-1 is deposited first, followed by curved channel profile films 337-1 and 337-2. In some embodiments, curved channel profile film 337-1 and curved channel profile film 337-2 may have different properties as described herein or the same properties. Then, a curved bar profile film 338-2 may be deposited last and may, in some embodiments, have different properties as described herein or the same properties as curved bar profile film 338-1.

backside of the wafer. Such one or more layers may be patterned. In some embodiments, shape may be defined by an x-bow and y-bow. In other embodiments, wafer shape may also be determined by internal stresses of the incoming wafer, particularly along perpendicular directions of the wafer, e.g., an x-direction and y-direction. In some embodiments, a wafer shape is selected from a pre-determined group of wafer shapes to best match a wafer being analyzed. For example, wafer bow of production wafers may be influenced by multiple different frontside layers that are computationally intensive to simulate, but can be sufficiently modelled by a single internal stress value for perpendicular directions and a corresponding polynomial function to define a stress distribution in the perpendicular directions. In some embodiments, an incoming wafer may be modelled by selecting a pre-determined wafer shape that best approximates the incoming wafer shape or by modelling the incoming wafer shape using simplified models of internal stress to approximate the incoming wafer shape.

[0093] One or more complementary profile film stack recipes may be selected (704). The recipes selected may be based upon the shape of the incoming wafer. For example, as noted above in relation to Figure 5C, the optimal stress ratio of a complementary profile film stack may depend on the incoming wafer shape. As the incoming wafer shape is known, certain complementary profile film stacks may be filtered and not simulated as they are already known to have poor performance. For example, if an incoming wafer shape was similar to incoming shape 502b, a complementary profile film stack similar to stack film A may not be selected, while stack film B is selected.

[0094] The wafer shape and selected complementary profile film stack recipes are simulated (706). The simulations may involve determine a compensated shape similar to those shown in Figures 5A and 5B. The simulations may also involve determining a flattening possible by each complementary profile film stack, similar to that shown in Figures 6A and 6B. Various data may be derived from the simulations, such as the efficiency of each complementary profile film stack and the minimum delta bow as a function of thickness for each complementary profile film stack.

[0095] In some embodiments, a cap layer may also be optionally simulated (708). The cap layer may be simulated for determining efficiency, thickness, and/or minimum delta bow. For efficiency, the cap layer may be combined with the complementary profile film stack to determine an average efficiency of the total backside film stack. For delta bow, that cap layer may be combined with the complementary profile film stack to determine a minimum thickness achievable when using a both a complementary profile film stack and the cap layer, similar to the charts shown in Figure 6C.

different cap layers may be simulated, including various magnitudes of internal stress and various thicknesses.

[0105] The properties of the simulated compensated wafers may then be determined (810). In some embodiments, properties may include the final wafer bow, including the delta bow as well as the x-bow and y-bow. In some embodiments properties may include an efficiency of each complementary profile film stack when applied to each incoming wafer shape. In some embodiments, properties may include a flattening percentage of each complementary profile film stack when applied to each incoming wafer shape (e.g., a percent reduction in delta bow) or a residual bow of the wafer after applying the complementary profile film stack (e.g., a percent of the original delta bow remaining). In some embodiments, properties may also include an optimal thickness or optimal stress ratio for each incoming wafer shape. The complementary profile film stack having the greatest efficiency or the greatest flattening percentage for a particular incoming wafer shape may be determined.

[0106] The relationships between complementary profile film stacks and incoming wafer shapes may be modelled (812). In some embodiments, modelling may include generating charts of efficiency vs stress ratio as shown in Figure 4C or charts of residual bow vs film thickness as shown in Figure 5C. In some embodiments, modelling may involve determining one or more relationships between incoming wafer shapes and backside film stacks, including complementary profile film stacks and cap layers. In some embodiments, relationships modelled may include stress ratios of complementary profile film stacks to stress ratios of frontside films for incoming wafer shapes. These models and relationships may then be used as shown in Figure 6 to identify which process recipe to use to compensate an incoming wafer bow.

[0107] In some embodiments, the simulated combinations of incoming wafer shapes and complementary profile film stacks may be calibrated against empirical data. A depth of experiment (DOE) may be performed on coupon wafers to determine the deposition profiles of non-uniform profile films as well as on coupon wafers having frontside films deposited thereon to simulate incoming wafer shapes. The deposition profile of the experimental films and the deposition profile of the simulated films may be compared and the model calibrated to minimize differences between the simulated deposition profile and the experimental deposition profile. In some embodiments, the model may be refined to minimize a cost function between the simulated deposition profile and the experimental deposition profile.

[0108] In some embodiments, simulations described herein may be performed using a FEM modelling software. Figure 9 illustrates a graphical user interface for a FEM model that can

carrier ring 1054 may therefore be lifted along with the wafer 1002. In some implementations, the carrier ring 1054 may be rotated to another station, e.g., in a multi-station system. In some embodiments, a spider forks or any other transfer mechanism may be used to lift or move the wafer directly without a carrier ring.

[0124] Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead 1036) and a ShoPed 1006. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination of showerhead and pedestal, which enables deposition on a backside of the wafer. The electrode geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal or ShoPed may include an embedded controlled heater (or distributed heater or heater elements), wafer lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

[0125] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the ShoPed, showerhead, and/or electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0126] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0127] In some embodiments, the gap between the side of the wafer that does not need plasma/deposition may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 mm (limited by the wafer bow), and such gap can be controlled. The gap maybe controlled depending on process conditions.

[0128] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposition film in different areas of

the backside of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0129] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 1054 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0130] Figure 11A shows a cross-sectional view of an edge region of the ShoPed 1106. This view provides a cross-sectional representation of the carrier ring 1154, which has a carrier ring inner radius 1154a and a carrier ring outer radius 1154b. In some embodiments, the carrier ring 1154 includes support extensions 1154c, which extend below the substantial flat surface of the carrier ring 1154.

[0131] The support extensions 1154c are configured to mate and sit within support surfaces defined into a top surface of the spacers 1144. The support surfaces provide a complementary mating surface for the support extensions 1154c, such that the carrier ring 1154 is prevented from sliding or moving when supported by the spacers 1144. Although three spacers are shown as spacers 1144 are shown in Figure 11B, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 1106, and spacing is defined for supporting wafer 1102 at a spaced apart relationship from a top surface of the ShoPed 1106.

[0132] Further shown is that a top surface of the ShoPed 1106 will include a hole pattern 1106a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 1106a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 1106 and extend to an outer periphery of the ShoPed 1106. At least one hole pattern 1106a is provided at an edge hole region 1107 of

the hole pattern, and orifices defined in the edge hole region 1107 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 1106.

[0133] In one example, the angle or tilt at which the orifices in the edge hole region 1107 is defined to tilt or angle away from the center of the ShoPed 1106. In one embodiment, the angle is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 1107, additional distribution of process gases can be provided during backside deposition of the wafer 1102. In one embodiment, the remainder orifices 1106d of the hole pattern 1106a are oriented substantially perpendicular to the surface of the ShoPed 1106 and directed toward the underside of the wafer 1102.

[0134] Figure 11B illustrates that when the wafer 1102 is held by the carrier ring 1154, the wafer 1102 edge will sit on an edge region closer to the carrier ring inner radius 1154a of the carrier ring 1154. The surface of the showerhead 1136 facing the top surface of the wafer 1102, when positioned using spacers 1144, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the wafer 1102.

[0135] By way of example, the distance between the top of the wafer 1102 and the surface of the showerhead 1136 is preferably between about 2 mm to about 0.5 mm, and in some embodiments about 1 mm to about 0.5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about 0.5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about 0.5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 1136 is configured to supply an inert gas flow over the top side of the wafer 1102 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 1106.

[0136] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., VECTOR® DT product lines and ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0137] Figure 12 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 1200 includes a transfer module 1203. The transfer module 1203 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 1203 is a multi-station reactor 1209 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-

the like. As used herein, data or other information provided in electronic format is available for storage on a machine and transmission between machines. Conventionally, data in electronic format is provided digitally and may be stored as bits and/or bytes in various data structures, lists, databases, etc. The data may be embodied electronically, optically, etc.

[0163] In certain embodiments, a machine learning model can each be viewed as a form of application software that interfaces with a user and with system software. System software typically interfaces with computer hardware and associated memory. In certain embodiments, the system software includes operating system software and/or firmware, as well as any middleware and drivers installed in the system. The system software provides basic non-task-specific functions of the computer. In contrast, the modules and other application software are used to accomplish specific tasks. Each native instruction for a module is stored in a memory device and is represented by a numeric value.

[0164] An example computer system 1300 is depicted in Figure 13. As shown, computer system 1300 includes an input/output subsystem 1302, which may implement an interface for interacting with human users and/or other computer systems depending upon the application. Embodiments of the invention may be implemented in program code on system 1300 with I/O subsystem 1302 used to receive input program statements and/or data from a human user (e.g., via a GUI or keyboard) and to display them back to the user. The I/O subsystem 1302 may include, e.g., a keyboard, mouse, graphical user interface, touchscreen, or other interfaces for input, and, e.g., an LED or other flat screen display, or other interfaces for output. Other elements of embodiments of the disclosure may be implemented with a computer system like that of computer system 1300, perhaps, however, without I/O.

[0165] Program code may be stored in non-transitory media such as persistent storage 1310 or memory 1308 or both. One or more processors 1304 reads program code from one or more non-transitory media and executes the code to enable the computer system to accomplish the methods performed by the embodiments herein, such as those involved with generating or using a process simulation model as described herein. Those skilled in the art will understand that the processor may accept source code, such as statements for executing training and/or modelling operations, and interpret or compile the source code into machine code that is understandable at the hardware gate level of the processor. A bus couples the I/O subsystem 1302, the processor 1304, peripheral devices 1306, memory 1308, and persistent storage 1310.

[0166] In various embodiments, the computer system 1300 may be part of or connected to a controller that is employed to control process conditions during various etch and deposition