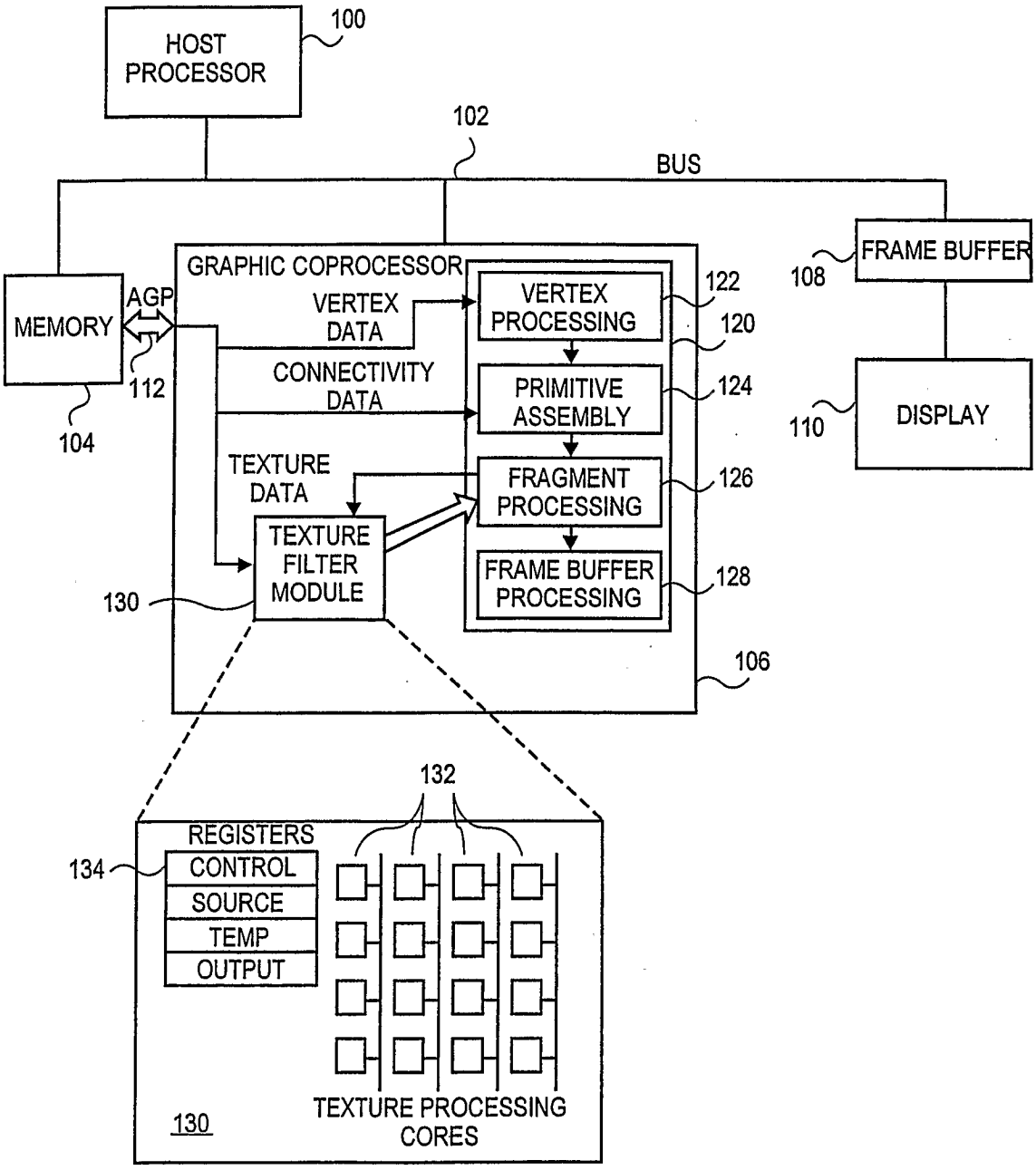
HOST PROCESSOR
100
102
BUS
FRAME BUFFER
108
GRAPHIC COPROCESSOR
MEMORY
AGP
112
104
VERTEX DATA
CONNECTIVITY DATA
TEXTURE DATA
VERTEX PROCESSING
122
120
PRIMITIVE ASSEMBLY
124
FRAGMENT PROCESSING
126
FRAME BUFFER PROCESSING
128
TEXTURE FILTER MODULE
130
106
DISPLAY
110
132
REGISTERS
134
CONTROL
SOURCE
TEMP
OUTPUT
130
TEXTURE PROCESSING CORES

FIG. 1A

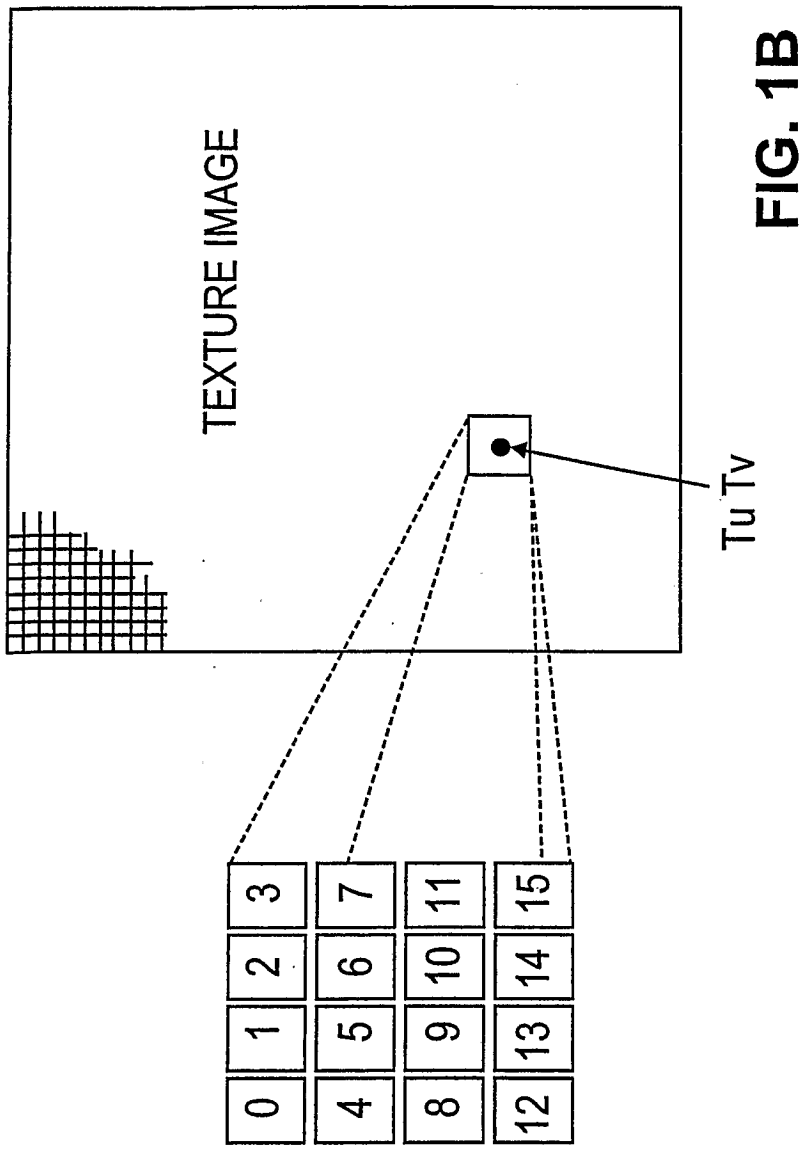

FIG. 1B

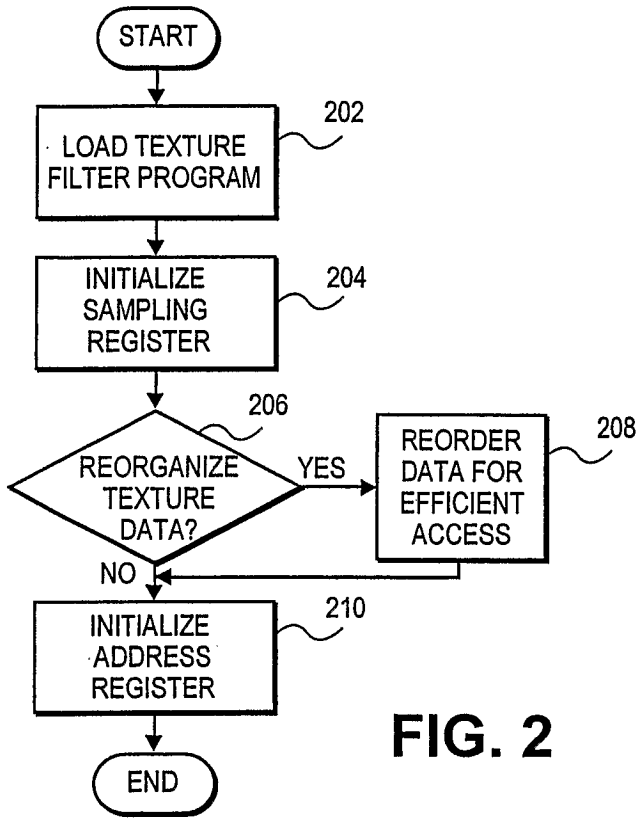
START
LOAD TEXTURE FILTER PROGRAM
202
INITIALIZE SAMPLING REGISTER
204
206
REORGANIZE TEXTURE DATA?
YES
REORDER DATA FOR EFFICIENT ACCESS
208
NO
INITIALIZE ADDRESS REGISTER
210
END

FIG. 2

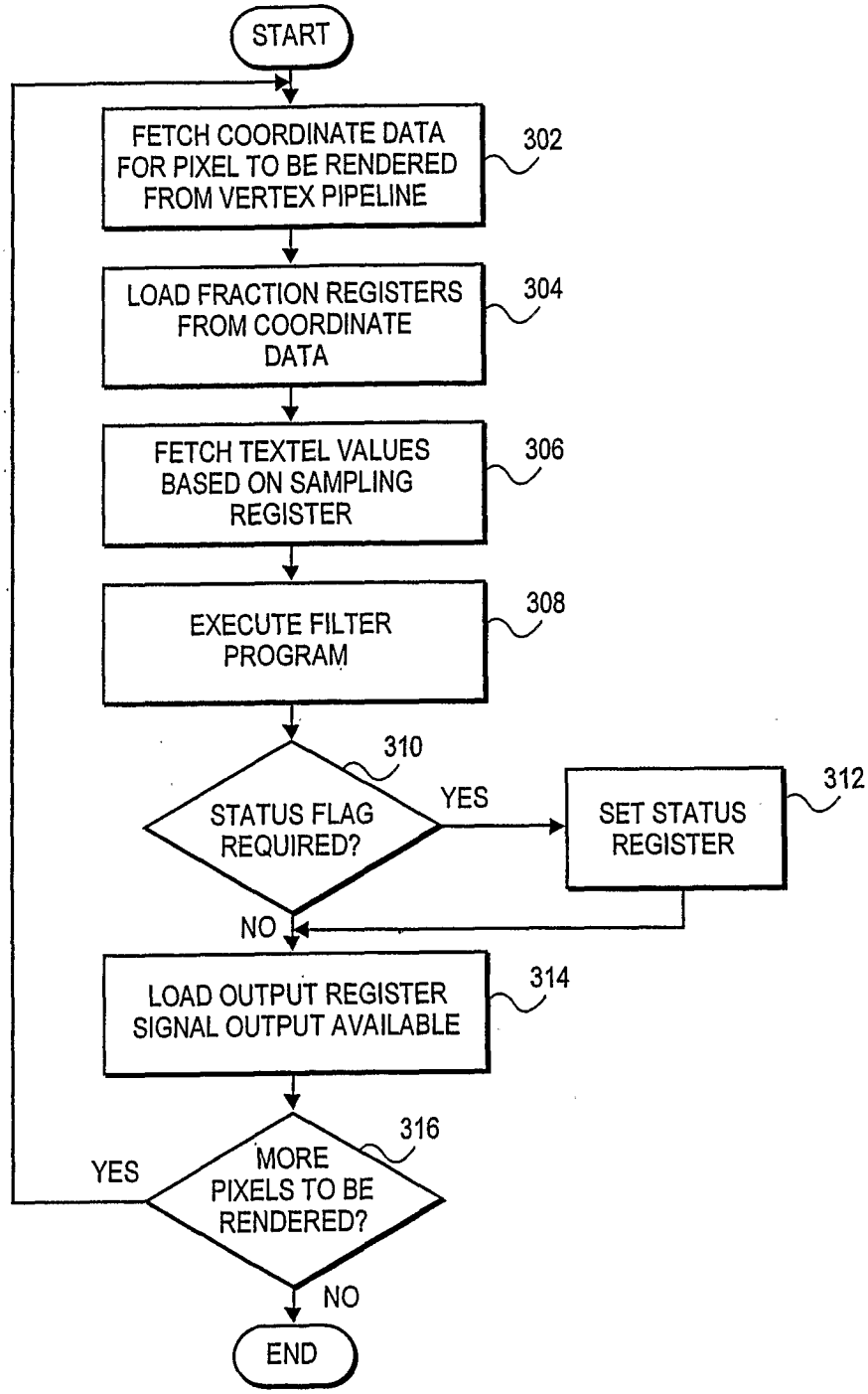
START
FETCH COORDINATE DATA FOR PIXEL TO BE RENDERED FROM VERTEX PIPELINE
302
LOAD FRACTION REGISTERS FROM COORDINATE DATA
304
FETCH TEXTEL VALUES BASED ON SAMPLING REGISTER
306
EXECUTE FILTER PROGRAM
308
310
STATUS FLAG REQUIRED?
YES
SET STATUS REGISTER
312
NO
LOAD OUTPUT REGISTER SIGNAL OUTPUT AVAILABLE
314
316
MORE PIXELS TO BE RENDERED?
YES
NO
END

FIG. 3