

CLAIMS

1. A method, implemented at a computer system that includes one or more processors, for performing breakpoint detection via a cache, the method comprising:
 - detecting an occurrence of a memory access; and
 - based at least on detecting the occurrence of the memory access, identifying whether any cache line of the cache matches an address associated with the memory access, and
 - when a cache line does match the address associated with the memory access, determining that no breakpoint was encountered; or
 - when no cache line matches the address associated with the memory access, identifying whether any cache line matches the address associated with the memory access when one or more flag bits are ignored, and
 - when a cache line does match the address associated with the memory access when the one or more flag bits are ignored, performing a check for whether a breakpoint was encountered; or
 - when no cache line matches the address associated with the memory access when the one or more flag bits are ignored, processing a cache miss.
2. The method of claim 1, further comprising, when no cache line matches the address associated with the memory access when the one or more flag bits are ignored, determining whether a cache line imported into the cache based on processing the cache miss overlaps with any address from a monitoring collection.
3. The method of claim 2, further comprising, when the cache line imported into the cache overlaps with an address from the monitoring collection, setting a flag bit on the cache line.
4. The method of claim 1, wherein performing the check for whether a breakpoint was encountered comprises determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.
5. The method of claim 4, wherein the monitoring collection is stored in system memory.
6. The method of claim 4, wherein the monitoring collection is stored in a processor memory.
7. The method of claim 6, wherein the processor memory comprises a cache coherence protocol directory.
8. The method of claim 1, wherein performing the check for whether a breakpoint was encountered comprises consulting a translation look aside buffer to

determine if a page table corresponding to the memory address contains any monitored memory address.

9. The method of claim 8, further comprising, when the page table corresponding to the memory address does contain a monitored memory address, determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.

10. The method of claim 1, wherein performing the check for whether a breakpoint was encountered comprises placing an address of the cache line into a hardware debug register.

11. A computer system, comprising:
one or more processors; and
one or more computer-readable media having stored thereon computer-executable instructions that configure the one or more processors to perform breakpoint detection via a cache, including at least:

detecting an occurrence of a memory access; and

based at least on detecting the occurrence of the memory access, identifying whether any cache line of the cache matches an address associated with the memory access, and

when a cache line does match the address associated with the memory access, determining that no breakpoint was encountered; or

when no cache line matches the address associated with the memory access, identifying whether any cache line matches the address associated with the memory access when one or more flag bits are ignored, and

when a cache line does match the address associated with the memory access when the one or more flag bits are ignored, performing a check for whether a breakpoint was encountered; or

when no cache line matches the address associated with the memory access when the one or more flag bits are ignored, processing a cache miss.

12. The computer system of claim 11, wherein the one or more processors comprise the computer-readable media and the cache, and wherein the computer-executable instructions comprise processor microcode.

13. The computer system of claim 11, the computer-executable instructions also configuring the one or more processors to determine whether a cache line imported into the cache based on processing the cache miss overlaps with any address from a monitoring

collection when no cache line matches the address associated with the memory access when the one or more flag bits are ignored.

14. The computer system of claim 11, wherein performing the check for whether a breakpoint was encountered comprises determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.

15. The computer system of claim 14, wherein the monitoring collection is stored in a processor memory.