(11) 1 595 801

1 595 801

(21) Application No. 92/77 (22) Filed 4 Jan. 1977
(23) Complete Specification filed 16 Dec. 1977
(44) Complete Specification published 19 Aug. 1981
(51) INT. CL.³ H04N 1/40
(52) Index at acceptance
H4F GX S25R S30H S30K S30T
(72) Inventor HENRY LOUIS BAKER

(19)

PATENT SPECIFICATION

(54) IMPROVEMENTS IN OR RELATING TO TELEVISION SYSTEMS

(71) We, COMMUNICATIONS PATENTS LIMITED, a British Company of Carlton House, Lower Regent Street, London SW1 4LS, England, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:–

The present invention relates to television systems, and in particular to systems for the display and storage of high contrast television pictures.

In a known television system for transmitting and displaying written information, a plurality of television cameras are used to transmit frame sequentially pictures of display boards on which they are severally focussed. An electromechanical frame snatcher or grabber is used to select and retain for display any one selected frame. It has been found that the contrast of the displayed television pictures is not satisfactory, particularly when information is written on the display boards in chalk or the like as occure for example in stock exchange displays. Furthermore, the reliability of the frame grabber is doubtful in view of its electromechanical structure, and its cost and size are excessive.

According to the present invention, there is provided a device for enhancing the contrast in television pictures comprising means for converting an analogue video signal into a two-level signal, the two levels of which correspond to the amplitude of the analogue video signal being above or below a predetermined threshold amplitude respectively, means for determining the positions of the respective levels in a frame, means for storing information representative of the determined positions of the respective levels in a frame, and means for reading out the stored information to recreate the frame, wherein the position determining means comprise means for identifying the co-ordinates of each transition between levels of the two level signal, and the storing means comprise a digital store in which the identified co-ordinates of each transition are stored in sequence, the reading out means being adapted to sequentially scan the contents of the digital store to recreate the frame.

The two levels may correspond with "black" and "white" respectively so that when a picture of a blackboard is displayed the surface of the board will appear black even if it has been smeared with chalk as the result of erasures. On the other hand, information written on the board will appear white even if not particularly clearly written providing the threshold amplitude is exceeded.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawing.

The illustrated embodiment of the invention comprises two comparators 1, 2 to which an analogue video input signal 3 is applied. The comparator 1 receives a reference input 4 from an adjustable potentiometer 5 and provides an output 6 in the form of a sequence of pulses the durations of which correspond with the times during which the amplitude of the picture content of the input 3 exceeds the reference "white" (input) preset potentiometer 5. The output 7 of comparator 2 comprises the line and field synchronizing pulses appearing on input 3.

The line and field synchronizing pulses on output 7 are separated by circuit 8, the field pulses appearing on output 9 and the line pulses on output 10. The black-white pulse sequence from comparator 1 is applied to an edge detector comprising buffer delays 11 and an exclusive OR gate 12. The output of gate 12 comprises a series of very short duration pulses each corresponding with the occurrence of a transition between the levels defined on either side of the reference 4. These transition identifying pulses trigger a monostable 13 which with switches 14 in the "record" position connecting to terminals 15 put a memory 16 into the write mode. The memory 16 comprises a 4096 by 16 bit random access memory.

With switches 14 in the "record" position connecting to terminals 15, the pulses from

gate 12 are counted by a twelve bit counter 17 which is reset to zero at the beginning of each field by the field synchronizing pulse output 9. The output of the counter 17 is used to address the memory 16.

The field synchronizing pulses are also applied via a delaying monostable 18 to reset to zero an eight bit counter 19 clocked by the line synchronizing pulse output 10 and the output of which forms the eight most significant bits (MSB) of the edge location data. The line synchronizing pulse output 10 also controls a 6MHz phase locked loop 20 and resets to zero a second eight bit counter 21 via a delaying monostable 22.

The counter 21 counts the 6MHz output of phase locked loop 20 and its output forms the eight least significant bits (LSB) of the edge location data. It will be realized that the sixteen bit edge location data is built up from two eight bit binary numbers the first of which denotes the line on which the edge occurs and the second the number of periods after a datum on that line which have elapsed before the occurrence of that edge, each period being for example 167 nano seconds. Thus the active picture area is divided into 256 locations on each of 256 lines. In the "record" mode the firing of the monostable 13 enables the writing into memory 15 of the sixteen bit location data of the corresponding edge.

With switches 14 in the "display" position connecting to terminals 23 the memory 16 operates in the read mode and its output is applied to a sixteen bit comparator 24 the other input of which is the sixteen bit location data sequence from counters 19 and 21. The memory addressing counter 17 is now clocked via switch 14 by the equality output of comparator 24.

At the beginning of each field the counter 17 is reset to zero and thus the output of the memory 16 comprises the sixteen bit location data of the first edge. When this is reached in the sequence being applied to the comparator 24, the comparator 24 produces an output pulse. This pulse clocks the addressing counter 17 to the next address and the read out continues. The field synchronizing pulse output 9 is used to reset to zero a D-type flip flop 25 arranged as a divide-by-two counter which is clocked by the equality output from comparator 24. The output 26 of flip flop 25 comprises a two-level video output.

At the beginning of each field the output 26 of flip-flop 25 is "0", corresponding with black level. At the time corresponding with the location of the first edge the output 26 changes to "1", corresponding with white level. The output 26 then alternates between black and white at times corresponding with the successive edge locations read out from the memory.

WHAT WE CLAIM IS:

1. A device for enhancing the contrast in television pictures, comprising means for converting an analogue video signal into a two-level signal, the two levels of which correspond to the amplitude of the analogue video signal being above or below a predetermined threshold amplitude respectively, means for determining the positions of the respective levels in a frame, means for storing information representative of the determined positions of the respective levels in a frame, and means for reading out the stored information to recreate the frame, wherein the position determining means comprise means for identifying the co-ordinates of each transition between levels of the two level signal, and the storing means comprise a digital store in which the identified co-ordinates of each transition are stored in sequence, the reading out means being adapted to sequentially scan the contents of the digital store to recreate the frame.

2. A device according to claim 1, comprising first and second comparators to each of which the analogue video signals are applied, the first comparator receiving a reference input which defines said threshold amplitude and the second comparator receiving a reference input such that the line and field synchronizing pulses of the analogue video signal appear at its output.

3. A device according to claim 2, wherein the output of the first comparator is applied to an edge detector in the form of a two input exclusive OR gate, one gate input receiving the comparator output direct and the other gate input receiving the comparator output via buffer delay circuits.

4. A device according to claim 3, wherein the output of the edge detection is applied to a monostable.

5. A device according to claim 4, comprising a first counter, a random access memory, and a switch actuable to connect the output of the edge detector to the clock input of the first counter and to connect the output of the monostable to the read/write input of the memory, the first counter being connected to the address inputs of the memory.

6. A device according to claim 5, wherein the output of the second comparator is applied to a pulse separating circuit which provides line pulses on a first output and synchronising pulses on a second output, the first output being connected to the clock input of a second counter, the clock input of a third counter via a phase locked loop circuit, and the reset input of the third counter via a monostable, and the second output being connected to the reset input of the second counter via a monostable and the reset input of the first counter,

gate 12 are counted by a twelve bit counter 17 which is reset to zero at the beginning of each field by the field synchronizing pulse output 9. The output of the counter 17 is used to address the memory 16.

The field synchronizing pulses are also applied via a delaying monostable 18 to reset to zero an eight bit counter 19 clocked by the line synchronizing pulse output 10 and the output of which forms the eight most significant bits (MSB) of the edge location data. The line synchronizing pulse output 10 also controls a 6MHz phase locked loop 20 and resets to zero a second eight bit counter 21 via a delaying monostable 22.

The counter 21 counts the 6MHz output of phase locked loop 20 and its output forms the eight least significant bits (LSB) of the edge location data. It will be realized that the sixteen bit edge location data is built up from two eight bit binary numbers the first of which denotes the line on which the edge occurs and the second the number of periods after a datum on that line which have elapsed before the occurrence of that edge, each period being for example 167 nano seconds. Thus the active picture area is divided into 256 locations on each of 256 lines. In the "record" mode the firing of the monostable 13 enables the writing into memory 15 of the sixteen bit location data of the corresponding edge.

With switches 14 in the "display" position connecting to terminals 23 the memory 16 operates in the read mode and its output is applied to a sixteen bit comparator 24 the other input of which is the sixteen bit location data sequence from counters 19 and 21. The memory addressing counter 17 is now clocked via switch 14 by the equality output of comparator 24.

At the beginning of each field the counter 17 is reset to zero and thus the output of the memory 16 comprises the sixteen bit location data of the first edge. When this is reached in the sequence being applied to the comparator 24, the comparator 24 produces an output pulse. This pulse clocks the addressing counter 17 to the next address and the read out continues. The field synchronizing pulse output 9 is used to reset to zero a D-type flip flop 25 arranged as a divide-by-two counter which is clocked by the equality output from comparator 24. The output 26 of flip flop 25 comprises a two-level video output.

At the beginning of each field the output 26 of flip-flop 25 is "0", corresponding with black level. At the time corresponding with the location of the first edge the output 26 changes to "1", corresponding with white level. The output 26 then alternates between black and white at times corresponding with the successive edge locations read out from the memory.

WHAT WE CLAIM IS:

1. A device for enhancing the contrast in television pictures, comprising means for converting an analogue video signal into a two-level signal, the two levels of which correspond to the amplitude of the analogue video signal being above or below a predetermined threshold amplitude respectively, means for determining the positions of the respective levels in a frame, means for storing information representative of the determined positions of the respective levels in a frame, and means for reading out the stored information to recreate the frame, wherein the position determining means comprise means for identifying the co-ordinates of each transition between levels of the two level signal, and the storing means comprise a digital store in which the identified co-ordinates of each transition are stored in sequence, the reading out means being adapted to sequentially scan the contents of the digital store to recreate the frame.

2. A device according to claim 1, comprising first and second comparators to each of which the analogue video signals are applied, the first comparator receiving a reference input which defines said threshold amplitude and the second comparator receiving a reference input such that the line and field synchronizing pulses of the analogue video signal appear at its output.

3. A device according to claim 2, wherein the output of the first comparator is applied to an edge detector in the form of a two input exclusive OR gate, one gate input receiving the comparator output direct and the other gate input receiving the comparator output via buffer delay circuits.

4. A device according to claim 3, wherein the output of the edge detection is applied to a monostable.

5. A device according to claim 4, comprising a first counter, a random access memory, and a switch actuable to connect the output of the edge detector to the clock input of the first counter and to connect the output of the monostable to the read/write input of the memory, the first counter being connected to the address inputs of the memory.

6. A device according to claim 5, wherein the output of the second comparator is applied to a pulse separating circuit which provides line pulses on a first output and synchronising pulses on a second output, the first output being connected to the clock input of a second counter, the clock input of a third counter via a phase locked loop circuit, and the reset input of the third counter via a monostable, and the second output being connected to the reset input of the second counter via a monostable and the reset input of the first counter,

17

the outputs of the second and third counters providing an edge location data input to the memory.

7. A device according to claim 6, comprising a third comparator connected to compare the combined outputs of the second and third counter with the output of the memory.

8. A device according to claim 7, comprising a flip flop arranged to be clocked by the equality output from the third comparator and to be reset by field synchronising pulses from the second output of the pulse separating circuit.

9. A device for enhancing the contrast in television pictures substantially as hereinbefore described with reference to the accompanying drawing.

WHEATLEY & MACKENZIE
Scottish Life House
Bridge Street
Manchester, M3 3DP
Agents for the Applicants

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1981. Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.