

PHASE CHANGE DEVICE

BACKGROUND

- [0001] The present invention relates to phase change devices. More specifically, the invention relates to phase change devices with multiple states.
- [0002] Some phase change devices (PCD) can operate at two states, for example at a high or higher resistive state (HRS) and at a low or lower resistive state (LRS). Other PCDs can operate at multiple states, e.g. at resistance values between the HRS and LRS. Different voltages applied to these devices can set and reset the device states.
- [0003] In some devices, a dielectric, which is normally insulating, can be made to conduct (in a low resistance state (LRS)) through one or more filaments or conduction paths formed by application of a sufficiently high voltage. Once the filament/path is formed, a voltage change can “reset” the dielectric (e.g. break the filament/path resulting in a HRS) or “set” (re-form the filament/path resulting in a LRS) the dielectric. It is also possible to form/store intermediate states between LRS and HRS by changing the configuration of filaments via electrical bias.
- [0004] PCDs, like resistive random-access memories (RRAMs), are considered as a promising technology for electronic synapse devices or memristors used in neuromorphic computing as well as for high-density and high-speed non-volatile memory applications. In neuromorphic computing applications, a resistive memory device can be used as a connection (synapse) between a pre-neuron and post-neuron, representing the connection weight in the form of device resistance. Multiple pre-neurons and post-neurons can be connected through a crossbar array of RRAMs, which naturally expresses a fully connected neural network.
- [0005] Making PCDs in the back end of the line (BEOL) can present challenges. While device circuitry is generally placed in lower levels of circuitry in the front end of the line (FEOL) processes, the BEOL typically has multiple dielectric substrate layers that can be

difficult to use when fabricating phase change devices, particularly when forming dense arrays of PCDs like large memory structures.

- [0006] There is a need for structures and methods that enable building PCDs and higher density PCD arrays, particularly in BEOL regions. Further, there is a need for multi-state PCD structures and methods of making these multi-state PCD structures.

SUMMARY

- [0007] According to some embodiments of the present invention a phase change device (PCD) has a first and second semiconductor layer. The first semiconductor layer made of a first semiconductor material and has a first semiconductor thickness, a first interface surface, and a first electrode surface. The first interface surface and first electrode surface are on opposite sides of the first semiconductor layer. The first semiconductor material can transition between a first amorphous state and a first crystalline state at one or more first conditions. The second semiconductor layer is made of a second semiconductor material and has a second semiconductor thickness, a second interface surface, and a second electrode surface. The second interface surface and second electrode surface are on opposite sides of the second semiconductor layer. The first interface surface and the second interface surface are in electrical, physical, and chemical contact with one another at an interface. The second semiconductor material can transition between a second amorphous state and a second crystalline state at one or more second conditions. A first electrode is in physical and electrical contact with the first electrode surface of the first semiconductor layer and a second electrode is in physical and electrical contact with the second electrode surface of the second semiconductor layer. The first conditions and second conditions are different. Therefore, in some embodiments, the first and second semiconductor materials can be in different amorphous and/or crystalline states.
- [0008] In some embodiments, the first semiconductor layer is divided or split into a first epitaxial crystalline layer and a first amorphous remainder layer. The first epitaxial crystalline layer has an epitaxial thickness and an epitaxial resistance and the first

amorphous remainder layer has a remainder thickness and a remainder resistance. By controlling the epitaxial thickness, the resistance across the first semiconductor, and hence the total resistance across (the electrodes of) the device are controlled to produce multiple resistance states, from a LRS to a plurality of HRSs.

[0009] Methods of making and using PCDs are disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Various embodiments of the present invention will be described below in more detail, with reference to the accompanying drawings, now briefly described. The Figures show various apparatus, structures, and related method steps of the present invention.

[0011] Figure 1 is a block diagram of an elevation of a preliminary layered structure at an initial step in an example process of making a phase changed device (PCD).

[0012] Figure 2 is a block diagram of an elevation of a preliminary layered structure after the addition of two semiconductor layers and an optional diffusion blocking layer.

[0013] Figure 3 is a block diagram of an elevation of a preliminary layered structure after a mask etching step that defines the PCD footprint.

[0014] Figure 4 is a block diagram of an elevation of a preliminary layered structure covered with a dielectric.

[0015] Figure 5 is a block diagram of an elevation of a layered structure including a top electrode that is precursor of a PCD.

[0016] Figure 6 is a block diagram of an elevation of a precursor PCD embodiment after a first and second semiconductor layer are heated and cooled to form a crystalline structure.

[0017] Figure 7 is a block diagram of an elevation of a PCD embodiment after the first semiconductor layer is reset to an amorphous structure.

- [0018] Figure 8 is a block diagram of an elevation of a PCD embodiment after the first semiconductor layer is set to one of a plurality of two-layer structures, a first semiconductor crystalline layer and a first semiconductor amorphous layer.
- [0019] Figure 9 is a block diagram of an elevation of an alternative PCD embodiment with a diffusion blocking layer.
- [0020] Figure 10A is a voltage vs time plot showing one or more reset pulses.
- [0021] Figure 10B is a voltage vs time plot showing one or more set pulses.
- [0022] Figure 11 is a flow chart of an embodiment of a process of making a PCD.
- [0023] Figure 12 is a flow chart of an embodiment of a process for operating a PCD.

DETAILED DESCRIPTION

- [0024] It is to be understood that embodiments of the present invention are not limited to the illustrative methods, apparatus, structures, systems and devices disclosed herein but instead are more broadly applicable to other alternative and broader methods, apparatus, structures, systems and devices that become evident to those skilled in the art given this disclosure.
- [0025] In addition, it is to be understood that the various layers, structures, and/or regions shown in the accompanying drawings are not drawn to scale, and that one or more layers, structures, and/or regions of a type commonly used may not be explicitly shown in a given drawing. This does not imply that the layers, structures, and/or regions not explicitly shown are omitted from the actual devices.
- [0026] In addition, certain elements may be left out of a view for the sake of clarity and/or simplicity when explanations are not necessarily focused on such omitted elements. Moreover, the same or similar reference numbers used throughout the drawings are used to denote the same or similar features, elements, or structures, and thus, a detailed

explanation of the same or similar features, elements, or structures will not be repeated for each of the drawings.

- [0027] The semiconductor devices, structures, and methods disclosed in accordance with embodiments of the present invention can be employed in applications, hardware, and/or electronic systems. Suitable hardware and systems for implementing embodiments of the invention may include, but are not limited to, personal computers, communication networks, electronic commerce systems, portable communications devices (e.g., cell and smart phones), solid-state media storage devices, expert and artificial intelligence systems, functional circuitry, neural networks, etc. Systems and hardware incorporating the semiconductor devices and structures are contemplated embodiments of the invention.
- [0028] As used herein, “height” refers to a vertical size of an element (e.g., a layer, trench, hole, opening, etc.) in the cross-sectional or elevation views measured from a bottom surface to a top surface of the element, and/or measured with respect to a surface on which the element is located.
- [0029] Conversely, a “depth” refers to a vertical size of an element (e.g., a layer, trench, hole, opening, etc.) in the cross-sectional or elevation views measured from a top surface to a bottom surface of the element. Terms such as “thick”, “thickness”, “thin” or derivatives thereof may be used in place of “height” where indicated.
- [0030] As used herein, “lateral,” “lateral side,” “side,” and “lateral surface” refer to a side surface of an element (e.g., a layer, opening, etc.), such as a left or right-side surface in the drawings.
- [0031] As used herein, “width” or “length” refers to a size of an element (e.g., a layer, trench, hole, opening, etc.) in the drawings measured from a side surface to an opposite surface of the element. Terms such as “thick”, “thickness”, “thin” or derivatives thereof may be used in place of “width” or “length” where indicated.
- [0032] As used herein, terms such as “upper”, “lower”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom”, and derivatives thereof shall relate to the disclosed structures and

methods, as oriented in the drawing figures. For example, as used herein, “vertical” refers to a direction perpendicular to the top surface of the substrate in the elevation views, and “horizontal” refers to a direction parallel to the top surface of the substrate in the elevation views.

[0033] As used herein, unless otherwise specified, terms such as “on”, “overlying”, “atop”, “on top”, “positioned on” or “positioned atop” mean that a first element is present on a second element, wherein intervening elements may be present between the first element and the second element. As used herein, unless otherwise specified, the term “directly” used in connection with the terms “on”, “overlying”, “atop”, “on top”, “positioned on” or “positioned atop,” “disposed on,” or the terms “in contact” or “direct contact” means that a first element and a second element are connected without any intervening elements, such as, for example, intermediary conducting, insulating or semiconductor layers, present between the first element and the second element.

[0034] It is understood that these terms might be affected by the orientation of the device described. For example, while the meaning of these descriptions might change if the device was rotated upside down, the descriptions remain valid because they describe relative relationships between features of the invention.

[0035] Embodiments of phase change device (PCD) structures and processes of making and operating PCDs are disclosed.

[0036] Non-limiting examples of the PCD structures include a first semiconductor layer and a second semiconductor layers sandwiched between a top and a bottom electrode. The first semiconductor layer and a second semiconductor layer have an interface where each of one of the surfaces (an interface surface) of the first and second semiconductor is in physical contact with the other interface surface. In some embodiments, there is a thin diffusion blocking layer between the first and second interface surface. Each of the first and second semiconductor layers has an electrode surface that is a side of the semiconductor layer opposite the interface surface of the respective semiconductor layer. A first electrode surface on the first semiconductor layer is in physical and electrical

contact with the bottom or first electrode and a second electrode surface on the second semiconductor layer is in physical and electrical contact with the top or second electrode.

- [0037] The materials making the first and second semiconductor layers have different and distinguishable thermal properties in that each of the semiconductors change from an amorphous structure to a crystalline structure under different conditions, e.g. thermal changes like temperature.
- [0038] A thermal heating and cooling step, e.g. an anneal, is performed to put both the first and second semiconductor layers in a crystalline state.
- [0039] A "set" step enables an epitaxial crystalline growth or change of the first crystalline layer to form a first epitaxial crystalline layer within the (split) first semiconductor layer, starting at the interface, and penetrating the first semiconductor layer. Accordingly, the first semiconductor layer is divided or split into a first epitaxial crystalline layer and a first amorphous remainder layer. The first epitaxial crystalline layer has an epitaxial thickness and an epitaxial resistance and the first amorphous remainder layer has a remainder thickness and a remainder resistance.
- [0040] By varying how the set step is performed, e.g. by changing characteristics of a set pulse, the epitaxial thickness and remainder thickness will change. Accordingly, the epitaxial resistance and remainder resistance can be varied and different amounts of resistance (total resistance) across the structure, e.g. different (resistive) states of the structure, can be pre-determined, controlled, and enabled.
- [0041] Refer now to the Figures.
- [0042] Figure 1 is a block diagram of an elevation of a preliminary layered structure 100 at an initial step in an example process of making a phase changed device (PCD).
- [0043] The structure 100 has a substrate 105. A dielectric layer 110 is disposed upon the substrate 105. In some embodiments, e.g. at the back end of the line (BEOL), the substrate 105 might be eliminated. A bottom electrode 115 is disposed on the dielectric layer 110.

- [0044] The substrate 105 can be made from a single element (e.g., silicon or germanium); primarily a single element (e.g., with doping), for example silicon; or a compound semiconductor, for example, gallium arsenide (GaAs), or a semiconductor alloy, for example silicon-germanium (SiGe). In some embodiments, the substrate 105 includes one or more semiconductor materials including, but not limited to, silicon (Si), SiGe, Si:C (carbon doped silicon), germanium (Ge), carbon doped silicon-germanium (SiGe:C), Si alloys, Ge alloys, III-V materials (e.g., GaAs, indium gallium arsenide (InGaAs), indium arsenide (InAs), indium phosphide (InP), aluminum arsenide (AlAs), etc.), II-V materials (e.g., cadmium selenide (CdSe), cadmium sulfide (CdS), or any combination thereof) or other like semiconductors. In addition, multiple layers of the semiconductor materials can be used as the semiconductor material of the substrate 105. In some embodiments, the substrate 105 includes both semiconductor materials and dielectric materials. In some silicon on insulator (SOI) implementations, a buried oxide layer, BOX, (e.g., SiO₂) is buried in the substrate 105.
- [0045] In some embodiments, the dielectric layer 110 is made of low-k dielectric. The term “low-k dielectric” generally refers to an insulating material having a dielectric constant less than silicon dioxide, e.g., less than 3.9. As a non-limiting example, the dielectric layer 110 is made of materials including: dielectric oxides (e.g. silicon oxide, SiO_x); dielectric nitrides (e.g., silicon nitride, SiN; siliconborocarbonitride, SiBCN; siliconcarbonitride, SiCN; and siliconboronitride SiBN); dielectric oxynitrides (e.g., silicon oxycarbonitride, SiOCN, and silicon oxynitride, SiON); silicon carbide (SiC); silicon oxycarbide (SiCO); or any combination thereof or the like.
- [0046] The dielectric layer 110 can be deposited by known deposition techniques including: atomic layer deposition (ALD), chemical vapor deposition (CVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), Radio Frequency Chemical Vapor Deposition (RFCVD,) Physical Vapor Deposition (PVD), Pulsed Laser Deposition (PLD), and/or Liquid Source Misted Chemical Deposition (LSMCD).
- [0047] In some embodiments, the dielectric layer 110 has a dielectric layer thickness 111 between 50 nanometers (nm) and 100 nm. Other thicknesses 111 are envisioned.

- [0048] The first or bottom electrode 115 is made of a conductive material, e.g. a metal. Non-limiting examples of metals include: copper (Cu), tungsten (W), aluminum (Al), nickel (Ni), thallium nitride (Tl₃N), and titanium nitride (TiN). In some embodiments, the first/bottom electrode 115 is made of Al.
- [0049] The first/bottom electrode 115 can be deposited by ALD, CVD, PECVD, RFCVD, PVD, PLD, LSMCD, and/or sputtering.
- [0050] In some embodiments, the first electrode 115 thickness 116 is between 50 nanometers (nm) and 100 nm. Other thicknesses 116 are envisioned.
- [0051] Figure 2 is a block diagram of an elevation of a preliminary layered structure 200 after the addition of two semiconductor layers (250, 225) and an optional diffusion blocking layer 285.
- [0052] A first semiconductor layer 250 is made of a first semiconductor material capable of being in an amorphous form (first amorphous form) and a crystalline form (first crystalline form). A second semiconductor layer 225 is made of a second semiconductor material capable of being in an amorphous form (second amorphous form) and a crystalline form (second crystalline form). The amorphous forms can transition to crystalline forms (and visa versa) under various physical conditions. The first semiconductor material has properties that cause the first semiconductor material to transition from amorphous form to crystalline form under conditions (e.g. application of temperature and/or voltage) that are different than the conditions under which the second semiconductor makes these transitions.
- [0053] In some embodiments, the first semiconductor layer 250 material is germanium (Ge) and the second semiconductor layer 225 material is silicon (Si). Other materials are envisioned.
- [0054] The first semiconductor layer 250 has a first semiconductor layer 250 thickness 251 between 20 nm and 50 nm. The second semiconductor layer 225 has a second semiconductor layer 225 thickness 226 between 20 nm and 50 nm, as well.

- [0055] The first semiconductor layer 250 has a first interface surface 257 and a first electrode surface 258. The first interface surface 257 and the first electrode surface 258 are opposite one another, i.e. on opposite sides of the first semiconductor layer 250.
- [0056] The second semiconductor layer 225 has a second interface surface 227 and a second electrode surface 228. The second interface surface 227 and the second electrode surface 228 are opposite one another, i.e. on opposite sides of the first semiconductor layer 225.
- [0057] The first electrode surface is in physical and electrical contact with the first/bottom electrode 115. In some embodiments, the first interface surface 257 is in physical, chemical, and electrical contact with the second interface surface 227. In alternative embodiments, there is an optional diffusion blocking layer (DBL) 285 “sandwiched” between the first 257 and second 227 interface surfaces. The second electrode surface 228 is in physical and electrical contact with the second/top electrode 515, shown below, e.g. in Figure 5.
- [0058] The DBL 285 prevents diffusion of the first semiconductor layer 250 material (e.g. Ge) into the second semiconductor layer 225 material, (e.g. Si). The DBL can be made of Titanium Nitride (TiN) or carbon (C). Other known barrier or diffusion prevention materials can be used.
- [0059] The DBL 285 is a thin layer having a thickness 286 between 1 nm and 10 nm.
- [0060] The first 250 and second 225 semiconductor layers and the DBL 285 can be deposited by ALD, CVD, PECVD, RFCVD, PVD, PLD, and/or LSMCD. The order of deposition is inconsequential. However, if the optional DBL layer 285 is disposed, the DBL layer 285 will be between the first 257 and second 227 interface surfaces. If the order of depositing the semiconductor layers (250, 225) is reversed, the second electrode surface 228 is in physical and electrical contact with the first/bottom electrode 115 and the first electrode surface 258 is in physical and electrical contact with the second/top electrode 515. However, in either case, the first semiconductor layer 250 will be the semiconductor layer with the epitaxial growth, as described below, without loss of generality.

- [0061] Figure 3 is a block diagram of an elevation of a preliminary layered structure 300 after a known mask etching step, e.g. a directional reactive ion etch (RIE), that defines the PCD footprint. A mask protects parts of the semiconductor layers (225, 250) while volumes of the semiconductor layers (225, 250) are removed 310 around (left and right - and front and back, not shown) the remaining semiconductor layers (350, 325). One or more known chemistries suitable to remove the unmasked first 250 and second 225 semiconductor layer 250 can be used. In some embodiments, the etching will stop at a barrier layer, e.g. the first/bottom electrode 115.
- [0062] In this structure 300 and following structures, the DBL 285 may or may not be included in the structure but the DBL 285 is not shown for reasons of clarity. This masked etching defines the size and/or area the PCD uses on the surface of the first/bottom electrode 115 surface, i.e. the PCD footprint.
- [0063] Figure 4 is a block diagram of an elevation of a preliminary layered structure 400 covered with a dielectric 410.
- [0064] In some embodiments, the dielectric 410 can be the same type as in the dielectric layer 110 and/or disposed by the same methods. In some embodiments, the dielectric 410 can be an interlayer dielectric (ILD). The ILD 410 may be formed from, for example, a low-k dielectric material (with $k < 4.0$), including but not limited to, silicon oxide, spin-on-glass, a flowable oxide, a high-density plasma oxide, borophosphosilicate glass (BPSG), or any combination thereof. The ILD 410 is deposited by a deposition process, including, but not limited to CVD, PVD, PECVD, ALD, evaporation, chemical solution deposition, or like processes.
- [0065] Figure 5 is a block diagram of an elevation of a layered structure 500 including a second/top electrode 515. The structure 500 is precursor of a PCD in that the structure 500 is complete but the semiconductor layers (325, 350) need to have their chemical structure transformed to operate efficiently as a PCD, as described below.
- [0066] The second/top electrode 515 is formed by performing a masked etch, e.g. a directional RIE, through the ILD/dielectric layer 410 above the second semiconductor layer 325. In

some embodiments, the etch stops at the second electrode surface 228. Using materials and methods like those used to deposit the first electrode layer 115, the second/top electrode 515 is deposited to be in physical and electrical contact with the second electrode surface 228.

- [0067] Figure 6 is a block diagram of an elevation of a precursor PCD embodiment 600 after a first 350 and second semiconductor layer 325 are heated and cooled to form crystalline structures (650, 625).
- [0068] A physical process is performed so that both the first 350 and second 325 semiconductor layers experience one or more changed physical conditions that transform the first semiconductor structure 350 into a first crystalline state 650 and transform the second semiconductor structure 325 into a second crystalline state 625.
- [0069] In some embodiments, the changed physical condition is a thermal anneal. In other words, both the semiconductor layers (350, 325) are heated above a temperature at which they melt and then cooled over time so both the first 650 and second 625 crystalline semiconductor layers are formed. The time and temperature levels that crystallize both the first 650 and second 625 layers crystalline depend on the type of the material in the layer and the volume of material within the layer. While actual time and temperature values need to be determined for the specific situation, as a non-limiting example, the temperature is raised to a temperature between 900 degrees Celsius (C) and 1000 C locally within the device and allowed to cool to room temperature over a period between 1 micro second and 10 micro second seconds.
- [0070] In a non-limiting example, amorphous Ge (α -Ge) in the first semiconductor layer 350 is changed to crystalline Ge (c-Ge) 650 and the amorphous Si (α -Si) in the second semiconductor layer 325 is changed to crystalline Si (c-Si) 625 by the anneal step.
- [0071] Figure 7 is a block diagram of an elevation of a PCD embodiment 700 after the first crystalline semiconductor layer 650 is reset to an amorphous structure 750.
- [0072] The first crystalline structure semiconductor layer 650 is “reset” to the amorphous structure 750 without changing the structure of the second crystalline structure

semiconductor layer 625. This is due to the fact that the first (350, 650) and second (325, 625) semiconductor layers each have properties that made their transitions from amorphous to crystalline (and back again) at one or more different and distinguishable physical conditions. Therefore, the transition from amorphous to crystalline (and back again) can be made in the first (350, 650) semiconductor layer structure without effecting the second (325, 625) semiconductor layer structure.

[0073] In a non-limiting example, Ge makes the transition from amorphous to crystalline (and back again) at a lower temperature than Si. By applying one or more electrical/voltage pulses across the first/bottom 115 and second/top 515 electrodes, current flows through the first (350, 650) and second (325, 625) semiconductor layers causing them to heat up. The pulses are designed to heat the Ge above the Ge transition point (temperature) but below the Si transition point. Accordingly, the first crystalline semiconductor layer 650 (e.g. c-Ge) melts but the second crystalline semiconductor layer 625 does not melt. There is a quick cooling period that is too fast to re-form the first amorphous semiconductor layer 750 into a crystalline state. The second crystalline 625 semiconductor layer 625 (e.g. c-Si) does not change from the crystalline state 625, due to the temperature/voltage change.

[0074] The structure 700 is now “reset” having the first semiconductor layer 350 in an amorphous state 750 at a higher resistance. Accordingly, the entire resistance of the structure 700 is higher because of the increased resistance of the first amorphous semiconductor layer 750. The structure 700 is reset in a HRS due to the amorphous structure of the first semiconductor layer 350. “Setting”, described below, the first semiconductor layer 350 back to the crystalline structure decreases the resistance across the first semiconductor layer (350, 650) and puts the structure 700 in multiple HRS until reaching a LRS – a PCD with two or more states, a LRS and a multiple HRS.

[0075] Material type in the first 350 and second 325 semiconductor layers, the volumes of the layers, and other factors are used to design the timing, shape, and magnitude of the voltage pulses. Examples of pulse timing, shape, and magnitude of the voltage pulses

used to “reset” are given below in Figure 10A. In some embodiments, in the reset state, the entire volume of the first semiconductor layer 350 is in the amorphous state.

- [0076] Figure 8 is a block diagram of an elevation of a PCD embodiment 800 after the first amorphous semiconductor layer 850 is “set” to one of a plurality of two-layer structures (850A, 850B), a first semiconductor crystalline layer 850A and a first semiconductor amorphous layer 850B.
- [0077] In one embodiment, a set pulse (see Figure 10B) causes the first amorphous semiconductor layer (e.g. after a reset pulse resets the first semiconductor layer totally in the amorphous state 750) to change into a split first semiconductor layer 850, split into two layers: 1. a first epitaxial crystalline layer 850A that has an epitaxial thickness 865 and an epitaxial resistance and 2. a first amorphous remainder layer 850B that has a remainder thickness 860 and a remainder resistance. The remainder layer 850B is what remains of the amorphous layer 750 of the first semiconductor amorphous layer 750 after a set pulse.
- [0078] The shape, durations, timing, and magnitudes of the set pulse determine how large, e.g. the thickness 865 of the first epitaxial crystalline layer 850A and the thickness 860 of the first amorphous remainder layer 850B. Accordingly, the epitaxial resistance and remainder resistance can be controlled by the design of the set pulse which controls the thicknesses (825, 860) of the respective epitaxial crystalline layer 850A and remainder layer 850B. Therefore, the resistance of the split first semiconductor layer 850 and the total resistance of the entire device 800 (measured across the first and second electrodes 115/515) in the set state, i.e. the amount of resistance in the HRSs, is controlled by the design of the set pulse.
- [0079] Other factors that affect the amount of resistance of the device 800 in one of the multiple HRS and how the set pulse is designed include the first 250 and second 225 semiconductor layer materials and thicknesses (251, 226) and the type of material and thickness 286 of the DBL layer 285, if any.

- [0080] As a result, with other external physical conditions of the first 250 and second 225 semiconductor layer held constant, multiple high resistance states, e.g. values of total resistance of the device 800 in the set state can be created by varying the shape, durations, timing, and magnitudes of the set pulse. Therefore, structure 800 can be a PCD with multiple (resistive) set states by varying the set pulse.
- [0081] By varying how the set step is performed, e.g. by changing characteristics of a set pulse, the epitaxial thickness and remainder thickness will change. Accordingly, the epitaxial resistance and remainder resistance can be varied and different amounts of resistance across the structure, e.g. different states of the structure, can be pre-determined, controlled, and enabled.
- [0082] The design of the set pulse determines how the first epitaxial crystalline layer 850A is formed.
- [0083] The term “epitaxially growth” means the growth of a semiconductor material on a contact surface of a semiconductor material, in which the semiconductor material being grown has the same crystalline characteristics as the semiconductor material of the deposition surface. Material parameters can be created so that the atoms at the surface 875 of the growing layer 850A have sufficient energy to move around on the surface 875 and orient themselves to the crystal arrangement of the atoms at where the epitaxial growth is continuing.
- [0084] For example, if the set pulse is designed to heat and melt the first amorphous semiconductor layer 750, the atoms in the first amorphous semiconductor layer 750 will have enough energy to move around. If in addition, the set pulse allows the first amorphous semiconductor layer 750 to cool slowly, the moving atoms (e.g. of Ge) will move into the crystal orientation of a crystal surface in which they are in contact.
- [0085] Where there is a DBL 985, the DBL 985 can act as a template for the Ge crystallization.
- [0086] To continue with this non-limiting example, when the set pulse melts the first amorphous semiconductor layer 750 material (Ge), the material (Si) in the second semiconductor layer 625 remains in a crystalline structure. As the atoms in the first amorphous

semiconductor layer 750 slowly cool, they arrange themselves in the crystalline order of the second semiconductor layer 625 starting at the interface 825. As the layer 850 continues to slowly cool, more of the atoms in the first amorphous semiconductor layer 750 arrange in the crystalline order thus growing the thickness 865 of the growing first epitaxial crystalline layer 850A and moving the boundary surface 875 deeper into the first amorphous semiconductor layer 750. As the thickness 865 of the first epitaxial crystalline layer 850A increases, the thickness 860 of the remainder layer 850B decreases.

- [0087] By changing the thickness 865 of the first epitaxial crystalline layer 850A and the thickness 860 of the remainder layer 850B, the resistances of these layers change and therefore, the entire resistance of the device 800 changes by controlling the set pulse.
- [0088] In some embodiments, by causing the set pulse(s) to slowly decrease in value over time, e.g. by reducing the rate of change of cooling and/or increasing the cooling time of the split first semiconductor layer 850, the thickness 865 of the first epitaxial crystalline layer 850A will increase and the thickness 860 of the remainder layer 850B will decrease.
- [0089] Figure 9 is a block diagram of an elevation of an alternative PCD embodiment 900 with a diffusion blocking layer (DBL) 985. The blocking layer 985 is formed by depositing the optional layer 285 shown in Figure 2 and continuing with process steps performed in the case when no DBL 285 was deposited.
- [0090] Figure 10A is a voltage 1030 vs time 1035 plot 1000 showing one or more reset pulses, typically 1025. The reset pulses 1025 have a duration 1010 and magnitude 1020 high enough to melt the material in the first semiconductor layer 250 (e.g. Ge) but not in the second semiconductor layer 225 (e.g. Si). However, the duration 1010 is short enough and, in particular, the fall time 1026 is fast enough so that the first 250 semiconductor layer material has no time to crystallize. Therefore, the first 250 semiconductor layer material remains in/returns to an amorphous structure/state 750 when the device 800/900

is reset.

- [0091] Figure 10B is a voltage 1030 vs time 1035 plot 1050 showing one or more set pulses, typically 1070. The set pulses have a magnitude 1055 and a duration 1060 with a gradual fall time rate 1065 over a set pulse fall time 1075. For example, the fall time rate 1065 is the magnitude 1055 of the pulse 1070 divided by the set pulse fall time 1075.
- [0092] As discussed, the design of magnitudes (1020, 1055), timing (1010, 1060, 1075), duration (1010, 1080), and shape of these pulses (1025, 1070) among other things depends on the types of material in and the thickness (251, 226) of the first 350 and second 325 semiconductor layers.
- [0093] However, in some embodiments, the reset pulse 1025 has a reset pulse magnitude 1020 of between 7 and 10 volts, e.g. 8 volts; a reset pulse rise time 1024 between 2.0 and 3.0 nanoseconds (ns), e.g. 2.5 ns; and a reset pulse fall time 1026 between 2.0 and 3.0 nanoseconds (ns), e.g. 2.5 ns. The reset pulse shape can be rectangular or other shapes. However, the reset pulse fall time 1026 must be fast enough so the material does not crystallize. The reset pulse 1025 magnitude 1020 has to be low enough so crystalline structure of the material of the second semiconductor layer 625 does not change.
- [0094] In some embodiments, non-limiting examples, the set pulse 1070 has a magnitude 1069 of between 4 and 6 volts, e.g. 5 volts; a set pulse rise time 1069 between 2.0 and 3.0 nanoseconds (ns), e.g. 2.5 ns; and a longer set pulse fall time 1075 between 0.8 milliseconds (ms) and 1.5 ms, e.g. 1.0 ms. Some set pulse shapes have gradual falling fall times e.g. more than 1.0 ms to give the first semiconductor crystalline layer 850A crystalline structure time to form. The duration 1080 of the set pulse 1070 is long enough to include the long fall time 1075, e.g. 1.0 ms or more.
- [0095] Figure 11 is a flow chart of an embodiment of a process of making 1100 a PCD.

- [0096] Step 1105 of the method begins with deposition the first electrode 115 on the dielectric layer 110 and/or substrate 105. Then the first 250 and second 225 semiconductor layers are deposited. In some embodiments the diffusion blocking layer 285 is deposited between the electric first 250 and second 225 semiconductor layers.
- [0097] Step 1110 deposits the second electrode 515 after doing the etching defining the PCD footprint and other lithographic steps as defined in Figures 3 to 5.
- [0098] Step 1115 crystallizes the first 250 and second 225 semiconductor layers with thermal heating and cooling step, e.g. an anneal, as described in Figure 6. Other crystallization methods are possible.
- [0099] Step 1120 makes the first semiconductor layer amorphous by changing a physical condition, e.g. with a reset voltage pulse 1025, placing the device in the reset state or LRS.
- [0100] Step 1125 splits the first semiconductor layer 850 into first semiconductor crystalline layer 850A and a first semiconductor amorphous layer 850B by changing a physical condition, e.g. with set voltage pulse 1075. This places the device 800 in one of a plurality of resistive states (as measured by the total resistance across the first 115 and second 515 electrodes) as selected by the design of the set voltage pulse 1075. The resistive states will have a total resistance across the device 800 with one of a plurality of values between the LRS and a HRS. In the LRS the first semiconductor crystalline layer 850A has a width or epitaxial thickness 865 that is equal to the total first semiconductor layer 250 width 251.
- [0101] Figure 12 is a flow chart of an embodiment of a process for operating 1200 a PCD.
- [0102] The process 1200 starts with step 1205 that resets the first semiconductor layer 850 to an amorphous state where the all the first semiconductor 850 material is in the amorphous state 750. In some embodiments, this step is performed with a reset pulse 1025.

- [0103] In step 1210 the device, e.g. 800, is set to split the first semiconductor layer 850 into the first semiconductor crystalline layer 850A and the remainder layer 850B.
- [0104] In step 1215, the total resistance across the device, e.g. 800, selected by the set pulse as described in Figure 10B. The total resistance is the resistance measured across the first 115 and second 515 electrodes. The total resistance is greatly influenced by the resistance of the first semiconductor layer 850 which in turn is influenced by the width or epitaxial thickness 865 of the first semiconductor crystalline layer 850A. The greater the epitaxial thickness 865, the greater the volume of the first semiconductor layer 850 material is in the crystalline state, a state with lower resistance. Therefore, by controlling the epitaxial thickness 865, the total resistance can be change to be one of a plurality of values between the LRS and HRS or between a structure where the first semiconductor layer 850 material is entirely amorphous or entirely crystalline, respectively. Design of the set pulse determines how much of the first semiconductor layer 850 material epitaxially grows, increases the epitaxial thickness 865, and decreases the total resistance.
- [0105] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. For example, the semiconductor devices, structures, and methods disclosed in accordance with embodiments of the present invention can be employed in applications, hardware, and/or electronic systems. Suitable hardware and systems for implementing embodiments of the invention may include, but are not limited to, personal computers, communication networks, electronic commerce systems, portable communications devices (e.g., cell and smart phones), solid-state media storage devices, expert and artificial intelligence systems, functional circuitry, etc. Systems and hardware incorporating the semiconductor devices are contemplated embodiments of the invention.
- [0106] The terminology used herein was chosen to explain the principles of the embodiments and the practical application or technical improvement over technologies found in the

marketplace or to otherwise enable others of ordinary skill in the art to understand the embodiments disclosed herein. Devices, components, elements, features, apparatus, systems, structures, techniques, and methods described with different terminology that perform substantially the same function, work in the substantial the same way, have substantially the same use, and/or perform the similar steps are contemplated as embodiments of this invention.