# System for Generic Static Multiple Issue Integrated Circuit Design with Static Auto-Parallelized Code, and Method Thereof

## *Field of the Invention*

This invention relates generally to the design and manufacture of integrated circuitry (IC) and more particularly to a system and a method of maximizing manufacturing yield as well as chip performance and processing speed by using IC layout optimization driven by integrated circuit fabrication process simulation. Furthermore, the current invention generally relates to the design and manufacture of integrated circuitry (IC) for multi-processor systems, in particular multi-core systems and parallel computing systems allowing multiprocessing. In a multi-core IC, two or more processors or cores work together to execute multiple program codes and/or processor instruction sets simultaneously, wherein in the IC for multi-processor systems or parallel-computing systems, the IC comprising a number of central processing units integrated on the IC and linked together to enable said multiprocessing or parallel processing to take place. Further, it relates to a system and a method of maximizing manufacturing yield, IC processing performance and processing speed in respect to a specific, parallelized code, for execution in the described, specifically architectured and optimized multi-processor architecture systems. More particular, it further relates to mutual optimization of the parallelization of code and optimization of a respective IC design. In the technical field of multiprocessor systems, important characteristics and classifications arise inter alia, from way, how processor memory access is handled and whether system processors are of a single type or various ones in the system architecture.

## *Background of the Invention*

In the last years, a fundamental change in computer architecture has been observed that will impact every facet of data processing and operation of every electronic device from cell phone to supercomputer, since it introduces parallelism of unprecedented scale, which confronts traditional technical approaches of code