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(54) Title: DIGITAL DESYNCHRONIZER

(57) Abstract

A digital desynchronizer device (10) includes an elastic store unit (12) that receives data in an asynchronous manner and synchronously transmits the data in response to a synchronization clock generated by a clock generator (14). The clock generator (14) operates off of a reference oscillator unit (16). The clock generator (14) generates the synchronization clock signal in response to pointer adjustments identified by a pointer movement unit (18). The clock generator (14) also generates the synchronization clock signal in response to mapping jitter identified by a mapping unit (20). The pointer movement unit (18) and the mapping unit (20) identify pointer adjustments and mapping jitter, respectively, independent of each other. The clock generator (14) adjusts a width of a specific pulse bit in response to pointer adjustments identified by the pointer movement unit (18). Clock generator (14) also adjusts a width of a specific bit position, separate from the pulse bit position used for pointer adjustments, in response to mapping jitter identified by the mapping unit (20).

