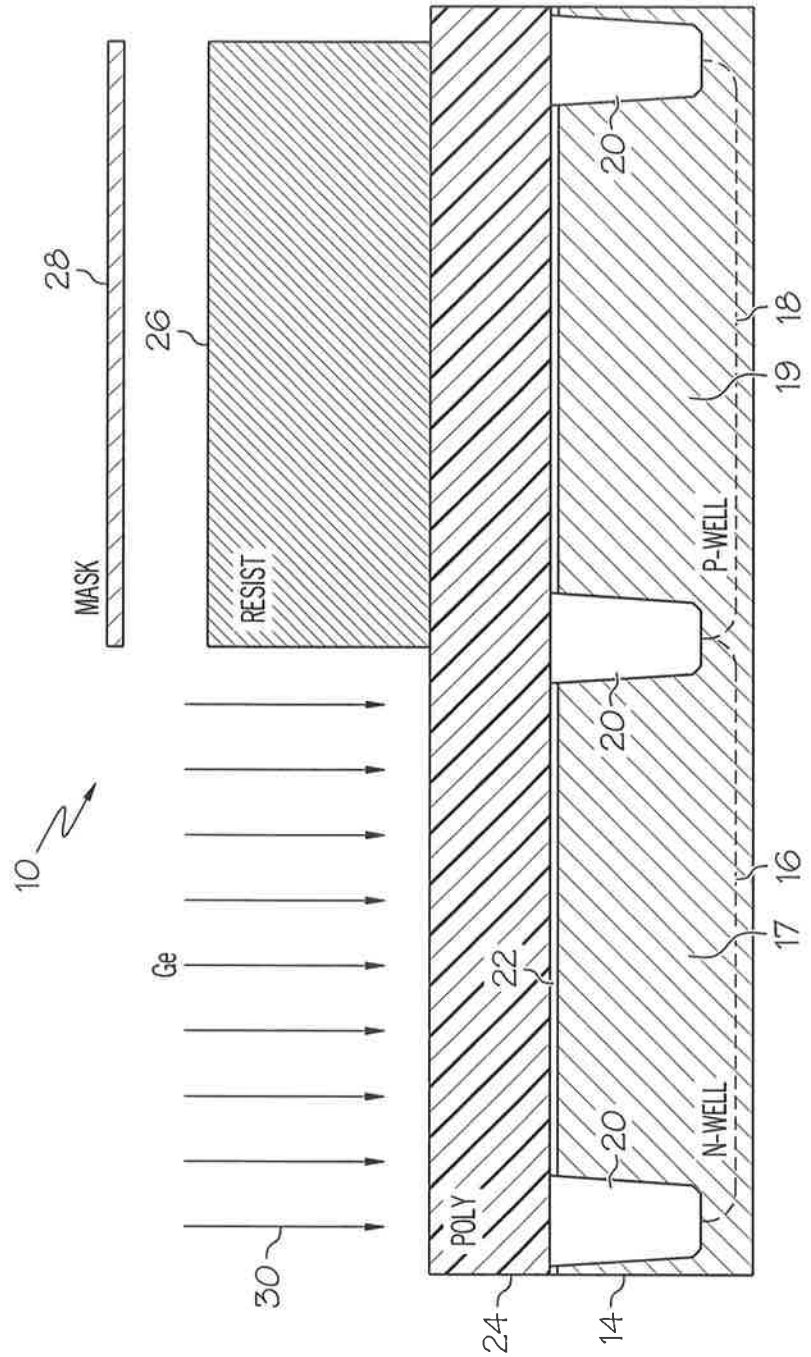

10
28
MASK
26
RESIST
Ge
30
POLY
22
24
14
N-WELL
P-WELL
20
16
17
18
19

FIG. 1A

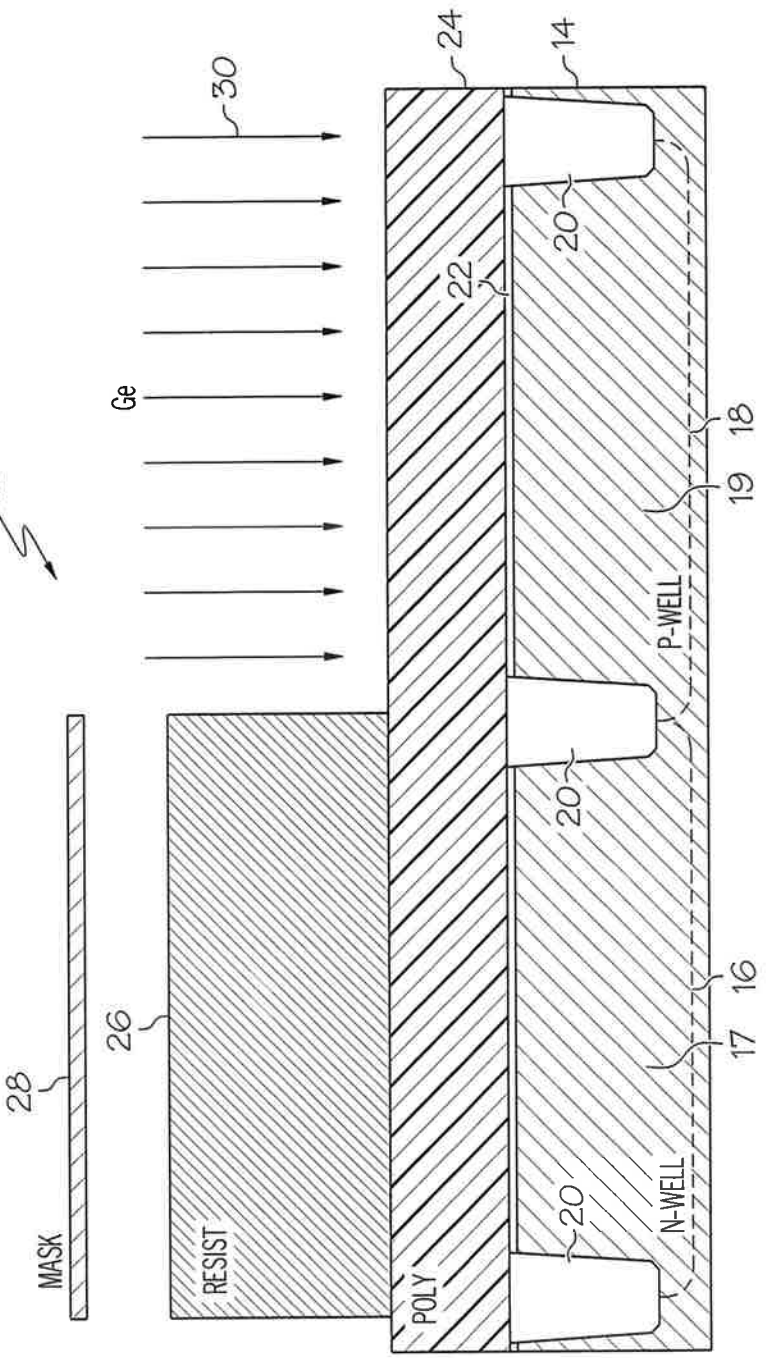

12
Ge
30
24
14
22
20
18
19
P-WELL
20
16
17
N-WELL
20
28
MASK
26
RESIST
POLY

FIG. 1B

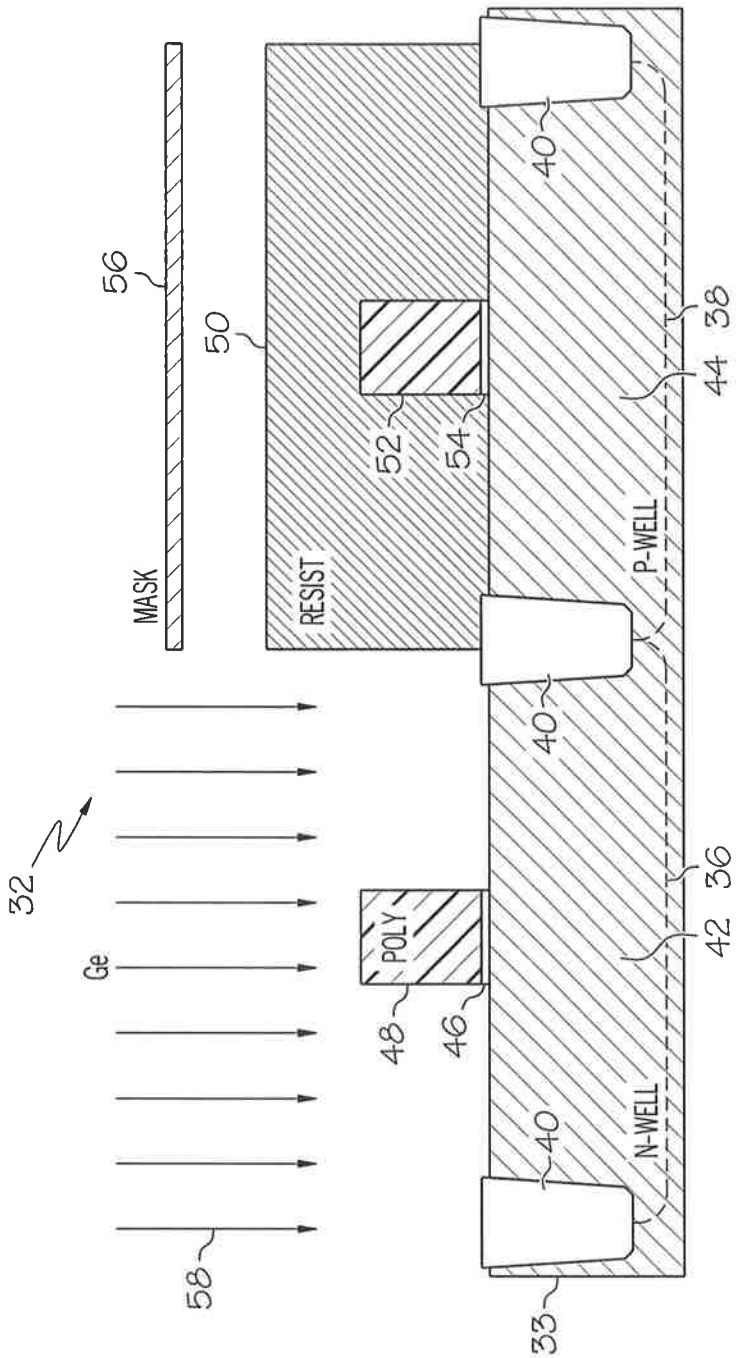

56
50
MASK
RESIST
52
54
40
38
44
P-WELL
40
36
42
32
Ge
POLY
48
46
40
N-WELL
58
33

FIG. 2A

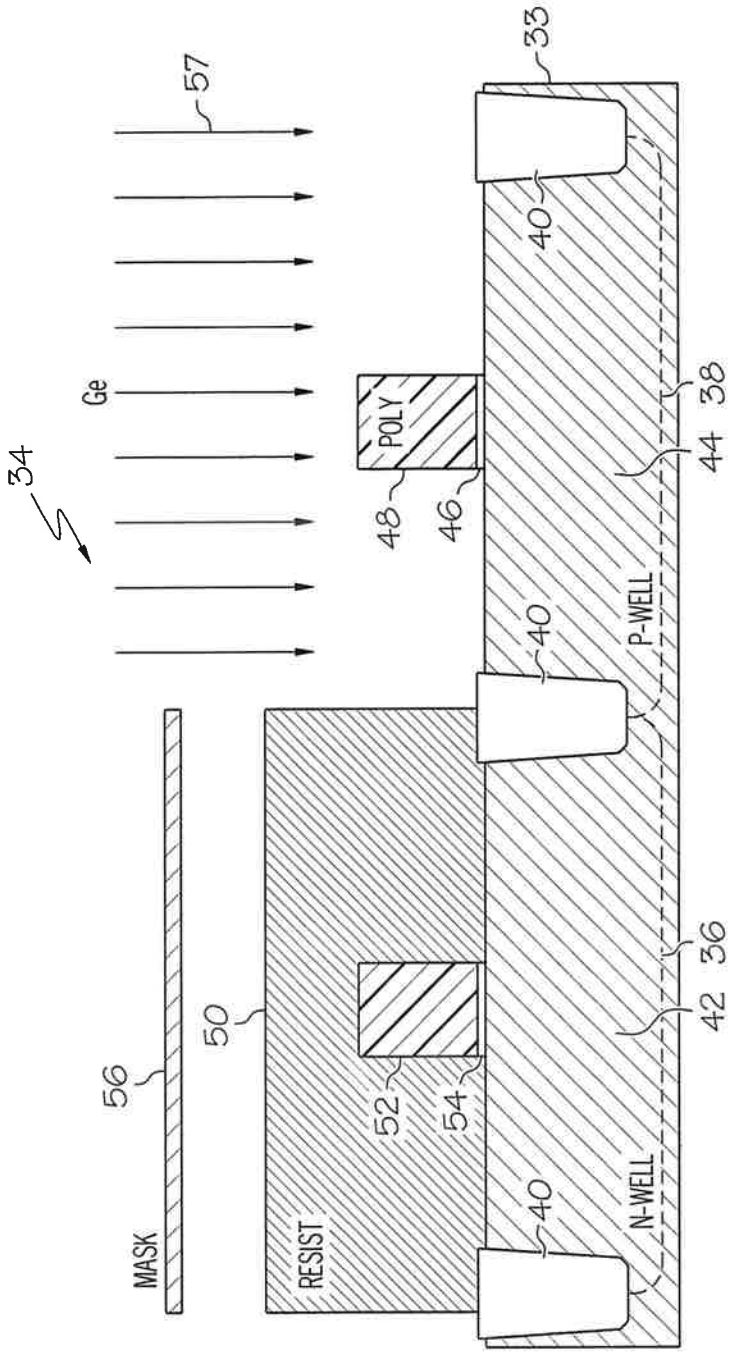

34
Ge
57
33
40
POLY
48
46
38
44
P-WELL
40
36
42
N-WELL
40
50
52
54
56
MASK
RESIST

FIG. 2B

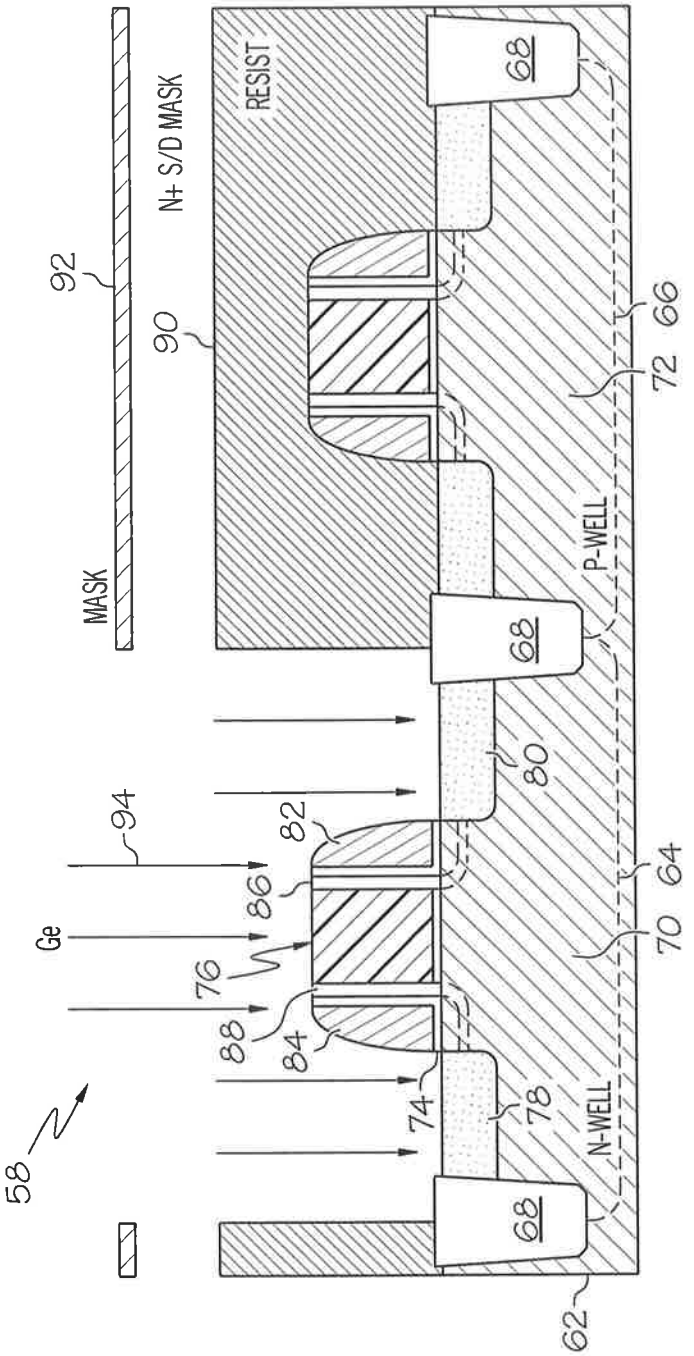

MASK
N+ S/D MASK
RESIST
92
90
94
Ge
58
68
66
72
P-WELL
80
82
64
86
70
76
88
84
74
78
N-WELL
62

FIG. 3A

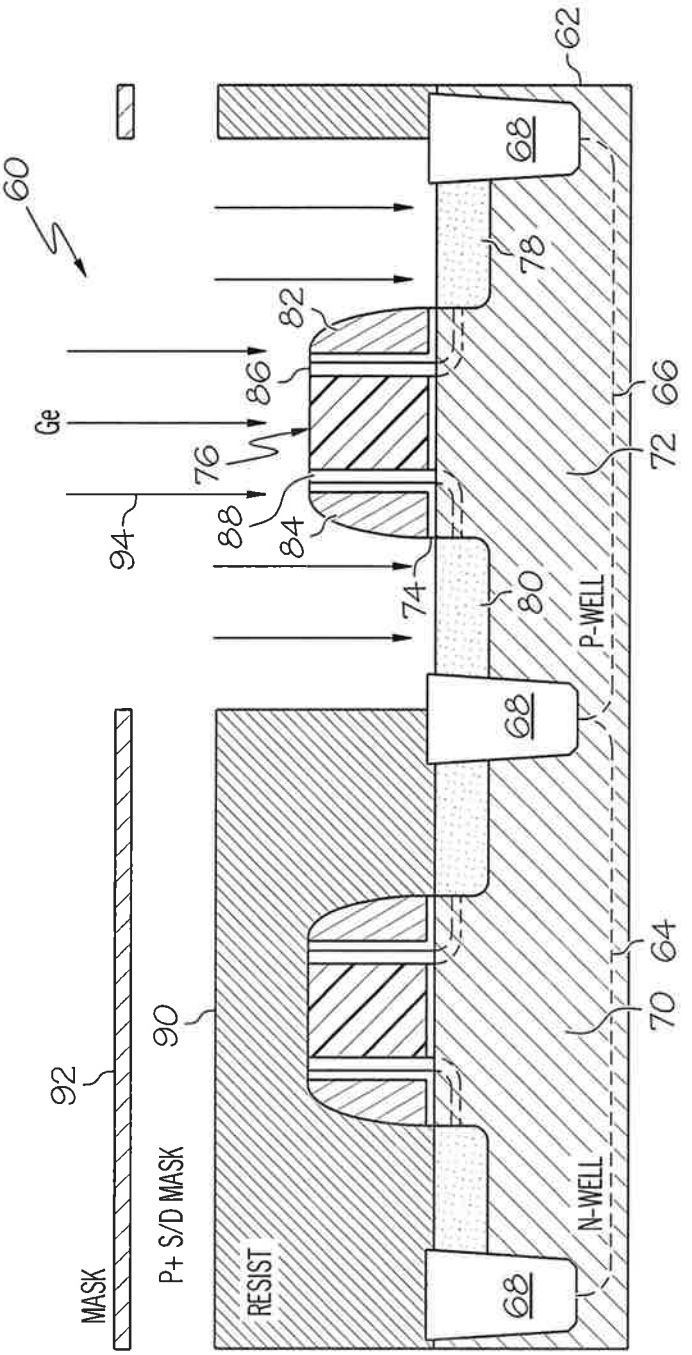

60
62
68
78
82
86
Ge
76
66
72
94
88
84
74
80
P-WELL
68
64
70
90
92
N-WELL
68
RESIST
P+ S/D MASK
MASK

FIG. 3B

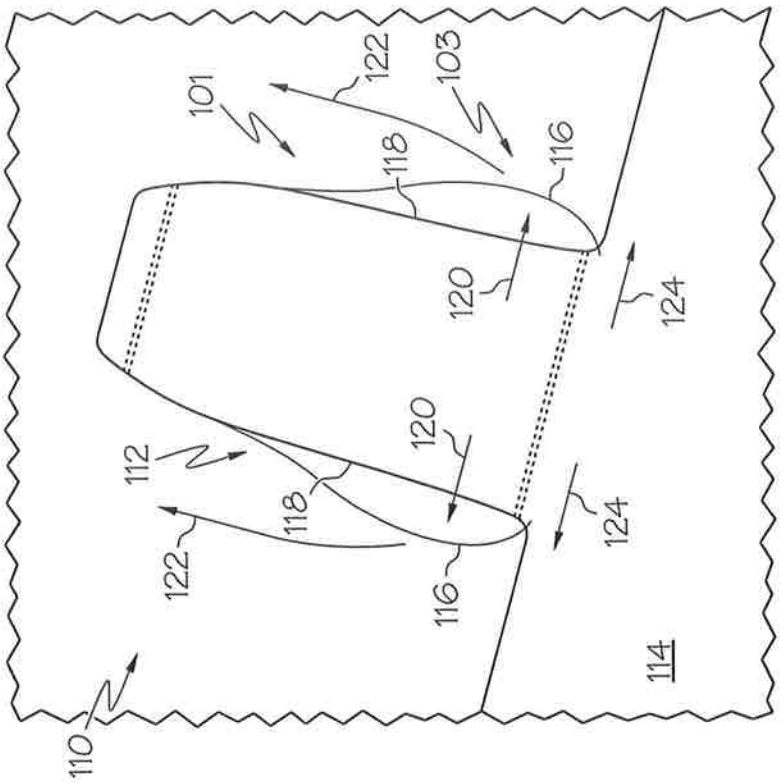

110
112
122
118
116
120
124
114
101
103
122
118
116
120
124

FIG. 5

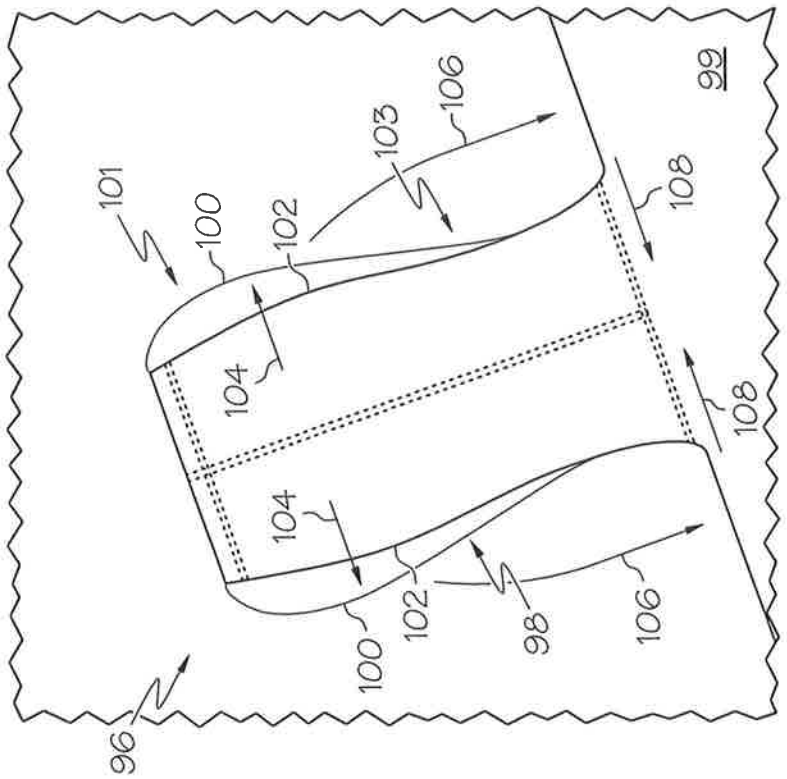

96
101
100
102
104
103
106
108
99
98

FIG. 4

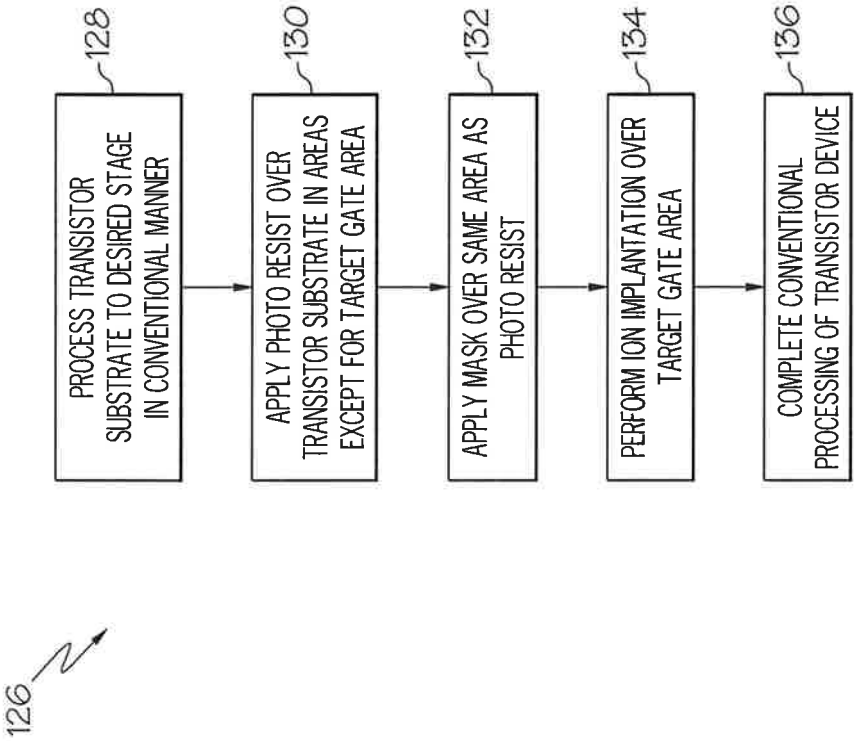

126
128
PROCESS TRANSISTOR SUBSTRATE TO DESIRED STAGE IN CONVENTIONAL MANNER
130
APPLY PHOTO RESIST OVER TRANSISTOR SUBSTRATE IN AREAS EXCEPT FOR TARGET GATE AREA
132
APPLY MASK OVER SAME AREA AS PHOTO RESIST
134
PERFORM ION IMPLANTATION OVER TARGET GATE AREA
136
COMPLETE CONVENTIONAL PROCESSING OF TRANSISTOR DEVICE

FIG. 6