Improve Transistor Mobility by Adjusting Stress in Shallow Trench Isolation

TECHNICAL FIELD

[0001] This invention relates generally to semiconductor integrated circuits, and more specifically to the improvement of CMOS transistors by applying stress.

BACKGROUND

[0002] The scaling of VLSI circuits is a constant effort. With circuits becoming smaller and faster, device driving current improvement becomes more important. Device current is closely related to gate length, gate capacitance, and carrier mobility. Shortening poly-gate length, increasing gate capacitance and increasing carrier mobility can improve the device current performance. Gate length reduction is an on-going effort in order to shrink circuit size. Increasing gate capacitance has also been achieved by efforts such as reducing the gate dielectric thickness, increasing the gate dielectric constant, and the like. In order to further improve device current, enhancing carrier mobility has also been explored.

[0003] Among efforts made to enhance carrier mobility, forming a stressed silicon channel is a known practice. Stress can enhance bulk electron and hole mobility. The performance of a CMOS transistor can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length, without adding complexity to circuit fabrication or design.

[0004] When silicon is placed under stress, the electron mobility is dramatically increased. Stress can also be applied to the channel region by forming a stress-inducing contact etch stop layer (CESL) over the transistor. When such a contact etch stop layer is

deposited, due to the lattice spacing mismatch between the CESL and the underlying layer, a stress develops to match the lattice spacing.

[0005] The stress may have components parallel to the transistor channel and parallel to the transistor width direction. Research has revealed that a CESL that induces a tensile stress field in channel length direction can improve nMOS performance, and compressive stress can improve pMOS performance. In order to increase the beneficial effects and reduce the detrimental effects, it is desired that the tensile stress in the channel length direction be increased for nMOS transistors, and the compressive stress in the channel length direction be increased for pMOS transistors.

[0006] Figure 1 illustrates a conventional nMOS transistor 1. Shallow trench isolations (STI) 4 are formed in the neighborhood of CMOS transistor 1. STIs 4 typically generate a compressive stress to the channel region of the transistor 1. This reduces the carrier mobility and hence degrades the device performance for nMOS transistors. Attempts are made to reduce the detrimental effect of the STIs 4. Figure 2 illustrates one such attempt. The gate structure comprises a dielectric 10, a gate electrode 12 and gate spacers 14. STIs 4 are recessed below the surface of the substrate 2. The removal of the STI material at opposite ends of the device channel 16 eliminates the compressive force caused by the STI material. Silicides 8 are then formed. Since recessing the STIs 4 exposes the silicon substrate 2 at the sidewall 11 of the substrate 2, a silicide penetration 13 is formed on the sidewalls 11 of the STI recesses. The penetrations 13 cause a leakage current and therefore degrade the device performance. Typically, for CMOS transistors with wide junctions (the distance L between STIs 4 is great), there is less of a silicide penetration problem. When the devices are scaled down and the junctions are small, however, the

penetration problem is more severe. Therefore, a method is needed for controlling the stress applied by STI without incurring a silicide penetration.

SUMMARY OF THE INVENTION

[0007] The preferred embodiments of the present invention present a method of improving transistor carrier mobility by adjusting stress through recessing shallow trench isolations.

[0008] In accordance with one aspect of the present invention, a trench is formed in a substrate. The trench is filled with a dielectric material. A CMOS transistor is formed next to the trench. A silicide layer is formed on the surface of the source/drain region. A recess is formed by removing portions of the dielectric material, so that the surface of the dielectric material is substantially lower than the surface of the substrate. The recess may be formed by any removal process, preferably by a selective etch process or etch-back process. The recessing of the STI removes the compressive stress applied to the channel region by STI material. A contact etch stop layer (CESL) is formed over the gate electrode, gate spacers, source/drain and the dielectric material. The CESL also applies a stress to the channel region of the transistor. Since the removal of portions of the STI is performed after the formation of the silicide, there is no silicide penetration.

[0009] In accordance with another aspect of the present invention, the STI is etched back first, and silicides on the source and drain regions are then formed. Trench spacers are formed protecting the substrate material before forming silicides so that there is no silicide formed on the sidewall of the substrate in the recess. Also, a CESL is applied to apply a beneficial stress to the channel of the CMOS device.

[0010] In accordance with yet another aspect of the present invention, the STI has a composite structure. That is, it has one, and optionally two, dielectric liners under the dielectric material. The extra liners not only provide a stress to the channel of the CMOS device, but they

also protect the sidewalls of the substrate in the recess of the STI from forming a silicide penetration.

[0011] By recessing the STI, the stress originally applied by the STI material is reduced or eliminated. The CESL formed in the recess may then apply a desired stress to the channel based on the type of CMOS transistor. The carrier mobility of the CMOS transistor is improved, thus performance is enhanced. The silicide penetration problem is also solved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0013] Figure 1 illustrates a conventional nMOS transistor;

[0014] Figure 2 illustrates a conventional nMOS transistor having a silicide penetration;

[0015] Figures 3 through 7 illustrate a first preferred embodiment of the present invention;

[0016] Figures 8 through 12 illustrate a second preferred embodiment of the present invention; and

[0017] Figures 13 through 16 illustrate a third preferred embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0018] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0019] The preferred embodiments are illustrated in Figures 3 through 16 wherein like reference numbers are used to designate like elements throughout the various views and illustrative embodiments of the present invention.

[0020] Figures 3 through 7 illustrate a preferred embodiment of the present invention. Figure 3 illustrates the formation of shallow trench isolations (STI) 4 in a substrate 2. In the preferred embodiment, substrate 2 is a silicon substrate. In other embodiments, substrate 2 comprises materials such as germanium, carbon, and/or their combinations. STIs 4 are formed in the substrate 2, preferably by etching shallow trenches in substrate 2, then filling the trenches through high density plasma deposition of SiO_2, or HDP oxide. The trenches can also be filled by a dielectric material comprising polysilicon. The process is controlled so that the STI is raised above the substrate 2, preferably about 0Å to about 500Å. By making STIs 4 with an acceptable height, the silicide formed in the subsequent steps is less likely to have penetration formed along the edge of the STIs 4. To improve the performance of the transistor to be formed, the STIs 4 are preferably located such that if a line is drawn between the STIs 4, the line is along the 110 or 100 direction of the substrate lattice structure. Therefore, the orientation of the transistor channel is along the 110 or 100 direction.

[0021] Figure 4 illustrates the formation of a gate stack, spacers, and source and drain regions. A gate dielectric 10 is deposited on the surface of substrate 2. A gate electrode 12 is formed on gate dielectric 10. The gate electrode 12 is preferably polysilicon, although it may be formed of metal, or a compound structure comprising metal, semiconductor, metal oxide and/or silicide.

[0022] A pair of spacers 14 is formed along the sidewalls of the gate dielectric 10 and gate electrode 12. Spacers 14 serve as self-aligning masks for a subsequent source/drain formation process. The spacer material can be oxide, silicon nitride, oxy-nitride or any combinations thereof. The spacers 14 may be formed by well-known methods such as blanket depositing a dielectric layer over substrate 2 and gate electrode 12 using thermal process, low pressure chemical vapor deposition (LPCVD) or plasma enhanced vapor deposition (PECVD), then anisotropically etching the dielectric material to remove the dielectric material from horizontal surfaces but not from the gate electrode sidewalls. In a more preferred embodiment, the spacers 14 comprise a silicon nitride layer formed on an SiO_2 layer. With such a structure, the spacers 14 not only have a high-k of silicon nitride (about 7.5), but they also have the excellent quality of SiO_2. Using silicon nitride in the spacers 14 also makes a selective etching possible when the STIs 4 are etched back.

[0023] Source and drain regions 6 are then formed. Source and drain regions 6 can be formed by implanting the desired dopant into silicon substrate 2 or by recessing the source and drain regions followed by epitaxially growing silicon with desired dopant. The formation of source and drain regions 6 are well known in the art. The details are not repeated herein.

[0024] As illustrated in Figure 5, a metal silicide 8, or a conductive layer, is formed on source and drain regions 6. In the preferred embodiment, silicide layer 8 is formed by first

depositing a thin composite layer of metal, then annealing to form a silicide 8 between the deposited metal and the underlying exposed silicon regions. The metal forming the silicide may be a transition metal or metal compound such as titanium, cobalt, tungsten, tantalum, nickel, or the like or some other appropriate conductive material. The metal can be deposited by chemical vapor deposition (CVD), physical vapor deposition (PVD) or other alternatives. The upper portion of any un-reacted metal is then removed.

[0025] The STIs 4 are then etched back, as shown in Figure 6. A highly selective etching back process is performed so that the spacers 14 are substantially not affected. In the preferred embodiment, a dry etch is performed. As discussed, the spacers 14 preferably comprise a silicon nitride on top, therefore an etchant, or gases that only attack HDP oxide but not silicon nitride, can be used. The etching back distance D is desired to be great enough so that the top portion on opposite sides of the device channel 16 is substantially removed and there is no STI material applying compressive stress to the channel 16. Therefore, it is desired that the top surfaces of the recessed STIs 4 be substantially lower than channel 16 of the CMOS transistor. The top surface of the recessed STIs 4 is lower than the top surface of the substrate 2. Preferably, the recessing depth D is between about 50Å to about 1000Å. It is noted that since the STIs 4 are recessed after the formation of silicide 8, no silicide penetration is formed. A gap G as shown in Figure 6 between the top surfaces of the recessed STIs 4 and the silicide 8 is about 50Å to about 900Å. The gap G defines a portion on the sidewalls of the STIs 4 where silicide penetration may occur.

[0026] Figure 7 illustrates formation of a contact etch stop layer (CESL) 22. This layer serves two purposes: first, it provides stress to the device and enhances carrier mobility; and second, it acts as an etch stop layer to protect underlying regions from being over etched. Since a tensile stress on channel 16 is beneficial to nMOS transistors and a compressive stress is

beneficial to pMOS transistors, a CESL 22 with tensile stress is preferred for an nMOS transistor, and a CESL 22 with compressive stress is preferred for a pMOS transistor. It is desired that the magnitude of the stress applied by the CESL is higher than about 100MPa, and more preferably higher than about 500MPa. In the case where the formed transistor is a pMOS transistor, since the original STI provides a compressive stress if there is no recess formed, the CESL layer 22 is preferred to have a compressive stress higher than the original stress provided by the STI, preferably higher than about 500MPa. As known in the art, contact etch stop layer 22 needs to have a certain thickness to provide enough stress. Therefore a thickness of about 10nm to about 100nm, and more preferably about 50nm, for CESL 22 is desired. In the preferred embodiment, CESL 22 is silicon nitride. In other embodiments, silicon dioxide, SION, and their combinations can also be used.

[0027] Figures 8 through 12 illustrate a second preferred embodiment. Figure 8 illustrates the formation of a gate dielectric 10 and a gate electrode 12 between STIs 4. STIs 4 are etched back, preferably by dry etching, therefore forming recesses 30. The preferred depth D of the recessing 30 is about 50Å to about 1000Å, and more preferably about 700Å.

[0028] Figure 9 illustrates the formation of gate spacers 14 and trench spacers 32. Gate spacers 14 are formed on the sidewalls of the gate dielectric 10 and gate electrode 12. Trench spacers 32 are formed on the sidewalls of the recess 30 in the silicon substrate 2. Preferably, gate spacers 14 and trench spacers 32 are formed at the same time and by the same process. Trench spacers 32 protect the substrate 2 so that it is not exposed from the side.

[0029] Figure 10 illustrates the formation of source and drain regions 6, followed by the deposition of a metal layer 34. In the preferred embodiment, the metal layer 34 is blanket

deposited on regions including electrode 12, spacers 14 and 32, source/drain regions 6 and STIs 4. In other embodiments, the metal layer 34 can also be deposited on source/drain regions 6 only.

[0030] Figure 11 illustrates the formation of silicide 8. After annealing, a silicide 8 is formed between the source/drain regions 6 and metal 34. At the same time, a silicide 35 is formed between the gate electrode 12 and metal layer 34. It is appreciated that the metal 34 formed on trench spacers 32 and gate spacers 14 does not form a silicide layer since there is no underlying silicon/polysilicon. Un-reacted metal is then removed leaving silicides 8 and 35. The trench spacers 32 and gate spacers 14 are exposed.

[0031] Figure 12 illustrates a CESL 22 formed on the silicide 35, gate spacers 14, trench spacer 32, silicides 8 and STIs 4. Similar to the previous embodiment, CESL 22 provides either a tensile stress or a compressive stress to improve carrier mobility.

[0032] It is to be appreciated that in the second preferred embodiment, the silicide 8 is formed after the STIs 4 are recessed. Although the sidewall of the substrate 2 is exposed due to recessing, by forming trench spacers 32, silicide penetration is prevented. Since the trench spacers 32 are formed at the same time the gate spacers 14 are formed, no extra mask is required.

[0033] Yet another preferred embodiment is illustrated in Figures 13 through 16. Figure 13 illustrates the formation of shallow trench isolations. Trenches are formed, preferably by etching the substrate 2. A first trench liner, also called trench liner oxide 50 is formed in a trench. Trench liner oxide 50 is typically a thermal oxide having a preferred thickness of between about 20Å to about 500Å. The liner oxide 50 helps fix the defects of the trench such as damage caused to the exposed surfaces of the trench arising from the etch step. It also rounds the trench corners so that the electrical field is less concentrated at the corners.

[0034] A second trench liner 52 is formed on the first trench liner oxide 50. It has a preferred thickness of between about 20Å to about 200Å. The second trench liner 52 has an inherent stress so that it applies a stress to the channel region of the CMOS transistor that will be formed in subsequent steps. The stress type depends on the type of CMOS transistor. If the transistor is an nMOS transistor, the second trench liner 52 preferably has a tensile stress. Conversely, if the neighboring transistor is a pMOS transistor, the second trench liner 52 preferably has a compressive stress. In either case, the stress is preferably higher than about 100MPa. The second trench liner 52 is a dielectric layer preferably formed of Si_3N_4, SiO_2, SiON, and combinations. It can be formed by CVD, PCVD or other known methods.

[0035] A third dielectric material 54 is then formed filling the remaining space of the trench. Preferably, the third dielectric 54 is a HDP CVD oxide. A CMOS transistor 57 comprising gate dielectric 10, gate electrode 12, gate spacers 14, source/drain regions 6 and silicides 8 is then formed. The resulting structure is shown in Figure 14.

[0036] Figure 15 shows that the third dielectric 54 is selectively etched to form a recess 56. The material of the second trench liner 52 is preferably different from the material of the third dielectric 54. Therefore, when recessing the third dielectric 54, the second trench liner 52 is not attacked. In other embodiments, the first trench oxide 50 can be omitted and the second trench liner 52 can be formed directly in the trench.

[0037] Figure 16 illustrates a CESL 22 formed on the CMOS transistor 57, the first trench liner 50, the second trench liner 52 and the third dielectric 54. The second trench liner 52 and the CESL 22 provide a combined tensile or compressive stress to the channel of the CMOS transistor 57 based on the CMOS transistor type so that the stress applied to the channel region can be adjusted in a greater range.

[0038] In the preferred embodiments discussed above, removal of the STI material at opposite ends of the device channel eliminates the compressive force caused by the STI materials. The applied CESL 22 further changes the stress applied to the device channel region. In order to effectively modify the stress applied by the STI material, the respective top surface of the recessed dielectrics 4 and 54 in Figures 6, 11 and 15 are preferably lower than the bottom of the silicide 8 by a gap G of preferably between about 50Å to about 900Å, and more preferably about 500Å. This gap G ensures that the top surfaces of the recessed dielectric are lower than the channel region so that the benefit of the preferred embodiments of the present invention is maximized.

[0039] The test data has shown that the stress has been significantly modified by using preferred embodiments of the present invention. An exemplary data reveals that for a conventional nMOS transistor, a 520MPa compressive stress is simulated in the channel region. When the first preferred embodiment of the present invention is employed, the detrimental compressive stress is reduced to about 216MPa.

[0040] The preferred embodiments of the present invention improve the carrier mobility and thus improve CMOS transistor performance. The silicide penetration problem is also solved by using various schemes as described.

[0041] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate

from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. An integrated circuit structure comprising:

a substrate;

a MOS device at a surface of the substrate, the MOS device having a source/drain region with at least a portion in the substrate;

a trench in the substrate and adjacent to the MOS device, and wherein the trench has a depth, and wherein a portion of the source/drain region is exposed through a sidewall of the trench;

a dielectric filling a lower portion of the trench; and

a conductive layer directly on the source/drain region, wherein the trench is free from the conductive layer.

2. The integrated circuit structure of claim 1 wherein the substrate comprises a material selected from the group consisting essentially of silicon, germanium or combinations thereof.

3. The integrated circuit structure of claim 1 wherein a depth of the recess is about 50Å to about 1000Å.

4. The integrated circuit structure of claim 1 wherein a top surface of the dielectric is lower than a bottom edge of the conductive layer by a gap of between about 50Å and about 900Å.

5. The integrated circuit structure of claim 1 wherein the dielectric comprises silicon oxide.

6. The integrated circuit structure of claim 1 further comprising an etch stop layer over the conductive layer, the trench and the dielectric, wherein the etch stop layer extends into the recess.

7. The integrated circuit structure of claim 6 wherein the etch stop layer comprises silicon nitride.

8. The integrated circuit structure of claim 6 wherein the etch stop layer comprises silicon oxynitride.

9. The integrated circuit structure of claim 1 wherein the conductive layer is a silicide layer comprising a metal selected from the group consisting essentially of titanium, cobalt, nickel and combinations thereof.

10. The integrated circuit structure of claim 1 further comprising:

a trench liner underlying the dielectric.

11. The integrated circuit structure of claim 1 wherein the trench liner comprises silicon nitride.

12. The integrated circuit structure of claim 1 wherein the trench liner has a thickness of between 20Å and 200Å.

13. The integrated circuit structure of claim 1 further comprising:

an additional trench liner underlying the trench liner.

14. The integrated circuit structure of claim 13 wherein the additional trench liner comprises thermal silicon oxide.

15. The integrated circuit structure of claim 13 wherein the additional trench liner has a thickness of between about 20Å and 500Å.

16. An integrated circuit structure comprising:

a substrate having a trench wherein the trench is partially filled with a dielectric and wherein the dielectric is recessed therefore forming a recess;

a gate dielectric on the substrate;

a gate electrode on the gate dielectric;

a pair of gate spacers on the sidewalls of the gate dielectric and the gate electrode;

a source/drain region in the substrate, the source/drain region being adjacent the gate spacer and adjoining the trench;

a silicide region on the source/drain region, wherein the silicide region is outside of the recess;

a trench liner lining sidewalls of the trench and at least a portion of a sidewall of the silicide region; and

an etch stop layer over the source/drain region and extending to a bottom of the recess, wherein the etch stop layer has a bottom surface lower than the top surface of the source/drain region.

17. The integrated circuit structure of claim 16 wherein the dielectric is lower than the bottom edge of the silicide layer by a gap of between about 50Å and about 900Å.

18. The integrated circuit structure of claim 16 wherein the dielectric comprises silicon oxide.

19. The integrated circuit structure of claim 16 wherein the silicide layer comprises a metal selected from the group consisting essentially of titanium, cobalt, nickel and combinations thereof.

20. The integrated circuit structure of claim 16 wherein the trench liner comprises silicon nitride.

21. The integrated circuit structure of claim 16 wherein the trench liner has a stress of higher than about 100MPa and wherein the stress is a tensile stress if the source/drain region is of n-type or a compressive stress if the source/drain region is of p-type.

22. The integrated circuit structure of claim 16 wherein the trench liner has a thickness of between about 20Å and 200Å.

23. The integrated circuit structure of claim 16 wherein

an additional trench liner underlying the trench liner.

24. The integrated circuit structure of claim 23 wherein the additional trench liner comprises thermal silicon oxide.

25. The integrated circuit structure of claim 23 wherein the additional trench liner has a thickness of between about 20Å and about 500Å.

26. An integrated circuit structure comprising:

a substrate;

a MOS device at a surface of the substrate, the MOS device having a source/drain region with at least a portion in the substrate;

a trench in the substrate and adjacent to the MOS device, wherein a portion of the source/drain region is exposed through a sidewall of the trench;

a trench liner lining sidewalls and a bottom of the trench, wherein the portion of the source/drain region is exposed through the sidewall of the trench is covered by the trench liner;

a dielectric filling a lower portion of a remaining space of the trench filled by the trench liner, and forming a recess in the trench;

a conductive layer directly on the source/drain region, wherein the trench is free from the conductive layer.

27. The integrated circuit structure of claim 26 wherein the trench liner has a top edge higher than a top surface of the source/drain region.

28. The integrated circuit structure of claim 26 wherein the trench liner has a bottom edge lower than a bottom surface of the source/drain region.

29. The integrated circuit structure of claim 26 further comprising:

an additional trench liner underlying the trench liner, wherein the additional trench liner has a top surface higher than a top surface of the source/drain region, and a bottom surface lower than a bottom surface of the source/drain region.