ABSTRACT OF THE DISCLOSURE

METHOD TO REDUCE POLYSILICON DEPLETION IN MOS TRANSISTORS

A method is provided to reduce poly depletion in MOS transistors. Conventionally, after a polysilicon electrode has been doped, an anneal step is usually performed to activate the dopants. However, the anneal step may be insufficient to drive the implanted impurities down the entire depth of the polysilicon electrode. Consequently, a portion of the polysilicon gate nearest to the gate oxide will be depleted of dopants. This poly depletion will have a detrimental effect on the control of the threshold voltage, and hence on the performance of the device. It is disclosed in the present invention a method of forming polysilicon gates where dopant depletion at the interface near the gate oxide layer is alleviated substantially by using laser annealing; however, by first pre-amorphizing the polycrystalline silicon prior to ion implantation to a desired depth such that during laser annealing the dopants will diffuse uniformly to a melt depth. In this manner, poly depletion effect is greatly reduced and hence performance of the device improved. The disclosed method is applicable to both $n^+$ doped polysilicon gates (NMOS) and $p^+$ doped polysilicon gates (PMOS).

Fig. 2i