

ABSTRACT

The present disclosure relates to a hybrid standard cell that includes a semiconductor substrate, a first power rail, a second power rail, a high-speed transistor region and a low-power transistor region. The first power rail and the second power rail are formed above the semiconductor substrate and extend in a first direction and arranged sequentially in a second direction perpendicular to the first direction. The high-speed transistor region and the low-power transistor region are adjacent to each other in the first direction and arranged in a row region between the first power rail and the second power rail. An operation speed of a high-speed transistor formed in the high-speed transistor region is higher than an operation speed of a low-power transistor formed in the low-power transistor region, and a power consumption of the low-power transistor is lower than a power consumption of the high-speed transistor.

FIG. 1