

Description

The invention relates to circuits for separating synchronization signals from a composite video signal.

In a standard NTSC television receiver, an incoming NTSC television signal is coupled via IF stages to a video detector that generates a corresponding NTSC baseband composite video signal. In order to separate the horizontal and vertical sync signals from the composite video signal, a voltage level that is sometimes referred to as the slice, or slicing level signal is established. Typically, the slicing level signal is established at a level that is between the expected level of the tip portion, or peak, of a given sync pulse and the back porch portion of the associated blanking pedestal. When the magnitude of the composite video signal exceeds that of the slicing level signal, such as, for example, during the occurrence of the tip portion of the given sync pulse, an output signal that is the separated sync signal is generated. On the other hand, when the magnitude of the composite video signal is lower than that of the slicing level signal, such as, for example, during an active video portion of a given video line signal of the composite video signal, such output signal is not generated.

FR-A-2514221 is illustrative of a prior art sync separation approach in which a slice level control signal for application to a sync separating comparator stage is derived by averaging the outputs of two locally keyed detectors, one intended to detect sync peak level and the other to detect sync reference level. Recognition of the existence of a synchronized state for the source of detector keying pulses permits operation of the peak level detector as a mean-value detector; otherwise, the peak level detector operates as a peak detector.

Typically, the signal gain of the IF stages that provide the input signal to the video detector is controlled in an automatic gain control (AGC) loop using feedback. In order to obtain noise immunity the slicing level is established at, for example, the mid-range level that is between the expected levels of the tip and the back porch portions, respectively. In some prior art circuits the AGC loop tends to maintain the level of the tip or the back porch portions at a substantially constant predetermined level, provided some conditions are met. The first of such conditions may be that the amplitude of the incoming television signal remains within the regulating range of the AGC loop. The second of such conditions may be that transient variations in the levels of the sync tip and back porch portions that occur from one sync pulse to the next one are small such that the AGC loop, which normally has a slow transient response time, can track such

changes. Transient variations in the composite video signal may occur, for example, when a television receiver is tuned to a different television channel. Such transient variations may also occur as a result of, for example, airplane induced flutter in the incoming television signal or as a result of other types of external noise signals accompanying the incoming television signal.

In some prior art circuits, the slicing level is updated only during the occurrence of the sync pulse by, for example, peak-detecting the composite video signal to obtain the peak voltage of the composite video signal at the proper polarity. Peak detecting may be accomplished by charging a capacitor to, for example, the level of the tip portion of the sync pulse. Updating of the voltage across the capacitor occurs provided, for example, the level of the tip portion of the sync pulse is larger than the voltage across the capacitor at the time the sync pulse occurs. On the other hand, if the level of the tip portion of the sync pulse is lower than the voltage across the capacitor, at the time the sync pulse occurs, the voltage across the capacitor is not affected by the newly received sync pulse. After the voltage across the capacitor is updated, the capacitor is discharged at a rate that is substantially smaller than the charging rate that occurred, as described before, during the occurrence of the corresponding sync pulse. In this way the voltage across the capacitor dynamically tracks variations in the amplitude of the sync pulses, thus causing the slicing level to do the same.

Whether a given sync pulse causes the updating of the slicing level is affected, in such prior art arrangement, by the voltage across the capacitor at the time the sync pulse occurs. The voltage across the capacitor that decreases in the interval between sync pulses is determined by the amplitude of a preceding sync pulse that causes the charging of the capacitor, as well as by the discharge rate of the capacitor.

It may be desirable to update the slicing level after a predetermined interval has elapsed without updating the slicing level such that at the end of the predetermined interval the slicing level is unconditionally updated. In this way the slicing level is updated independently of the slicing level that has existed prior to the end time of the predetermined interval.

In accordance with the present invention, there is provided a sync separator apparatus responsive to a video signal that contains synchronizing and other information for generating from said video signal an output signal that contains separated synchronizing information, including a comparator responsive to said video signal and to a slice level signal for developing said output signal, characterized by: waveform pattern recognition means re-

sponsive to said video signal for generating a first signal when a pulse that is similar in characteristic to a sync signal of said video signal occurs in said video signal, said first signal being indicative of a given level of said pulse; means responsive to said first signal for generating an update control signal when a difference in values of given levels of at least two occurring ones of said pulses or a time-out control signal occurs; means responsive to said first signal for generating said slice level signal said slice level signal being subject to updating in response to said update control signal; and a timer responsive to said update control signal for generating said time-out control signal, provided a predetermined interval has elapsed from a prior updating of said slice level signal.

In accordance with an embodiment of the invention, the update control signal is generated when the level of the pulse has an amplitude which is larger than that of the last pulse that caused the second signal to be updated.

In accordance with a further embodiment of the invention, the time-out control signal causes the second signal to be updated to contain information of most extreme amplitude of the given level that occurs during the predetermined interval.

In accordance with a yet further embodiment of the invention, the predetermined interval that is associated with the time-out signal has a duration that is independent of an amplitude of the video signal.

An embodiment of the present invention, given by way of non-limitative example, will now be described with reference to the accompanying drawings, in which:

FIGURE 1 illustrates a sync separator in accordance with an illustrative embodiment of the invention;

FIGURES 2a-2b illustrate waveforms related to the trailing edge of a sync pulse that are useful in explaining sync pattern recognition operation of the sync separator of FIGURE 1; and

FIGURES 3a-3c illustrate waveforms useful in explaining the operation of the sync separator of FIGURE 1 immediately after a sync pattern is recognized.

FIGURE 1 illustrates a sync separator 200 embodying an aspect of the invention. An analog, baseband composite video signal 100 such as, for example, defined in an NTSC standard, is obtained at an output terminal of, for example, a video detector of a television receiver, not shown in FIGURE 1. Analog signal 100 is sampled and then converted to a digital word in an analog-to-digital converter 27 at a rate $1/T$ that meets the Nyquist sampling criteria, where T is the interval between successive sampling cycles. The rate $1/T$ is equal, illustratively, to 14.32 MHz, four times the color

subcarrier frequency of an NTSC signal. The digitized signal is low-pass filtered in a digital low-pass filter 28 to generate a signal A_{IN} . Signal A_{IN} is coupled to an input port IN of a shift register 24.

Associated with the trailing edge of a given sync pulse H_s of signal A_{IN} is a flat portion FFP that corresponds with the tip portion of sync pulse H_s , a transition portion TR and a flat portion FBP that corresponds with the back porch portion of the associated blanking pedestal. Portion FFP is, illustratively, at a value that is lower, or less positive, than that of portion FBP.

Sync separator 200 stores values representative of portions FFP and FBP, respectively, associated with a given sync pulse H_s to provide, in a manner to be described later, a sync tip signal ST and a back porch signal BK, respectively, that are coupled to corresponding input ports of a summer 21. A slice level signal SL that is produced at an output terminal 21a of summer 21 contains the average value of signals ST and BK. Slice level signal SL having a value that is, illustratively, in the mid-range between the levels of tip portion FFP and the back porch portion FBP associated with sync pulse H_s is coupled to an input terminal 20a of a digital comparator 20. Signal A_{IN} is coupled to an input terminal 20b of comparator 20. Comparator 20 generates a separated sync signal 100a when signal A_{IN} has a value that is, illustratively, lower than that of slice level signal SL. Thus, signal 100a contains the separated sync signals that correspond with sync pulses H_s of signal A_{IN} .

Frequency components at an output terminal 27a of analog-to-digital converter 27 that are higher than the filter cutoff frequency that is between 360 KHz and 500 KHz are substantially reduced in signal A_{IN} by low-pass filter 28. The words of signal A_{IN} are sequentially shifted into shift register 24 at the rate $1/T$. Each storage cell 24n of shift register 24 is capable of storing a corresponding digital word of signal A_{IN} .

A group A_{1b} of, illustratively, five consecutively shifted-in words of signal A_{IN} , that are shifted, or stored, in register 24, are coupled to corresponding input ports of a summer 25 that generates at an output port 25a a signal A_1 that contains in each period T a correspondent word that provides a running average of the five digital words of group A_{1b} . Similarly, a group A_{2b} of, illustratively, five consecutively stored words of signal A_{IN} is coupled to corresponding input ports of a summer 26 that generates a signal A_2 that provides a running average of the five words of group A_{2b} that are stored immediately before the five words of group A_{1b} . Thus, signal A_1 provides the running average of a corresponding portion of signal A_{IN} . Likewise, signal A_2 provides, after a delay interval that is equal to $5T$, the running average of signal A_{IN} . Each of

signals A_1 and A_2 represents signal A_{IN} that is low-pass filtered by this five point averaging process. It should be understood that groups A_{1b} and A_{2b} may include, if desired, common, or overlapping, ones of the storage cells $24n$ of register 24.

Signals A_1 and A_2 are coupled to corresponding input ports of a summer 11 that generates a sum, or average, signal A_{12} at an output port 11a. Signal A_2 is subtracted from signal A_1 in a subtractor 23 to form a difference signal C. Difference signal C is coupled to an input port of a comparator 18 that generates a signal D on a line 18a when signal C, that is equal to the value of signal A_1 minus the value of signal A_2 , is greater than a predetermined positive value K. Signal C is also coupled to an input port of an absolute value converter 19 that generates a signal 0 that is equal to the absolute value of signal C. A comparator 27 generates a signal E on a line 27a when signal 0 is smaller than or equal to a predetermined positive value L that is substantially smaller than K. Signals C, D and E are indicative of the rate of change of signal A_{IN} . Signals D and E are coupled to a controller 28 that performs the control functions of separator 200, in accordance with, for example, signals D and E. When the rate of change of signal A_{IN} is small, corresponding to a flat portion of signal A_{IN} , signal E is generated. When the rate of change of signal A_{IN} is positive and large, corresponding with, for example, the trailing edge TR of sync pulse H_s , signal D is generated.

Controller 28 may be constructed using conventional control logic. For example, controller 28 may include a logic sequencer or microcomputer operating in accordance with microinstructions of a microprogram that is stored in a read only memory, not shown in FIGURE 1 and that performs the procedure described below.

During operation in a search mode, controller 28 searches for and recognizes in the waveform of signal A_{IN} , a predetermined waveform pattern occurring in a corresponding part of signal A_{IN} by detecting the occurrence of a predetermined rate of change of signal A_{IN} . The waveform pattern, that occurs in the corresponding part of signal A_{IN} , may be indicative of the occurrence of the trailing edge of a given sync pulse H_s . The operation in the search mode is described in detail in European Patent Application (RCA Docket 81,944), filed concurrently herewith.

During a first step of the operation in the search mode, controller 28 generates a clock signal CT5 and a clock signal CT2. Each signal CT5 and CT2 occurs at a rate of, illustratively, $1/T$. Sum signal A_{12} that provides the average value of signals A_1 and A_2 is coupled to an input port of a register 17. Clock signal CT5 causes, in each period T, a corresponding word of signal A_{12} to be

stored in register 17. A signal ST2 at an output port of register 17 contains the stored word of signal A_{12} . Similarly, sum signal A_{12} is coupled to an input port of a register 14. Clock signal CT2 causes, in each period T in which clock signal CT2 is generated, a corresponding word of signal A_{12} to be stored in register 14. A signal BK2 at an output port of register 14 contains the corresponding word of signal A_{12} that is stored in register 14. Operation of controller 28 in the search mode is explained with the aid of FIGURES 2a and 2b.

FIGURE 2a illustrates schematically the digitized values of signal A_{IN} that are associated with the trailing edge of, for example, horizontal sync pulse H_s of FIGURE 1. Sync pulse H_s includes flat portion FFP followed by transition portion TR, that is then followed by flat portion FBP of the associated blanking pedestal. FIGURE 2b illustrates schematically the digitized values of signals A_1 and A_2 that correspond with signal A_{IN} . Similar numbers and symbols in FIGURES 1, 2a and 2b indicate similar items or functions.

In the first step of the operation in the search mode, controller 28 of FIGURE 1 tests line 27a in each period T for detecting the occurrence of signal E. As can be seen in FIGURE 1b, signal E of FIGURE 1 is generated when a flat portion occurs in signal A_{IN} of FIGURE 2a such as portion FFP. After signal E of FIGURE 1 is detected in each of, illustratively, at least five consecutive tests, controller 28 tests line 27a for detecting the first nonoccurrence of signal E. Signal E is no longer detected when a positive transition at a rate that exceeds the value L occurs in signal A_{IN} , or A_{12} , such as when transition portion TR of FIGURE 2a occurs. When signal E of FIGURE 1 is no longer detected, such as, for example, after time T_{11} of FIGURE 2b, controller 28 of FIGURE 1 terminates the generation of clock signal CT5 such that last value of signal A_{12} that appears concurrently with signal E is stored in register 17. Signal E is indicative of a slow rate of change of signal A_{IN} . Thus, signal ST2 of register 17 remains at a level that is indicative of, illustratively, the level of flat portion FFP of signal A_{IN} of FIGURE 2a. When signal E of FIGURE 1 is no longer detected, such as immediately after time T_{11} of FIGURE 2b, controller 28 of FIGURE 1 immediately generates a signal CT1 that resets, or initializes, a counter 41 to zero. After being initialized by signal CT1, counter 41 begins counting up, in each period T. Counter 41 generates a signal TRTO when, for example, a period of $32T$ has elapsed from the time signal CT1 initializes counter 41.

In the next step, controller 28 tests line 18a of FIGURE 1 in each subsequent period T for detecting the occurrence of signal D. Signal D is indicative of an upramping positive transition in signal A_{IN}

of FIGURE 2a at a rate of change, or slope, that exceeds the value K. The value K is substantially larger than the value L that is indicative of the slope of signal A_{IN} when signal E was generated. Thus, signal D of FIGURE 1 is generated at, for example, time T_7 of FIGURE 2b. The occurrence of signal D in, illustratively, at least each of five consecutive tests is indicative of the occurrence of an upramping transition such as, for example, caused by portion TR of signal A_{IN} of FIGURE 2a.

In the last step of the search mode, controller 28 of FIGURE 1 tests line 27a, in each period T that follows, for detecting signal E again. Signal E is now indicative of, illustratively, the occurrence of back porch portion FBP of signal A_{IN} of FIGURE 2a. When signal E of FIGURE 1 is detected, such as, for example at time T_{12} of FIGURE 2b, controller 28 of FIGURE 1 terminates the generation of clock signal CT2 that stores signal A_{12} in register 14. Thus, signal BK2 of register 14 remains, after signal E is detected again, at a level that is indicative of, illustratively, the level of back porch portion FBP of signal A_{IN} FIGURE 2a.

If the sequence of tests, that was described above, that terminates at, for example, time T_{12} of FIGURE 2b, occurs before signal TRTO of counter 41 of FIGURE 1 is generated, in that it occurs within the period of $32T$ from the time signal CT1 is generated, the corresponding part waveform of signal A_{IN} has a waveform pattern that is substantially similar in characteristic to that associated with the trailing edge of a given sync pulse H_s . It should be understood that because signals A_1 and A_2 are low-pass filtered, a transition in signal A_{IN} that occurs after, for example, time T_{11} of FIGURE 2b that is not similar to the trailing edge of pulse H_s , will cause signal TRTO to be generated. A search mode at the end of which the pattern is recognized is referred to herein as the successful search mode. In contrast, if signal TRTO of counter 41 is generated prior to the completion of such sequence, controller 28 begins operating at the first step of the search mode by testing, as described before, line 27a for detecting the occurrence of five consecutive tests in which signal E occurs.

Signals ST2 and BK2 are coupled to corresponding input ports of a register 16. When controller 28 generates a clock signal CT4, both signals ST2 and BK2 are stored in register 16 to form a signal ST1 and a signal BK1, respectively, at corresponding output ports of register 16. Similarly, signals ST1 and BK1 are coupled to corresponding input ports of a register 15. When controller 28 generates a clock signal CT3, both signals ST1 and BK1 are stored in register 15 to form sync tip signal ST and back porch signal BK, respectively, at corresponding output ports of register 15. Signals ST and BK are summed in summer 21 for

generating slice level signal SL, as described before. Thus, signals ST2 and BK2 may be stored, via register 16, in register 15 to form signals ST and BK, respectively.

Signal CT3 is also coupled to an input terminal 40b of a flip-flop 40. When signal CT3 is applied to terminal 40b, flip-flop 40 is caused to be at a "RESET" state such that an output signal ST1VD of flip-flop 40 is at a logical "FALSE" state. Clock signal CT4 that is used for storing signals ST2 and BK2 in register 16 is also coupled to an input terminal 40a of flip-flop 40. Signal CT4 causes flip-flop 40 to be at a "SET" state to provide signal ST1VD at a logical "TRUE" state. Signal ST1VD at logical "TRUE" state is indicative of the fact that signals ST1 and BK1 of register 16 have not yet been transferred to register 15; whereas, signal ST1VD at a logical "FALSE" state indicates that these signals have been transferred.

Output signals ST, ST1 and ST2 are coupled to a comparator 22 that generates a signal F, on a line 22a, when signal ST is smaller than or equal to signal ST1. A signal G of comparator 22 is generated on a line 22b when signal ST1 is smaller than or equal to signal ST2. Signals F, G and ST1VD, are coupled to corresponding input terminals of controller 28 for controlling the operation in a sync processing mode that immediately follows the corresponding successful search mode.

After the occurrence of the successful search mode, in which the pattern was recognized in signal A_{IN} , controller 28 processes signals ST2 and BK2 for establishing the corresponding values of signal ST1, BK1, ST, BK, and SL, as described later on. After establishing such values, operation in the search mode resumes at the first step, as described before.

At the end of each successful search mode, output signal ST2 of register 17 contains the average value of the part of signal A_{IN} that corresponds with, illustratively, flat portion FFP of FIGURE 2a. Similarly, output signal BK2 of register 14 of FIGURE 1 contains the average value of the part of signal A_{IN} that corresponds with, illustratively, flat portion FBP of FIGURE 2a.

In accordance with a preferred feature of the invention, if signal ST2 at the end of the corresponding successful search mode is smaller than signal ST, signal ST2 is immediately stored in register 15 for updating signal ST. Such updating of signal ST is justified because it is likely that such successful search mode was caused by the occurrence of sync pulse H_s and not by a signal transition in another part of signal A_{IN} such as during the active video interval. After signal ST is updated, operation at the first step of the search mode is resumed, as described before.

Assume a situation in which during an interval T_{10} , having a duration that is, illustratively, slightly longer than a horizontal interval H , following the last time signal ST has been updated, one or more successful search modes operations occur. Assume further that at the end of each such successful search mode, the corresponding level of signal $ST2$ was higher than that of signal ST .

In accordance with another preferred feature of the invention, when the last mentioned situation occurs, the lowest level of signal $ST2$ obtained at the end of a corresponding successful search mode that occurs during interval T_{10} is stored in register 15. Such lowest level of signal $ST2$ is stored at the end of interval T_{10} in order to update signal ST . Typically, the level of signal $ST2$ that corresponds with sync tip portion FFP of sync pulse H_s is lower than that of signal $ST2$ that does not correspond with portion FFP, even when signal A_{IN} is distorted or accompanied by a moderate level of noise. Consequently, in the typical case, signal $ST2$ resulted from a transition that occurs during, for example, the active video interval of a given video line of signal A_{IN} , advantageously, will not affect signal ST .

A first and a second hypothetical situation demonstrate the ways signals ST , BK and SL are updated at the end of the corresponding operation in the successful search mode. The first hypothetical situation occurs when at the end of a given successful search mode, signal $ST1VD$ is at logical "FALSE" state, indicating that signals $ST1$ and $BK1$ of registers 16 have already been stored in, or transferred to, register 15. In this case, signals $ST2$ and $BK2$ are stored by signal $CT4$ in register 16 to form updated signals $ST1$ and $BK1$, respectively; simultaneously, flip-flop 40 is set by signal $CT4$, causing signal $ST1VD$ to be at the logical "TRUE" state to indicate that signals $ST1$ and $BK1$ contain information that has not been transferred yet to register 15. If signal $ST1$, now being equal to signal $ST2$, is smaller than signal ST , updated signals $ST1$ and $BK1$ are stored in register 15 by signal $CT3$. Thus, when signal $ST2$ of the newly received sync pulse H_s is at a level that is lower than that of signal ST , signal $ST2$ and the associated signal $BK2$ are transferred, via register 16, to register 15 to form updated signals ST and BK , respectively, and operation begins at the first step of the subsequent search mode, as described before.

Controller 28 determines that signal $ST2$, now being equal to signal $ST1$, is smaller than signal ST by testing line 22a for detecting the absence of signal F . Because signal $CT3$ was generated in the course of storing signals $ST1$ and $BK1$ in register 15, output signal $ST1VD$ of flip-flop 40 returns to the logical "FALSE" state to indicate that signals $ST1$ and $BK1$ of register 16 have already been

stored in register 15.

If signal ST is smaller than or equal to signal $ST1$, signals $ST1$ and $BK1$ of register 16 are not immediately transferred to register 15 and signal $ST1VD$ remains at the logical "TRUE" state. Thereafter, operation begins at the first step of the subsequent search mode.

A second hypothetical situation occurs when, prior to, for example, the first step of a given successful search mode, signals $ST1$ and $BK1$ have not been stored in, or transfer to, register 15, as indicated by signal $ST1VD$ being at the "TRUE" state. If, signal $ST2$, at the end of the such successful search mode, is larger than or equal to signal $ST1$, signals $ST2$ and $BK2$ will not be stored in register 16; consequently signals $ST1$ and $BK1$ will remain unchanged. The result is that signal $ST1$ remains equal to the lowest value of signal $ST2$ obtained since the last time signal ST has been updated. On the other hand, if signal $ST2$, at the end of such successful search mode, is at a level that is lower than that of signal $ST1$, signals $ST2$ and $BK2$ are stored in register 16 for updating signals $ST1$ and $BK1$, respectively. Again, the result is that signal $ST1$ is equal to the lowest value of signal $ST2$ obtained since the last time signal ST has been updated.

After signal $ST2$ is stored in register 16, the new value of signal $ST1$ is further compared with signal ST . In the same way discussed before, if signal ST is at a level that is lower than that of signal $ST1$, signal ST remains unchanged and signal $ST1VD$ remains at logical "TRUE" state, for the reasons discussed before. Thereafter, operation begins at the first step of the subsequent search mode. However, if signal $ST1$ is at a level that is lower than that of signal ST , signal $ST1$ and $BK1$ are stored in register 15 to form updated sync tip signal ST and back porch signal BK , respectively. Signal $CT3$ that causes signals $ST1$ and $BK1$ to be stored in register 15, also causes signal $ST1VD$ to assume the logical "FALSE" state. Thereafter, operation begins at the first step of the subsequent search mode.

Signal $CT3$ that supplies the clock signal to register 15 is also coupled to an input terminal 30b of a time-out counter 30. Signal $CT3$ resets, or initializes, counter 30 to zero each time signals $ST1$ and $BK1$ are stored in register 15. Counter 30 counts up from zero immediately after signal $CT3$ is applied. If signal $CT3$ does not occur again within time-out interval T_{10} , that is, illustratively, slightly longer than a horizontal line period H , and that occurs after the last time signals ST and BK have been updated, counter 30 generates a time-out signal TO at a terminal 30a. If signals ST and BK have not been updated within an interval that is equal to, illustratively, period H , it is assumed that

the lowest level of signal ST1 within such interval has been caused by portion FFP of sync pulse H_s . Signal TO that is coupled to a corresponding input terminal of controller 28 is indicative of the fact that signals ST and BK have not been updated within, for example, the immediately preceding horizontal period H. After signal TO occurs, controller 28 generates signal CT3 that stores signals ST1 and BK1 of register 16 in register 15 for updating signals ST and BK, respectively. Signals ST and BK are updated in order to track or follow the levels of portions FFP and FBP, respectively, of signal H_s . In this way, slice level signal SL is established at the desired level even when signal 100 is distorted by, for example, airplane flutter. Thereafter, operation begins at the first step of the subsequent search mode.

In accordance with yet another preferred feature of the invention, interval T_{10} that determines the maximum length of time between instants in which slice level signal SL is updated is predetermined, or known in advance, at the beginning time of interval T_{10} and is controlled independently of the amplitude of sync pulse H_s . The beginning time of each interval T_{10} occurs, for example, at the time signal SL has been lastly updated. In contrast, in some prior art circuits such maximum length of time between the instants in which the slice level signal is updated may be a function of, for example, the amplitude of the sync pulse.

As described before, signal ST1 that is stored in register 16 is equal to the lowest value of signal ST2 that has occurred, at the end of the corresponding successful search mode, since the last time signals ST and BK have been updated. After signal CT3 is generated for updating signals ST and BK, signal ST1VD is at the logical "FALSE" state and counter 30 begins counting up again from zero for beginning a new period.

FIGURES 3a-3c illustrate waveforms useful in explaining the operation of separator 200 of FIGURE 1 after the end of the corresponding operation in the successful search mode. Similar numbers and symbols in FIGURES 1, 2a-2b and 3a-3b indicate similar items or functions.

In the example of FIGURE 3a, signal A_{IN} includes sync tip portions FFP having levels, respectively, that are different in correspondingly different sync pulses H_s . Such variations in signal A_{IN} may be caused by, for example, a noise related disturbance or airplane flutter. Signal A_{IN} includes a sync pulse $H_{s(1)}$ has sync tip portion FFP₍₁₎, causing signal ST2₍₁₎ to be at a level that is lower, during the occurrence of pulse $H_{s(1)}$, than that of sync tip signal ST. A second sync pulse $H_{s(2)}$ of signal A_{IN} has sync tip portion FFP₍₂₎ causing signal ST2₍₂₎ to be at a higher level than that of slice level signal SL, during the occurrence of pulse $H_{s(2)}$. Sync

pulse $H_{s(3)}$ has sync tip portion FFP₍₃₎, causing signal ST₍₃₎ to be at a lower level than that of sync tip signal ST, during the occurrence of pulse $H_{s(3)}$. The waveform of signal A_{IN} shows an example in which the AGC loop of a television receiver, not shown in the FIGURES, is not capable of tracking fast changes in sync tip portions FFP of signal A_{IN} of FIGURE 3a. Had the AGC loop been able to track the fast changes in signal A_{IN} , portions FFP₍₁₎, FFP₍₂₎ and FFP₍₃₎ would have been at substantially the same level.

FIGURE 3b illustrates schematically an example of the count number, or state, of counter 30 of FIGURE 1. The count number of counter 30, shown schematically in FIGURE 3b as an upramping signal, increases until signal CT3 of FIGURE 1 is generated. When signal CT3 is generated, the count number becomes zero. Signal TO is generated if the count number has reached a predetermined value, occurring after time-out interval T_{10} of FIGURE 3a that is, illustratively, slightly longer than period H, has elapsed since the last time signals ST and BK have been updated.

At time t_1 of FIGURE 3a, after the predetermined pattern is recognized in the waveform of pulse $H_{s(1)}$, signal ST2₍₁₎ that corresponds with the level of portion FFP₍₁₎ is at a lower level than that of signal ST. Signal ST2₍₁₎ and the corresponding signal BK2₍₁₎ are then transferred to register 15 via register 16 of FIGURE 1 for updating signals ST and BK, respectively, to generate a new level for slice level signal SL. Counter 30 is reset to a count number that is equal to zero. At time t_2 of FIGURE 3a, after the predetermined pattern is recognized in pulse $H_{s(2)}$, signal ST2₍₂₎ that is at a level higher than that of signal ST, and the corresponding signal BK₍₂₎, are transferred to, or stored in, register 16 of FIGURE 1. Signals ST, BK and SL, however, are not updated at this time. At time t_3 of FIGURE 3b, time-out signal TO of FIGURE 1 is generated, because signals ST and BK have not been updated in the preceding interval T_{10} . When signal TO occurs, signal ST1 and the corresponding signal BK1 of register 16 are stored in register 15 to form updated signal ST. At time t_4 of FIGURE 3a, signal ST2₍₃₎ and the corresponding signal BK2₍₃₎ are stored in register 15, via register 16 of FIGURE 1, so as to update signals ST, BK and SL.

The example of FIGURE 3a shows that even when the AGC loop, not shown in the FIGURES, is not capable of tracking the level of tip portion FFP of sync pulse H_s of signal A_{IN} , signal ST, of FIGURE 3a is, advantageously, capable of tracking the level of sync tip portion FFP; likewise, signal BK is, advantageously, capable of following the level of back porch portion FBP. Advantageously, even when the amplitude of sync pulse H_s varies significantly, slice level signal SL is automatically estab-

lished at the mid-range between portions FBP and FFP.

FIGURE 3c illustrates separated sync signals SSP of sync signal 100a that are separated by comparator 20 of FIGURE 1 and that correspond with signal A_{IN} of FIGURE 3a. Because flat portion FFP₍₂₎ of sync pulse $H_{s(2)}$ is higher than slice level signal SL, no separated sync signal SSP occurs during the occurrence of pulse $H_{s(2)}$. However, the next signal SSP₍₃₎, does advantageously, occur. Thus, when a fast change in signal A_{IN} occurs, slice level signal SL of FIGURE 1 is, advantageously, capable of tracking such fast change even when the AGC loop is not capable of doing so.

It should be understood that signals ST and BK of FIGURE 1 are also properly updated during vertical blanking because, in NTSC, horizontal rate pulse H_s occurs also during each period H of the vertical blanking interval.

In accordance with a further preferred feature of the invention, operations of sync separator 200 of FIGURE 1 that follow the occurrence of a given successful search mode and that result in updating slice level signal SL may be performed, instead, following a well known mode of operation that is different from the successful search mode described above but that also identifies a waveform pattern that is similar in characteristic to that of a given valid sync pulse H_s . For example, such mode of operation may identify sync pulse H_s by peak-detecting signal A_{IN} to obtain the most extreme amplitude of signal A_{IN} at the proper polarity. Such most extreme amplitude may correspond with sync pulse H_s .

Claims

1. A sync separator apparatus responsive to a video signal (100) that contains synchronizing and other information for generating from said video signal an output signal (100a) that contains separated synchronizing information, including a comparator (20) responsive to said video signal (100) and to a slice level signal (SL) for developing said output signal, characterized by:

waveform pattern recognition means (24,25,26,11) responsive to said video signal for generating a first signal (A12) when a pulse that is similar in characteristic to a sync signal of said video signal occurs in said video signal, said first signal (A12) being indicative of a given level of said pulse;

means (22,28) responsive to said first signal (A12) for generating an update control signal (CT3) when a difference in values of given levels of at least two occurring ones of said pulses, or a time-out control signal (TO) occurs;

means responsive to said first signal (A12) for generating said slice level signal (SL) said slice level signal being subject to updating in response to said update control signal (CT3); and

a timer (30) responsive to said update control signal (CT3) for generating said time-out control signal (TO), provided a predetermined interval has elapsed from a prior updating of said slice level signal.

2. An apparatus according to claim 1 wherein said predetermined interval that is associated with said time-out signal has a duration that is independent of an amplitude of said video signal.
3. An apparatus according to claim 1 or claim 2 wherein said interval is of a fixed duration.
4. An apparatus according to claim 1 wherein said given level corresponds to a tip portion of said sync signal of said video signal.
5. An apparatus according to claim 4 wherein said first signal additionally includes a component indicative of the level of a porch portion of said sync signals.
6. An apparatus according to claim 4 or 5 further comprising means for generating a signal that is indicative of the level (BK2) of a porch portion (FBP) of said sync signal, wherein said first signal (A12) is also indicative of the level of the porch portion of said sync signal.
7. An apparatus according to any one of the preceding claims wherein said time-out control signal (TO) causes said second signal to be updated to contain information of most extreme amplitude of said given level that occurs during said predetermined interval.

Patentansprüche

1. Synchronsignal-Abtrennvorrichtung, die auf ein Videosignal (100) anspricht, das synchronisierende oder andere Informationen enthält, um aus dem Videosignal ein Ausgangssignal (100a) zu erzeugen, das eine getrennte synchronisierende Information enthält, mit einer Vergleichsschaltung (20), die auf das Videosignal (100) und auf ein Scheibenpegelsignal (SL) anspricht, um das Ausgangssignal zu entwickeln, gekennzeichnet durch

Erkennungsmittel (24, 25, 26, 11) für das Wellenformschema, die auf das Videosignal ansprechen, um ein erstes Signal (A12) zu



lished at the mid-range between portions FBP and FFP.

FIGURE 3c illustrates separated sync signals SSP of sync signal 100a that are separated by comparator 20 of FIGURE 1 and that correspond with signal A_{IN} of FIGURE 3a. Because flat portion $FFP_{(2)}$ of sync pulse $H_{s(2)}$ is higher than slice level signal SL, no separated sync signal SSP occurs during the occurrence of pulse $H_{s(2)}$. However, the next signal $SSP_{(3)}$, does advantageously, occur. Thus, when a fast change in signal A_{IN} occurs, slice level signal SL of FIGURE 1 is, advantageously, capable of tracking such fast change even when the AGC loop is not capable of doing so.

It should be understood that signals ST and BK of FIGURE 1 are also properly updated during vertical blanking because, in NTSC, horizontal rate pulse H_s occurs also during each period H of the vertical blanking interval.

In accordance with a further preferred feature of the invention, operations of sync separator 200 of FIGURE 1 that follow the occurrence of a given successful search mode and that result in updating slice level signal SL may be performed, instead, following a well known mode of operation that is different from the successful search mode described above but that also identifies a waveform pattern that is similar in characteristic to that of a given valid sync pulse H_s . For example, such mode of operation may identify sync pulse H_s by peak-detecting signal A_{IN} to obtain the most extreme amplitude of signal A_{IN} at the proper polarity. Such most extreme amplitude may correspond with sync pulse H_s .

Claims

1. A sync separator apparatus responsive to a video signal (100) that contains synchronizing and other information for generating from said video signal an output signal (100a) that contains separated synchronizing information, including a comparator (20) responsive to said video signal (100) and to a slice level signal (SL) for developing said output signal, characterized by:

waveform pattern recognition means (24,25,26,11) responsive to said video signal for generating a first signal (A12) when a pulse that is similar in characteristic to a sync signal of said video signal occurs in said video signal, said first signal (A12) being indicative of a given level of said pulse;

means (22,28) responsive to said first signal (A12) for generating an update control signal (CT3) when a difference in values of given levels of at least two occurring ones of said pulses, or a time-out control signal (TO) occurs;

means responsive to said first signal (A12) for generating said slice level signal (SL) said slice level signal being subject to updating in response to said update control signal (CT3); and

a timer (30) responsive to said update control signal (CT3) for generating said time-out control signal (TO), provided a predetermined interval has elapsed from a prior updating of said slice level signal.

2. An apparatus according to claim 1 wherein said predetermined interval that is associated with said time-out signal has a duration that is independent of an amplitude of said video signal.
3. An apparatus according to claim 1 or claim 2 wherein said interval is of a fixed duration.
4. An apparatus according to claim 1 wherein said given level corresponds to a tip portion of said sync signal of said video signal.
5. An apparatus according to claim 4 wherein said first signal additionally includes a component indicative of the level of a porch portion of said sync signals.
6. An apparatus according to claim 4 or 5 further comprising means for generating a signal that is indicative of the level (BK2) of a porch portion (FBP) of said sync signal, wherein said first signal (A12) is also indicative of the level of the porch portion of said sync signal.
7. An apparatus according to any one of the preceding claims wherein said time-out control signal (TO) causes said second signal to be updated to contain information of most extreme amplitude of said given level that occurs during said predetermined interval.

Patentansprüche

1. Synchronsignal-Abtrennvorrichtung, die auf ein Videosignal (100) anspricht, das synchronisierende oder andere Informationen enthält, um aus dem Videosignal ein Ausgangssignal (100a) zu erzeugen, das eine getrennte synchronisierende Information enthält, mit einer Vergleichsschaltung (20), die auf das Videosignal (100) und auf ein Scheibenpegelsignal (SL) anspricht, um das Ausgangssignal zu entwickeln, gekennzeichnet durch

Erkennungsmittel (24, 25, 26, 11) für das Wellenformschema, die auf das Videosignal ansprechen, um ein erstes Signal (A12) zu



erzeugen, wenn ein Impuls in dem Videosignal auftritt, der in seinen Eigenschaften einem Synchronsignal des Videosignals gleicht, wobei das erste Signal (A12) ein Maß für einen gegebenen Pegel des Impulses ist;

Mittel (22, 28), die auf das erste Signal (A12) ansprechen, um ein Aktualisierungs-Steuersignal (CT3) zu erzeugen, wenn eine Differenz in Werten mit gegebenen Pegeln von wenigstens zwei auftretenden Impulsen oder ein Zeitsperr-Steuersignal (T0) auftritt;

Mittel, die auf das erste Signal (A12) ansprechen, um das Scheibenpegelsignal (SL) zu erzeugen, wobei das Scheibenpegelsignal einer Aktualisierung in Abhängigkeit von dem Aktualisierungs-Steuersignal (CT3) unterworfen wird; und

einen Zeitgeber (30), der auf das Aktualisierungs-Steuersignal (CT3) anspricht, um das Zeitsperr-Steuersignal (T0) zu erzeugen, sofern ein vorbestimmtes Intervall seit einer früheren Aktualisierung des Scheibenpegelsignals verstrichen ist.

2. Vorrichtung nach Anspruch 1, bei der das vorbestimmte Intervall, das dem Taktsperr-Signal zugeordnet ist, eine Dauer hat, die unabhängig von einer Amplitude des Videosignals ist. 25
3. Vorrichtung nach Anspruch 1 oder 2, bei der das Intervall eine feste Dauer hat. 30
4. Vorrichtung nach Anspruch 1, bei der der gegebene Pegel einem Spitzenteil des Synchronsignals des Videosignals entspricht. 35
5. Vorrichtung nach Anspruch 4, bei der das erste Signal zusätzlich eine Komponente enthält, die ein Maß für den Pegel eines Schwarzschilderteils des Synchronsignals ist. 40
6. Vorrichtung nach Anspruch 4 oder 5, bei der Mittel zur Erzeugung eines Signals vorgesehen sind, das ein Maß für den Pegel (BK2) eines Schwarzschilderteils (FBP) des Synchronsignals ist, wobei das erste Signal (A12) ebenfalls ein Maß für den Pegel des Schwarzschilderteils des Synchronsignals ist. 45
7. Vorrichtung nach einem der vorhergehenden Ansprüche, bei dem das Zeitsperr-Steuersignal (T0) die Aktualisierung des zweiten Signals bewirkt, damit dieses eine Information über die äußerste Amplitude des gegebenen Pegels enthält, der während des vorgegebenen Intervalls auftritt. 50

Revendications

1. Circuit séparateur de signaux de synchronisation agissant en réponse à un signal vidéo (100) qui contient une information de synchronisation et d'autres informations pour générer, à partir dudit signal vidéo, un signal de sortie (100a) qui contient de l'information de synchronisation séparée, comprenant un comparateur (20) agissant en réponse audit signal vidéo (100) et à un signal de niveau de tranche (SL) pour développer ledit signal de sortie, caractérisé par :
 - des moyens de reconnaissance de configuration de forme d'ondes (24, 25, 26, 11), agissant en réponse audit signal vidéo pour générer un premier signal (A12) quand une impulsion, dont la caractéristique est similaire à un signal de synchronisation dudit signal vidéo, apparaît dans ledit signal vidéo, ledit premier signal (A12) constituant une indication d'un niveau donné de ladite impulsion,
 - des moyens (22, 28) agissant en réponse audit premier signal (A12) pour générer un signal de commande de réactualisation (CT3) quand apparaît une différence de valeurs des niveaux donnés d'au moins deux desdites impulsions surveillées, ou un signal de commande de temporisation (ST0) ;
 - des moyens agissant en réponse audit premier signal (A12) pour générer ledit signal de niveau de tranche (SL), ledit signal de niveau de tranche étant soumis à une réactualisation en réponse audit signal de commande de réactualisation (CT3) et,
 - un séquenceur (30) agissant en réponse audit signal de commande de réactualisation (CT3) pour générer ledit signal de commande de temporisation (T0), à condition qu'un intervalle prédéterminé se soit écoulé à partir d'une réactualisation antérieure dudit signal de niveau de tranche.
2. Dispositif selon la revendication 1 dans lequel ledit intervalle prédéterminé qui est associé audit signal de temporisation présente une durée qui est indépendante d'une amplitude dudit signal vidéo.
3. Dispositif selon la revendication 1 ou 2 dans lequel ledit intervalle est de durée fixe.
4. Dispositif selon la revendication 1 dans lequel le niveau donné correspond à la portion d'ex-



trémité dudit signal de synchronisation dudit signal vidéo.

5. Dispositif selon la revendication 4 dans lequel ledit premier signal comporte en outre une composante indiquant le niveau d'une portion de palier desdits signaux de synchronisation. 5
6. Dispositif selon la revendication 4 ou 5 comprenant en outre des moyens pour générer un signal qui est une indication du niveau (BK2) d'une portion de palier (FBP) dudit signal de synchronisation, dans lequel ledit premier signal (A12) est également une indication du niveau de la portion de palier dudit signal de synchronisation. 10 15
7. Dispositif selon l'une quelconque des revendications précédentes dans lequel le signal de commande de temporisation (T0) entraîne une réactualisation dudit second signal pour qu'il contienne de l'information de l'amplitude la plus extrême dudit niveau donné qui survient pendant ledit intervalle prédéterminé. 20 25

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